22639

23124

3 Hours / 70 Marks Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

Marks

1. Attempt any FIVE of the following : **10**

(a) Define the terms : Power fan-out and skew.

(b) Write the applications of test bench.

(c) List the data types in VHDL.

(d) Write two examples of sequential construct in VHDL.

(e) Define Mealy machine and draw the diagram for it.

(f) State the concept of delta delay.

(g) Draw the simplified CMOS logic for the NAND gate.

2. Attempt any THREE of the following : **12**

(a) Compare CPLD and FPGA on the basis of flexibility, capacity and any other two parameters.

(b) Write the VHDL code for 3 bit right shift register.

(c) Explain the estimation process of resistance with layout diagram.

(d) Explain the different delays in VHDL simulation.

3. Attempt any THREE of the following : **12**

(a) Draw the circuit of CMOS inverter and its characteristics.

(b) Write the VHDL code for 8:1 multiplexer.

(c) Explain various operators used in VHDL.

(d) Write the Pro's and Con's of VHDL.

4. Attempt any THREE of the following : **12**

(a) Explain with block diagram the architecture of FPGA.

(b) Draw the CMOS transistor cross-section diagram and layout diagram using Twin tub process.

(c) Explain the HDL design flow for synthesis process.

(d) Compare BJT and CMOS technology.

(e) Design following function using CMOS logic : $Z = \overline{AB} + (\overline{C + D})$.

5. Attempt any TWO of the following : **12**

(a) Design the Moore or Mealy machine for detecting the sequence 1011.

(b) Explain any two processes :

(i) Diffusion (ii) Oxidation (iii) Deposition

(c) Write the VHDL code for 2 input EX-OR gate using –

(i) Behavioural modelling and (ii) Data flow modelling

6. Attempt any TWO of the following : **12**

(a) Explain the following terms related to VHDL simulation :

(i) Event scheduling, (ii) Zero modelling (iii) Sensitivity list

(b) Explain ASIC design flow with neat sketch.

(c) Explain the following terms with respect to VHDL with example :

(i) Entity (ii) Architecture (iii) Configuration

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