23124

3 Hours / 70 Marks Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Use of Non-programmable Electronic Pocket Calculator is permissible.

(7) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. Attempt any FIVE of the following : **10**

(a) Draw symbol and construction of npn transistor.

(b) Write the classification of power amplifier.

(c) State Barkhausen criterion for sustained oscillations.

(d) In an RC phase shift oscillator the value of resistor R = 10 kΩ and capacitor C = 3.25 nF. Calculate frequency of oscillation.

(e) Write classification of wave shaping networks.

(f) Define load regulation. Write its value for ideal voltage regulator.

(g) Using IC 78XX/79XX, draw voltage regulator circuit to provide 12V dc output voltage.

2. Attempt any THREE of the following : **12**

(a) Draw npn transistor in Common Base (CB) configuration. Name input, output voltages and currents with their directions. Write formula for current gain.

(b) Draw equivalent circuit and V-I characteristics of UJT.

(c) Draw circuit of common source FET amplifier. State function of each element.

(d) Draw drain characteristics of JFET and describe channel ohmic region and pinch-off region.

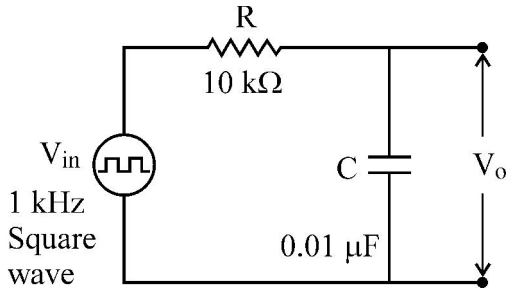
3. Attempt any THREE of the following : **12**

(a) Describe method to calculate current gain of transistor in CE configuration (β_{dc}, β_{ac}) with the help of output characteristics of transistor.

(b) Describe operating principle of E-MOSFET.

(c) Draw circuit of UJT relaxation oscillator. Draw waveforms at each terminal of UJT.

(d) Observe given integrator circuit. State whether it provides good integration or not. Give justification.



R = 10 kΩ C = 0.01 μF

Fig. 1

4. Attempt any THREE of the following : **12**

(a) Observe the given circuit. Write the state of LED when switch(s) is open and when switch(s) is closed. State the function of transistor in this circuit.

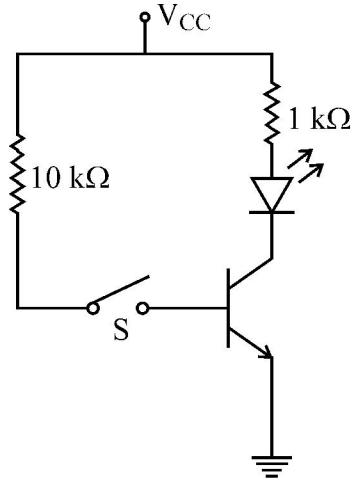


Fig. 2

(b) A JFET is to be used as an amplifier, in which operating region should be biased. Draw its biasing circuit and describe it.

(c) Draw frequency response of single stage CE amplifier. Write the steps to calculate bandwidth of CE amplifier.

(d) Suggest the multistage amplifier for audio signal amplification. Draw its circuit diagram.

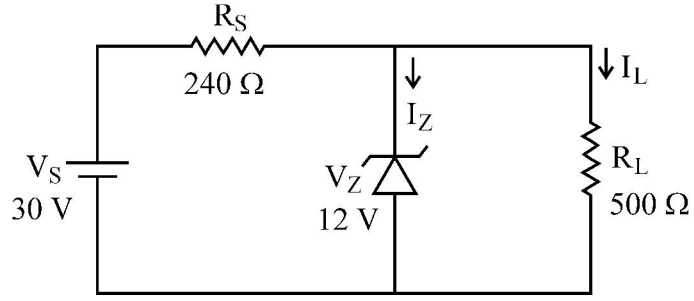
(e) For the given zener diode shunt regulator circuit. Calculate :

(i) The load voltage V_{RL}

(ii) Voltage drop across series resistance V_{RS}

(iii) Load current I_L

(iv) Zener current I_Z



$R_S = 240\ \Omega$ $V_2 = 12$ V

$V_S = 30$ V $R_L = 500\ \Omega$

Fig. 3

5. Attempt any TWO of the following : **12**

(a) Define thermal run-away of BJT. Draw voltage divider bias circuit and describe, how this bias circuit provides bias stability against temperature change.

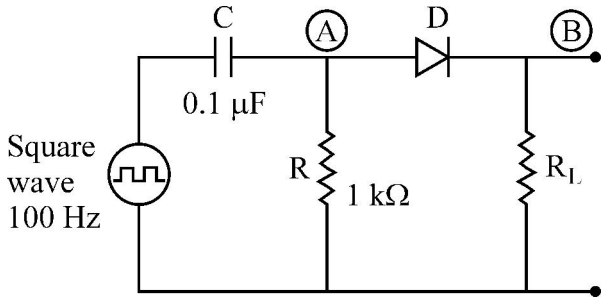
(b) Draw and describe operation of Class-B push-pull power amplifier. Define cross-over distortion. Draw input & output voltage waveforms showing cross-over distortion.

(c) Define clamper. Draw and describe negative clamper circuit. Draw input and output waveforms for sine wave input.

6. Attempt any TWO of the following : **12**

(a) Draw block diagram of voltage series and voltage shunt feedback connection. State their effect on parameters of amplifier.

(b) Observe the given circuit. A square wave input of 100 Hz frequency is applied to it. Draw input waveform, waveform at point A and waveform at point B. Name the circuit.



C = 0.1 μF

R = 1 kΩ

Fig. 4

(c) Draw transistorised series voltage regulator with error amplifier. Describe how the output voltage is regulated if there is a drop in input voltage because of some reason. State the draw-back of linear regulator.