22639

12425

3 Hours / 70 Marks Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory.*

(2) Illustrate your answers with neat sketches wherever necessary.

(3) Figures to the right indicate full marks.

(4) Assume suitable data, if necessary.

Marks

1. Attempt any FIVE of the following : **10**

(a) Draw NMOS transistor side-view structure with labels.

(b) List the logical operators in VHDL.

(c) Write the applications of Test bench.

(d) Write the meaning of product number XC35400 – 4PQG208C.

(e) State the concept of zero modeling.

(f) Draw the symbol and configuration/schematic diagram of Transmission Gate.

(g) List two examples of sequential and concurrent statements in VHDL.

2. Attempt any THREE of the following : **12**

(a) Draw the block diagram of CPLD. State the function of Logic or Function block. Write two names of Families of CPLD.

(b) Write the VHDL code for 4-bit adder without instantiation.

(c) Draw CMOS inverter (1) Circuit diagram (2) Cross section diagram (3) VTC characteristics (4) VTC characteristics with Good NMOS and bad PMOS.

(d) Write VHDL code for EXOR gate using (1) Behavioural modeling and (2) Data flow modeling.

3. Attempt any THREE of the following : **12**

(a) Explain the estimation process of resistance with layout diagram.

(b) Write the pro's and con's of VHDL.

(c) Draw the FPGA architecture and state the function of any four blocks.

(d) Write VHDL code for 4 : 1 mux.

4. Attempt any THREE of the following : **12**

(a) Compare FPGA, CPLD and ASIC on the basis of – (1) Performance (2) Memory (3) Power consumption (4) Security.

(b) Draw the circuit diagram of NAND gate using (1) NMOS and (2) CMOS logic.

(c) Draw the cross-section view of CMOS inverter with N-Well OR Twin-tub. State the advantages of Twin-tub process.

(d) Define the terms : (1) Noise margin (2) Fan-out (3) Metastability (4) Skew

(e) List the delays in VHDL simulation. Explain any one with statement and waveform.

5. Attempt any TWO of the following : **12**

(a) Design FSM circuit for sequence detector 1101 using D-flip-flop.

(b) Draw the stepwise diagram for N-well CMOS fabrication process.

(c) Write VHDL code for 3 : 8 decoder using case statement.

6. Attempt any TWO of the following : **12**

(a) Explain VLSI design flow for synthesis with neat sketch.

(b) (i) Draw the block diagram of Moore machine and Mealy machine FSM. Write the output expression.

(ii) Compare Moore machine and Mealy machine.

(c) (i) Write the function of (1) Library and (2) Entity

(ii) Explain different data types used in VHDL.
