22536

12425

03 Hours / 70 Marks Seat No. | | | | | | | | |

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. Attempt any FIVE of the following: **10**

a) Draw the circuit diagram of two bit comparator using IC7485.

b) Draw neat labelled block diagram of sequential circuit.

c) Compare combinational and sequential air units.

d) Define Hazards. State its types.

e) Draw excitation table for JK flip flop.

f) State the difference between FPGA and CPLD.

g) State the use of IC ADD 3501.

Marks

2. Attempt any THREE of the following: **12**

a) Solve the following using K-map F (A, B, C, D, E) = Σ (0, 2, 3, 4, 5, 6, 7, 11, 15, 16, 18, 19, 23, 27, 31)

b) Design 8 bit comparator using IC 7485.

c) Compare Mealy and Moore machine models.

d) Convert SR Flip Flop to JK Flip Flop.

3. Attempt any THREE of the following: **12**

a) Design 1:16 Demux using 1:4 Demux having active low enable input.

b) Draw an ASM chart and state table of a 2 bit up-down counter having mode control input.

c) Explain race around condition in asynchronous sequential circuit. Also state method to avoid it.

d) Draw and explain the architecture of CPLD.

4. Attempt any THREE of the following: **12**

a) Design JK flip flop using T Flip Flop.

b) Draw and explain the block diagram of asynchronous sequential air units.

c) Design Full adder using PLA.

d) Design D type Flip Flop using sequential logic PLA.

e) Explain the working of four decimal digit frequency counter.

Marks

5. Attempt any TWO of the following: **12**

a) Design a sequence generator for 101 sequence using moore model and implement using D - Flip Flop.

b) Implement the following Boolean functions using PLA.

F_1 (A, B, C) = Σ_m (1, 3, 5, 7)

F_2 (A, B, C) = Σ_m (0, 2, 4, 6)

c) Draw the internal diagram of ADD 3501 and design 3½ digit Digital Voltmeter using ADD 3501.

6. Attempt any TWO of the following: **12**

a) Draw and explain FPGA architecture block diagram.

b) Describe the instrument to measure time with block diagram. Consider the unknown input is 100 Hz square wave.

c) Draw and explain common Anode type seron segment display. Write the difference between common anode and common calkods display.