16117

3 Hours / 100 Marks

Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory*.

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

Marks

1. Attempt any TEN : **20**

(a) Convert (i) $(28.56)_{10} = (?)_2$ (ii) $(372)_8 = (?)_{10}$

(b) Draw logic diagram of tristate buffer with active low enable and active high enable.

(c) Draw truth table for logic gates represented by following IC's :

(i) IC7400

(ii) IC7402

(d) State triggering methods in digital circuits (any two)

(e) Identify SOP and POS equations :

(i) AB + CD

(ii) (A + B) (C + D)

(f) Differentiate between RAM & ROM (2 points)

(g) List any two non-weighted codes.

(h) Add the binary numbers (1011) & (1100)

(i) Find Y_1 & Y_2 for Fig. 1 & Fig. 2 respectively.

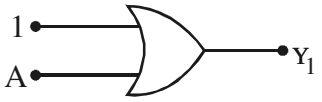

Fig. 1

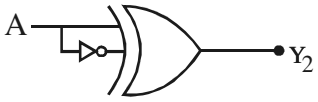

Fig. 2

(j) Define universal shift register.

(k) Draw symbol of TFF & write its truth table.

(l) Implement given logic equation using basic gates $Y = A\overline{B} + \overline{A}B$.

(m) Prove that $AB + A\overline{B} = A$, using laws of Boolean Algebra.

(n) Draw 3 variable K-map format.

2. Attempt any FOUR : **16**

(a) Subtract $(1101)_2$ from $(1110)_2$ using 1's & 2's complement method.

(b) Two square waves of 4 kHz & 8 kHz are applied as the inputs of AND gate & NAND gate. Draw the output waveform in each case.

(c) Design 1 : 32 De MUX using 1 : 8 De MUX.

(d) Write down excitation table of JK & DFF.

(e) Describe 3 bit R-2R ladder DAC with neat diagram.

(f) Compare Static RAM & Dynamic RAM (any 4 points)

3. Attempt any FOUR : **16**

(a) Perform the following operations :

(i) $(1001)_2 \times (1101)_2$

(ii) $(1001)_2 / (11)_2$

(b) Compare TTL, ECL & CMOS logic families (any 4 points)

(c) Realize following expression using MUX :

$f = \Sigma_m (0, 3, 5, 9, 11, 15)$

(d) Describe operation of PISO shift register with neat circuit diagram.

(e) Compare single slope ADC with dual slope ADC w.r.t.

(f) Draw organization of 4×4 memory and lable it.

4. Attempt any FOUR : **16**

(a) Perform BCD addition :

(i) $(45)_{10} + (33)_{10}$

(ii) $(57)_{10} + (26)_{10}$

(b) Define following characteristics of logic families :

(i) fan in

(ii) fan out

(iii) Propagation delay

(iv) Power dissipation

(c) Design 32 : 1 MUX using 16 : 1 MUX.

(d) Draw logic diagram for 3 bit up-down counter.

(e) Simplify given SOP equation using K map

$Y = \Sigma_m (0, 1, 2, 3, 5, 7, 8, 9, 11)$

(f) Write advantages (any 3) and disadvantage (any 1) of dual slope ADC.

5. Attempt any FOUR : **16**

(a) Define priority encoder. Draw the generalised block diagram of priority encoder.

(b) Compare R-2R ladder DAC with weighted resistor DAC (any 4 points)

(c) Explain the operation of TTL logic NAND gate. Draw the circuit diagram.

(d) Design MOD-6 counter using IC 7490.

(e) Compare combinational circuit with sequential circuit (any 4 points)

(f) Compare EPROM and EEPROM (any four points).

P.T.O.

6. Attempt any FOUR : **16**

(a) Implement Y = f (A, B, C) = Σ_m (0, 1, 2, 6, 7) using suitable DeMUX & logic gates.

(b) State the use of preset and clear terminal in a Flip-flop.

(c) Draw 3 bit synchronous up counter. Write its truth table.

(d) Draw 4 bit weighted resistor DAC and give expression for output voltage.

(e) Describe successive approximation ADC with neat diagram.

(f) Describe the operation of 1 dig it BCD adder using IC 7483.
