22639

23242

3 Hours / 70 Marks Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory.*

(2) Illustrate your answers with neat sketches wherever necessary.

(3) Figures to the right indicate full marks.

(4) Assume suitable data, if necessary.

(5) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. Attempt any FIVE of the following : **10**

(a) Define clock skew. State causes of clock skew (any **two**).

(b) State ways to reduce the metastability (any **four**).

(c) State the rules for using identifiers in VHDL (any **four**).

(d) Define test bench with the help of suitable example.

(e) Enlist two VHDL statements which are used to define sensitivity list.

(f) Define concept of Event Scheduling. State types of events involved in event scheduling.

(g) Draw NAND gate using CMOS.

2. Attempt any THREE of the following : **12**

(a) With the help of suitable diagram explain ASIC design flow.

(b) Write a VHDL program for BCD to seven segment converter using When-Else statement.

(c) Compare software description language and hardware description language.

(d) Differentiate between CMOS technology and BJT.

3. Attempt any THREE of the following : **12**

(a) Draw general architecture of FPGA. State function of each block in it.

(b) Write a short note on Architecture in VHDL program. Give one example of it.

(c) Explain various operators used in VHDL.

(d) Write VHDL program for 4 : 1 multiplexer using CASE statement.

4. Attempt any THREE of the following : **12**

(a) Differentiate between FPGA and CPLD.

(b) Explain delays in simulation with suitable example.

(c) Explain process of resistance estimation for CMOS.

(d) Explain nMOS fabrication process with the help of suitable diagram.

(e) Define following terms with respect to CMOS fabrication :

(i) Wafer Processing (ii) Oxidation

(iii) Ion implementation (iv) Diffusion

5. Attempt any TWO of the following : **12**

(a) Differentiate between Melay Machine and Moore Machine (any **six** points).

(b) Write a VHDL program for 2 : 4 decoder. Also write a test bench for it.

(c) Design following function using CMOS logic

$$Z = \overline{(A \cdot B + \overline{C} \cdot D) + E}$$

6. Attempt any TWO of the following : **12**

(a) Design sequence detector to detect sequence '1011' using 'D' flip-flop.

(b) Differentiate between signals, variable and constants in VHDL (any **four** points).

(c) Explain simulation cycle with the help of suitable diagram. State function of event queue and evaluation queue in it.