Embedded System

1. Which one of the following offers CPUs as integrated memory or peripheral interfaces?
a) Microcontroller
b) Microprocessor
c) Embedded system
d) Memory system

Answer: a

2. Which of the following offers external chips for memory and peripheral interface circuits?
a) Microcontroller
b) Microprocessor
c) Peripheral system
d) Embedded system

Answer: b

3. How many bits does an MC6800 family have?
a) 16
b) 32
c) 4
d) 8

Answer: d

4. Which of the following is a 4-bit architecture?
a) MC6800
b) 8086
c) 80386
d) National COP series

Answer: d

5. What is CISC?
a) Computing instruction set complex
b) Complex instruction set computing
c) Complimentary instruction set computing
d) Complex instruction set complementary

Answer: b

6. How is the protection and security for an embedded system made?
a) OTP
b) IPR
c) Memory disk security
d) Security chips

Answer: b

7. Which of the following possesses a CISC architecture?
a) MC68020
b) ARC
c) Atmel AVR
d) Blackfin

Answer: a

8. Which of the following is a RISC architecture?
a) 80286
b) MIPS
c) Zilog Z80
d) 80386

Answer: b

9. Which one of the following is board based system?
a) Data bus
b) Address bus
c) VMEbus
d) DMA bus

Answer: c

10. VME bus stands for
a) Versa module Europa bus
b) Versa module embedded bus
c) Vertical module embedded bus
d) Vertical module Europa bus

Answer: a

1. It retains its content when power is removed. What type of memory is this?
a) Volatile memory
b) Nonvolatile memory
c) RAM

d) SRAM

Answer: b

2. Name a volatile memory.
a) RAM
b) EPROM
c) ROM
d) EEPROM

Answer: a

3. Name a nonvolatile memory.
a) ROM
b) RAM
c) SRAM
d) DRAM

Answer: a

4. The initial routine is often referred to as
a) Initial program
b) Bootstrap program
c) Final program
d) Initial embedded program

Answer: b

5. What kind of socket does an external EPROM to plugged in for prototyping?
a) Piggyback

b) Single socket
c) Multi-socket
d) Piggyback reset socket

Answer: a

6. Which one of the following is UV erasable?
a) Flash memory
b) SRAM
c) EPROM
d) DRAM

Answer: c

7. What kind of memory does an OTP have?
a) SRAM
b) RAM
c) EPROM
d) DRAM

Answer: c

8. Which type of memory is suitable for low volume production of embedded systems?
a) ROM
b) Volatile
c) Non-volatile
d) RAM

Answer: c

9. Which is the single device capable of providing prototyping support for a range of microcontroller?
a) ROM
b) Umbrella device
c) OTP
d) RAM

Answer: b

10. What type of memory is suitable for high volume production?
a) RAM
b) ROM
c) EPROM
d) EEPROM

Answer: b

11. What type of memory is suitable for medium volume production?
a) Umbrella devices
b) OTP
c) ROM
d) RAM

Answer: b

12. How an embedded system communicate with the outside world?
a) Peripherals
b) Memory
c) Input

d) Output

Answer: a

13. How the input terminals are associated with external environments?
a) Actuators
b) Sensors
c) Inputs
d) Outputs

Answer: b

14. Which of the following are external pins whose logic state can be controlled by the processor to either be a logic zero or logic one is known as
a) Analogue value
b) Display values
c) Binary values
d) Time derived digital outputs

Answer: c

15. What kind of visual panel is used for seven segmented display?
a) LED
b) LCD
c) Binary output
d) Analogue output

Answer: b

1. Which one of the following is a microcontroller from Motorola?
a) MC68HC05
b) 4004
c) MIPS
d) 8080

Answer: a

2. Which is the first microcontroller?
a) 8051
b) Arm
c) TMS1000
d) Intel 4004

Answer: c

3. How many bits does MC68HC05 possess?
a) 4
b) 8
c) 16
d) 32

Answer: b

4. What is the bit size of the program counter in MC68HC05?
a) 7
b) 9
c) 13

d) 17

Answer: c

5. Which of the following microcontroller is used in engine management system?
a) MC68HC05
b) MC68HC11
c) Intel 80286
d) Intel 8086

Answer: b

6. Which is the concatenated register of MC68HC11?
a) D
b) X
c) IP
d) DI

Answer: a

7. What does CCR stand for?
a) Condition code register
b) Computing code register
c) Complex code register
d) Code control register

Answer: a

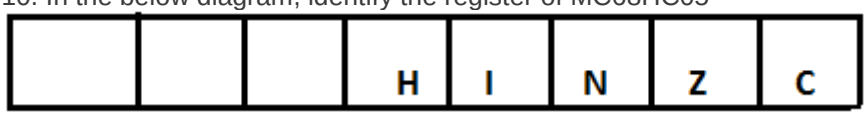
8. How many bytes of EPROM does MC68HC7054A possess?
a) 176 bytes

b) 240 bytes
c) 4144 bytes
d) 1024 bytes

Answer: c

9. Which of the following is an 8-bit command in MC68HC11?
a) Add
b) Shift
c) Multiply
d) Subtract
Answer: c

10. In the below diagram, identify the register of MC68HC05



a) CCR
b) PC
c) SP
d) IV

Answer: a

11. Which one of the following is an asynchronous communication channel?
a) SPI
b) MUDs
c) MOO

d) VOIP

Answer: a

1. Which of the following microprocessor is designed by Zilog?
a) Z80
b) Zigbee
c) 80386
d) 8087

Answer: a

2. Z80 is mainly based on
a) Intel 8080
b) MIPS
c) TIMS
d) 8051

Answer: a

3. Flag register of Z80 is also known as
a) Program status register
b) Program status address
c) Program status word
d) Program address register

Answer: c

4. What are the two register sets used in Z80?
a) C'D' and BC'
b) CD and BD
c) IV and MR
d) Main and alternate

Answer: d

5. How an alternate set of the register can be identified in Z80?
a) 'Suffix
b) 'Prefix
c) ,suffix
d) ,prefix

Answer: a

6. What is the purpose of memory refresh register of Z80?
a) To control on-chip DRAM
b) To control on-chip SRAM
c) To control ROM
d) To clear cache

Answer: a

7. What is the clock frequency of Z80?
a) 6 MHz
b) 8 MHz
c) 4 MHz

d) 2 MHz

Answer: c

8. Which are the two additional registers of Z80?
a) Interrupt and NMI
b) NMI and PSW
c) Interrupt vector and memory refresh
d) NMI and memory refresh

Answer: c

9. By which instruction does the switching of registers take place?
a) Instruction opcodes
b) AXX instruction
c) EXX instruction
d) Register instruction

Answer: c

10. Which of the following can be a paired set of 16-bit register?
a) CD
b) HL
c) AB
d) EH

Answer: b

11. Which signal is used to differentiates the access from a normal memory cycle?
a) HALT

b) RESET
c) MREQ
d) IORQ
Answer: d

12. What is done in mode1 of Z80?
a) Interrupt vector is supplied via the external bus
b) Interrupt vector is supplied via the peripherals
c) NMI gets started
d) Interrupt gets acknowledge from peripheral

Answer: a

13. What does m1 signal in Z80 describes?
a) I/O operation status
b) Memory refresh output
c) Output pulse on instruction fetch cycle
d) Interrupt request input

Answer: c

1. Which is the first device which started microprocessor revolution by Intel?
a) 8080
b) 8086
c) 8087
d) 8088
View Answer

Answer: a
Explanation: 8086 was released in 1978 and 8088 was released in 1979 .8087 is a numeric coprocessor which was released in 1977. Furthermore, 8080 is a device designed by Intel in 1974.

2. Which is the first microprocessor by Motorola?
a) MC6800
b) MC68001
c) MIPS
d) powerPC
View Answer
Answer: a
Explanation: MC6800 is the first microprocessor by Motorola which started a revolution to the embedded systems.

3. Motorola MC6800 is a how many it processor?
a) 4
b) 8
c) 16
d) 32
View Answer
Answer: b
Explanation: MC6800 is an 8-bit processor and having two 8 bit accumulator registers.

4. How many accumulators does an MC6800 have?
a) 1
b) 2
c) 3
d) 4
View Answer
Answer: b
Explanation: MC6800 is having 2 accumulators both comprising of 8 bits.

5. How many bits does an accumulator of MC6800 have?
a) 8
b) 16
c) 32
d) 4
View Answer
Answer: a
Explanation: MC6800 possess 8-bit accumulator register since it is an 8-bit processor.

6. What is the performance of an accumulator?
a) Storing data and performing logical operation
b) Storing data and performing arithmetic operation
c) Storing address
d) Pointer
View Answer
Answer: b
Explanation: Accumulator is used for all the arithmetic operation such as addition, subtraction, multiplication, relational, logical etc. It is also used for storage.

7. Which of the following is the area of memory that is used for storage?
a) Register
b) Stack
c) Accumulator
d) Memory
View Answer
Answer: b
Explanation: Stack can be used at the time of function call or it is a short time large scale storage of data. Therefore, stack is the area within memory for storage.

8. How a stack is accessed?
a) Stack pointer
b) Stack address
c) Stack bus
d) Stack register
View Answer
Answer: a
Explanation: Stack pointer is a special register that indexes into the stack.
9. PUSH-POP mechanism is seen in _____
a) Stack pointer
b) Register
c) Memory
d) Index register
View Answer
Answer: a
Explanation: Stack pointer is used to store data like subroutine calls in which a push-pop mechanism is followed. Data is pushed into the stack to store it and popped off to retrieve it.

10. 8 bits equals _____
a) 128 bytes
b) 64 bytes
c) 256 bytes
d) 32 bytes
View Answer
Answer: c
Explanation:2^8 = 256 by which bytes are calculated.

11. What is the address range in 80286?
a) 1 Mbytes
b) 2 Mbytes

c) 16 Mbytes
d) 32 mbytes
View Answer
Answer: c
Explanation: 80286 is a 16 bit processor. So it has an address range of 16 Mbytes.

12. Which is the first 32 bit member of Intel?
a) 8086
b) 8088
c) 80286
d) 80386
View Answer
Answer: d
Explanation: The new generation of Intel starts with 80386 which have 32 bit registers.

13. What supports multitasking in 80386?
a) Read mode
b) External paging memory management unit
c) Paging and segmentation
d) On-chip paging memory management unit
View Answer
Answer: d

1. Which one of the following is the successor of 8086 and 8088 processor?
a) 80286

b) 80387
c) 8051
d) 8087
View Answer
Answer: a
Explanation: 80286 is the successor of 8086 and 8088 because it possess a CPU based on 8086 and 8088. 8051 is a microcontroller designed by Intel which is commonly known as Intel MCS-51. 8087 is the first floating point coprocessor of 8086.

2. Which is the processor behind the IBM PC AT?
a) 80387
b) 8088
c) 80286
d) 8086
View Answer
Answer: c

Explanation: The processor was successful in the PC market and it was a successful processor behind the IBM.

3. Which are the two modes of 80286?
a) Real mode and protected mode
b) Mode1 and mode2
c) Alternate and main
d) Mode A and mode B
View Answer
Answer: a
Explanation: It possess two modes which are called real and protected modes. In real modes it adds some additional register in order to access a size greater than 16MB but still preserving its compatibility with 8086 and 8088.

4. Which register set of 80286 form the same register set of 8086 processor?
a) AH,AL
b) BX
c) BX,AX
d) EL
View Answer
Answer: a
Explanation: The 16 bit register of 80286 can also act as 8 bit register by splitting into a higher register and lower register.

5. Which are the 4 general purposes 16 bit register in Intel 80286?
a) CS,DS,SS,ES
b) AX,BX,CX,DX
c) IP,FL,DI,SI
d) DI,SI,BP,SP
View Answer
Answer: b
Explanation: Intel 80286 possess 4 general purpose registers and these are 16-bit in size. In addition to the general purpose register, there are four segmented registers, two index registers and a base pointer register.
6. Which are the 4 segmented registers in intel 80286?
a) AX,BX,CX,DX
b) AS,BS,CS,DS
c) SP,DI,SI,BP
d) IP,FL,SI,DI
View Answer
Answer: b
Explanation: Intel 80286 possess 4 general purpose registers, 4 segmented registers, 2 index register and a base pointer register.

7. How is expanded memory accessed in 80286?
a) Paging

b) Interleaving
c) RAM
d) External storage
View Answer
Answer: a
Explanation: The 80286 processor can access beyond 1MB by paging and special hardware to stimulate the missing address lines. This is called expanded memory.

8. When is the register set gets expanded in 80286?
a) In real mode
b) In expanded mode
c) In protected mode
d) Interrupt mode
View Answer
Answer: c
Explanation: In protected mode, two additional register arises which is called index register and base pointer register which helps in expanding the register.

9. Which are the two register available in the protected mode of 80286?
a) General and segmented
b) General and pointer
c) Index and base pointer
d) Index and segmented
View Answer
Answer: c
Explanation: In the protected mode of 80286, two additional register arises which is called index register and base pointer register.

10. What kind of support does 80286 access in protected mode?
a) Real mode

b) Address access
c) Data access
d) Virtual memory
View Answer
Answer: d
Explanation: In the protected mode of 80286, two additional register arises which is called index register and base pointer register. This allows the 80286 to support virtual memory scheme.

11. Which of the following processor possess memory management?
a) 8086
b) 8088
c) 80286
d) 8051
View Answer
Answer: c
Explanation: Because of the efficient paging mechanism, 80286 is one of the processors which allows the memory management unit. 8086 and 8088 does not allow paging mechanism. 8051 is a microcontroller which have an in-built memory and does not possess a paging mechanism.

12. What is the size of the address bus in 80286?
a) 20
b) 24
c) 16
d) 32
View Answer
Answer: b
Explanation: The size of the address bus in 80286 is 24 bits and 20 bits in 8088 and 8086.

13. Which is the interrupt vector in 80286 which functions for stack fault?
a) 11
b) 12
c) 14
d) 16
View Answer
Answer: b
Explanation: 12 is the interrupt vector indicating stack fault. It will be different for a different microprocessor.

14. Which is the interrupt vector that functions as invalid opcode?
a) 9
b) 8
c) 7
d) 6
View Answer
Answer: d
Explanation: 6 is the interrupt vector indicating invalid opcode. It will be different for a different microprocessor.

15. Which of the following possess the same set of instructions?
a) 8088 and 80286
b) 8086 and 80286
c) 8051 and 8088
d) 8051 and 8086
View Answer
Answer: b

1. Which of the following is a coprocessor of 80386?
a) 80387
b) 8087
c) 8089
d) 8088
View Answer
Answer: a
Explanation: 80386 have 80387 as a floating point arithmetic coprocessor which can perform various floating point calculations.

2. Name the processor which helps in floating point calculations.
a) microprocessor
b) microcontroller
c) coprocessor
d) controller
View Answer
Answer: c
Explanation: The coprocessor can perform signal processing, floating point arithmetics, encryption etc.

3. Which is the coprocessor of 8086?
a) 8087
b) 8088
c) 8086
d) 8080
View Answer
Answer: a
Explanation: 8087 is the coprocessor for both 8086 and 8088. 8089 is also a coprocessor of 8086 and 80888.

4. Which of the following is a coprocessor of Motorola 68000 family?
a) 68001
b) 68011
c) 68881
d) 68010
View Answer
Answer: c
Explanation: The 68881 coprocessor of Motorola provides floating point arithmetics.

5. Which of the following processors can perform exponential, logarithmic and trigonometric functions?
a) 8086
b) 8087
c) 8080
d) 8088
View Answer
Answer: b
Explanation: 8087 is a coprocessor which can perform all the mathematical functions including addition, subtraction, multiplication, division, exponential, logarithmic, trigonometric etc. 8086, 8080 and 8088 are microprocessors which require the help of a coprocessor for floating point arithmetic.

6. How many stack register does an 8087 have?
a) 4
b) 8
c) 16
d) 32
View Answer

Answer: b
Explanation: The 8087 coprocessor does not have a main register set but they have an 8-level deep stack register from st0 to st7.

7. Which of the following processor can handle infinity values?
a) 8080
b) 8086
c) 8087
d) 8088
View Answer
Answer: c
Explanation: 8087 is a coprocessor which can handle infinity values with two types of closure known as affine closure and projective closure.

8. Which coprocessor supports affine closure?
a) 80187
b) 80287
c) 80387
d) 8088
View Answer
Answer: b
Explanation: 80287 uses an affine closure for infinity values whereas 80387 and 80187 support projective closure for infinity values.

9. Which one is the floating point coprocessor of 80286?
a) 8087
b) 80187

c) 80287
d) 80387
View Answer
Answer: c
Explanation: 80286 supports 80287 as its floating point coprocessor which helps in floating point calculations.

10. How many pins does 8087 have?
a) 40 pin DIP
b) 20 pin DIP
c) 40 pins
d) 20 pins
View Answer
Answer: a
Explanation: All 8087 models have a 40 pin DIP which is operated in 5V.
11. What is the clock frequency of 8087?
a) 10 MHz
b) 5 MHz
c) 6 MHz
d) 4 MHz
View Answer
Answer: b
Explanation: 8087 have 5 MHz as its clock frequency because the coprocessor must have the same clock frequency as that of the main processor.

12. How are negative numbers stored in a coprocessor?
a) 1’s complement
b) 2’s complement
c) decimal

d) gray
View Answer
Answer: b
Explanation: In a coprocessor, negative numbers are stored in 2’s complement with its leftmost sign bit of 1 whereas positive numbers are stored in the form of true value with its leftmost sign bit of 0.

13. How many bits are used for storing signed integers?
a) 2
b) 4
c) 8
d) 16
View Answer
Answer: d
Explanation: Signed integers in a coprocessor are stored as a 16-bit word, 32-bit double word or 64-bit quadword.

14. Which of the processor has an internal coprocessor?
a) 8087
b) 80287
c) 80387
d) 80486DX
View Answer
Answer: d
Explanation: 8087 is an external IC designed to operate with the 8088/8086 processor but 80486DX is an on-chip coprocessor that is, it does not require an extra integrated chip for floating point arithmetics.

15. What are the two major sections in a coprocessor?
a) control unit and numeric control unit
b) integer unit and control unit

c) floating point unit and coprocessor unit
d) coprocessor unit and numeric control unit
View Answer
Answer: a

1. What are the three stages included in pipelining of 80386?
a) Fetch, decode, execute
b) Fetch, execute, decode
c) Execute, fetch, decode
d) Decode, execute, fetch
View Answer
Answer: a
Explanation: The instruction can execute in a single cycle which is done by pipelining the instruction flow. The address calculations are performed as the instruction proceeds down the line. Pipelining may take several cycles, an instruction can potentially be started and completed on every clock edge, thus achieving the single cycle performance.

2. How instructions and data are accessed to pipeline stages of 80486 processor?
a) Through internal unified cache
b) Through external unified cache
c) Through external cache
d) Through multiple caches
View Answer
Answer: a
Explanation: In order to have instruction and data to the pipeline, the 80486 has an internal unified cache to contain both data and instructions. This helps in the independency of the processor on external memory.

3. Which of the following processor possesses a similar instruction of 80486?
a) 8086

b) 80286
c) 80386
d) 8080
View Answer
Answer: c
Explanation: The instruction set is same as that of 80386 but there are some additional instructions available when the processor is in protected mode.

4. What are the two external interrupt signals in 80386?
a) IV and NMI
b) NMI and INTR
c) INTR and IV
d) PC and NMI
View Answer
Answer: b
Explanation: The 80386 has two external interrupt signals which allow external devices to interrupt the processor. The INTR input creates a maskable interrupt while the NMI creates a non-maskable interrupt.

5. How many bit vector number is used in an interrupt cycle of 80386?
a) 4
b) 8
c) 16
d) 32
View Answer
Answer: b
Explanation: While an interrupt cycle is running, the processor possesses two interrupts to acknowledge bus cycles and reads an 8-bit vector number. This vector is then used to locate, within the vector table and it has the address of the corresponding interrupt service routine. NMI is automatically assigned as vector number 2.

6. In how many modes does 80386 can run?
a) 2
b) 4
c) 3
d) 5
View Answer
Answer: c
Explanation: The 80386 can run in three different modes: the real mode, the protected mode, and a virtual mode. In real mode, the size of each segment is limited to 64 Kbytes and in protected mode, the largest segment size is increased to 4 Gbytes and the virtual mode is a special version of the protected mode.

7. How many bit flag register does 80386 have?
a) 8
b) 16
c) 32
d) 64
View Answer
Answer: c
Explanation: The 32-bit flag register possesses the normal carry zero, auxiliary carry, parity, sign and overflow flags.
8. Which processor is the derivative of 80386DX?
a) 80387
b) 80386SX
c) 80386 DDX
d) 8087
View Answer
Answer: b
Explanation: Derivative of the 80386DX called the 80386SX which provides the same architecture and lowers cost. To minimal the cost value, it uses an external 16-bit data bus and a 24-bit memory bus.

9. Which of the following is a portable device of Intel?
a) 80386DX
b) 8087
c) 80386SL
d) 80386SX
View Answer
Answer: c
Explanation: Intel has 80386SL as the portable PCs which helps in controlling power and increases the power efficiency of the processor.

10. Which of the processor has a 5 stage pipeline?
a) 80386
b) 80486
c) 80286
d) 80386DX
View Answer
Answer: b
Explanation: 80486 have a five stage pipeline ALU. These include fetch, decode, execute, memory access and write back. This helps in accessing instruction faster and thus makes the processor faster. 80386DX have a three-stage pipelining which only includes fetch, decode and execute.

11. Which of the following processor can execute two instructions per cycle?
a) 80486
b) 80386DX
c) Intel Pentium

d) 80386
View Answer
Answer: c
Explanation: Intel Pentium have many advanced features one of which is, it can execute two instructions per cycle thus improving the speed of the processor whereas 80486, 80386 and 80386DX does not have this feature.

12. Which of the following processors have two five-stage pipelines?
a) 80486
b) 80386
c) Intel Pentium
d) 80386DX
View Answer
Answer: c
Explanation: The intel Pentium possess two five-stage pipelines which allow the execution of two integer instruction jointly.

13. In which processor does the control register and system management mode register first appeared?
a) 80386
b) 80386SL
c) 80386DX
d) 80486
View Answer
Answer: b
Explanation: The control register and system management mode register has first appeared in 80386SL and later on succeeded by other processors. These registers can provide intelligent power control.

14. Which is the next successor of Intel Pentium?
a) Pentium pro

b) P1
c) P2
d) P5
View Answer
Answer: a
Explanation: Intel Pentium is succeeded by Pentium pro. P1, P2, and P5 are the other processors of Intel.

15. Which of the following processor allows a multiple branch prediction?
a) 80386
b) P1
c) Intel Pentium
d) Intel Pentium pro
View Answer
Answer: d

1. Which are the processors based on RISC?
a) SPARC
b) 80386
c) MC68030
d) MC68020
View Answer
Answer: a
Explanation: SPARC and MIPS processors are the first generation processors of RISC architecture.

2. What is 80/20 rule?
a) 80% instruction is generated and 20% instruction is executed
b) 80% instruction is executed and 20% instruction is generated
c) 80%instruction is executed and 20% instruction is not executed
d) 80% instruction is generated and 20% instructions are not generated
View Answer
Answer: a
Explanation: 80% of instructions are generated and only 20% of the instruction set is executed that is, by simplifying the instructions, the performance of the processor can be increased which lead to the formation of RISC that is reduced instruction set computing.

3. Which of the architecture is more complex?
a) SPARC
b) MC68030
c) MC68030
d) 8086
View Answer
Answer: a
Explanation: SPARC have RISC architecture which has a simple instruction set but MC68020, MC68030, 8086 have CISC architecture which is more complex than CISC.

4. Which is the first company who defined RISC architecture?
a) Intel
b) IBM
c) Motorola
d) MIPS
View Answer
Answer: b
Explanation: In 1970s IBM identified RISC architecture.

5. Which of the following processors execute its instruction in a single cycle?
a) 8086
b) 8088
c) 8087
d) MIPS R2000
View Answer
Answer: d
Explanation: MIPS R2000 possess RISC architecture in which the processor executes its instruction in a single clock cycle and also synthesize complex operations from the same reduced instruction set.

6. How is memory accessed in RISC architecture?
a) load and store instruction
b) opcode instruction
c) memory instruction
d) bus instruction
View Answer
Answer: a
Explanation: The data of memory address is loaded into a register and manipulated, its contents are written out to the main memory.

7. Which of the following has a Harvard architecture?
a) EDSAC
b) SSEM
c) PIC
d) CSIRAC
View Answer

Answer: c
Explanation: PIC follows Harvard architecture in which the external bus architecture consist of separate buses for instruction and data whereas SSEM, EDSAC, CSIRAC are stored program architecture.

8. Which of the following statements are true for von Neumann architecture?
a) shared bus between the program memory and data memory
b) separate bus between the program memory and data memory
c) external bus for program memory and data memory
d) external bus for data memory only
View Answer
Answer: a
Explanation: von Neumann architecture shares bus between program memory and data memory whereas Harvard architecture have a separate bus for program memory and data memory.

9. What is CAM stands for?
a) content-addressable memory
b) complex addressable memory
c) computing addressable memory
d) concurrently addressable memory
View Answer
Answer: a
Explanation: Non-von Neumann architecture is based on content-addressable memory.
10. Which of the following processors uses Harvard architecture?
a) TEXAS TMS320
b) 80386
c) 80286
d) 8086
View Answer

Answer: a
Explanation: It is a digital signal processor which have small and highly optimized audio or video processing signals. It possesses multiple parallel data bus.

11. Which company further developed the study of RISC architecture?
a) Intel
b) Motorola
c) university of Berkeley
d) MIPS
View Answer
Answer: c
Explanation: The University of Berkeley and Stanford university provides the basic architecture model of RISC.

12. Princeton architecture is also known as
a) von Neumann architecture
b) Harvard
c) RISC
d) CISC
View Answer
Answer: a
Explanation: The von Neumann architecture is also known as von Neumann model or Princeton architecture.

13. Who coined the term RISC?
a) David Patterson
b) von Neumann
c) Michael J Flynn

d) Harvard
View Answer
Answer: a
Explanation: David Patterson of Berkeley university coined the term RISC whereas Michael J Flynn who first views RISC.

14. Which of the following is an 8-bit RISC Harvard architecture?
a) AVR
b) Zilog80
c) 8051
d) Motorola 6800
View Answer
Answer: a
Explanation: AVR is an 8-bit RISC architecture developed by Atmel. Zilog80, 8051, Motorola 6800 are having CISC architectures.
15. Which of the following processors has CISC architecture?
a) AVR
b) Atmel
c) Blackfin
d) Zilog Z80
View Answer
Answer: d

1. What are the factors of filters which are determined by the speed of the operation in a digital signal processor?
a) attenuation constant
b) frequency
c) bandwidth

d) phase
View Answer
Answer: c
Explanation: The bandwidth of any filter depends on the speed of operations held in a digital signal processor.

2. How many tables does an FIR function of a digital signal processor possess?
a) 1
b) 2
c) 3
d) 4
View Answer
Answer: b
Explanation: Digital signal processor function involves setting up of two tables and one is for sampled data and the other table is for filter coefficients which determine the filter response. It takes values from the table and performs programs.

3. Why is said that branch prediction is not applicable in a digital signal processor?
a) low bandwidth
b) high bandwidth
c) low frequency
d) high frequency
View Answer
Answer: a
Explanation: Loop control timing varies depending on the branch predictions which in turn make bandwidth predictions difficult thereby lowering the bandwidth of the digital signal processor.

4. Which architecture can one overcome the low bandwidth issue in MC6800 family?
a) RISC

b) CISC
c) von Neumann
d) program stored
View Answer
Answer: a
Explanation: RISC architecture can offer some improvement in the low bandwidth issue since it has the ability to perform operations in a single cycle.

5. Which architecture in digital signal processor reduces the execution time?
a) Harvard
b) CISC
c) program storage
d) von Neumann
View Answer
Answer: a
Explanation: Harvard architecture in a digital signal processor allows continuous data fetching and performing the corresponding instructions.

6. Which of the following processors also can work as a digital signal processor?
a) 8086
b) 8088
c) 8080
d) ARM9E
View Answer
Answer: d
Explanation: ARM9E can also have DSP level of performance without having a digital signal processor by its enhanced DSP instructions.

7. What types of modules are used in the digital signal processor to form the loop structure?
a) modulo-timer
b) modulo-counter
c) timer
d) external timer
View Answer
Answer: b
Explanation: By using hardware multipliers, counters etc the entire hardware can be redesigned to perform some specific functions which are used in digital signal processors. One such is the modulo-counter to form the loop structure.

8. Name a processor which is used in digital audio appliances.
a) 8086
b) Motorola DSP56000
c) 80486
d) 8087
View Answer
Answer: b
Explanation: Motorola DSP56000 is a powerful digital signal processor which is used in digital audio applications which have the capability of noise reduction and multi-band graphics whereas 8087 is a coprocessor and 80486 and 8086 are microprocessors.

9. How many bits does DSP56000 processor have?
a) 8
b) 16
c) 24
d) 32
View Answer
Answer: c
Explanation: In order to increase the resolution, DSP56000 is a 24-bit data word processor.

10. How many buses did DSP56000 possess?
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: b
Explanation: It possess three separate external buses, one is for the program and the remaining two buses are for X and Y memories for data.

11. Which of the following architecture does DSP56000 possess?
a) Harvard
b) von Neumann
c) CISC
d) program-stored
View Answer
Answer: a
Explanation: DSP56000 possess Harvard architecture since this architecture has a separate bus for program memory and data memory.
12. What does AAU stand for?
a) arithmetic address unit
b) address arithmetic unit
c) address access unit
d) arithmetic access unit
View Answer
Answer: b
Explanation: DSP56000 possess two external bus switches in which one is for data and the other is for the address for communicating with the outside world and these two switches are reproduced by the internal data bus and AAU.

13. How many address register does the AAU of a DSP56000 have?
a) 8
b) 16
c) 24
d) 32
View Answer
Answer: c
Explanation: AAU have 24 address registers in three banks of eight.

14. How many registers does a DSP56000 have?
a) 4
b) 5
c) 7
d) 6
View Answer
Answer: c
Explanation: DSP56000 has six 24-bit registers for controlling the loop counts, operating mode, stack manipulation and condition codes.

15. Which of the following bits are used for sign extension in DSP56000?
a) upper 8 bits of the stack pointer
b) lower 8 bits of the stack pointer
c) lower 8 bits of the program counter
d) upper 8 bits of the program counter
View Answer
Answer: d

1. How many bit register set does RISC 1 model used?
a) 138*24
b) 138*32
c) 69*16
d) 69*32
View Answer
Answer: b
Explanation: RISC 1 model is developed in the 1970s and uses a large register set of 138*32 bit. These are arranged in eight overlapping windows which have 24 registers each and these windows are split so that six registers can be used during function calls.

2. Which of the following processor commercializes the Berkeley RISC model?
a) SPARC
b) Stanford
c) RISC-1
d) RISC
View Answer
Answer: a
Explanation: The Berkeley RISC design was developed between the year 1980 and 1984 and later on the RISC design were commercialized as SPARC processor.

3. How many transistors does RISC 1 possess?
a) 44000
b) 45000
c) 44500

d) 45500
View Answer
Answer: c
Explanation: The final design of the RISC concept is called the RISC 1 which was published by ACM ISCA. It possesses 44500 transistors which can implement 31 instruction.

4. How many registers does RISC 1 model have?
a) 68
b) 58
c) 78
d) 88
View Answer
Answer: c
Explanation: The RISC 1 model have 78 registers of size 32 bits.

5. Which of the architectures are made to speed up the processor?
a) CISC
b) RISC
c) program stored
d) von Neumann
View Answer
Answer: b
Explanation: RISC architecture is made for speeding up the processor with limited execution time whereas CISC architecture is mainly for code efficiency.

6. How did 8086 pass its control to 8087?
a) BUSY instruction
b) ESCAPE instruction

c) CONTROL instruction
d) fetch 8087
View Answer
Answer: b
Explanation: When 8086 comes across any floating point arithmetic operations, it executes ESCAPE instruction code in order to pass the control of bus and instruction op-code to 8087.

7. Which of the following processor supports MMX instructions?
a) 8080
b) 80486
c) Intel Pentium
d) 80386
View Answer
Answer: c
Explanation: MMX instructions or multimedia extensions were introduced in Pentium processors to provide support for multimedia software running on a PC.

8. Which of the following processors has a speculative execution?
a) 80486
b) P1
c) Intel Pentium
d) Pentium pro
View Answer
Answer: d
Explanation: Speculative execution is executed speculatively that is, following the predicted branch paths in the code until the true path is determined. If the processor executes correctly, then the performance is gained, if not, the results are discarded and the processor continues to execute until the correct path is identified.

9. How many bit accumulator does DSP56000 have?
a) 28
b) 56
c) 112
d) 14
View Answer
Answer: b
Explanation: The ALU of DSP56000 have two 56-bit accumulator A and B each of which have a small register with it.

10. How many additional registers does DSP56000 have?
a) 2
b) 4
c) 6
d) 8
View Answer
Answer: b
Explanation: In addition to the six registers of DSP56000, it has four 24-bit registers X1, X0, Y1, Y0 which can be concatenated to form 48 bit register X and Y.

11. What does MAC instruction of DSP56000 stand for?
a) multiply accumulator
b) multiple access
c) multiple accounting
d) multiply accumulator counter
View Answer
Answer: a

1. What does SPARC stand for?
a) scalable processor architecture
b) speculating architecture
c) speculating processor
d) scaling Pentium architecture
View Answer
Answer: a
Explanation: SPARC was designed for optimizing compilers and easily pipelined hardware implementations and it can license by anyone that is, having a nonproprietary architecture which is used to develop various microprocessors.

2. How many bits does SPARC have?
a) 8
b) 16
c) 32
d) 64
View Answer
Answer: c
Explanation: It is a 32 bit RISC architecture having 32-bit wide register bank.

3. Which company developed SPARC?
a) intel
b) IBM
c) Motorola
d) sun microsystem
View Answer
Answer: d
Explanation: SPARC is developed by Sun Microsystem but different manufacturers from other companies like Intel, Texas worked on it.

4. What improves the context switching and parameter passing?
a) register windowing
b) large register
c) stack register
d) program counter
View Answer
Answer: a
Explanation: SPARC follows Berkeley architecture model and uses register windowing in order to improve the context switching and parameter passing. It also supports superscalar operations.

5. How many external interrupts does SPARC processor support?
a) 5
b) 10
c) 15
d) 20
View Answer
Answer: c
Explanation: SPARC processor provides 15 external interrupts which are generated by the interrupt lines IRL0-IRL3.

6. Which level is an in-built nonmaskable interrupt in SPARC processor?
a) 15
b) 14
c) 13
d) 12
View Answer
Answer: a
Explanation: The level 15 of the SPARC processor is assigned to be a nonmaskable interrupt and the remaining 14 levels are unmasked and if necessary they can be made maskable.

7. How many instructions does SPARC processor have?
a) 16
b) 32
c) 64
d) 128
View Answer
Answer: c
Explanation: The instruction set of SPARC processor have 64 instructions which can be accessed by load and store operation with a RISC architecture.

8. What is generated by an external interrupt in SPARC?
a) internal trap
b) external trap
c) memory trap
d) interfaced trap
View Answer
Answer: a
Explanation: In SPARC when an external interrupt is generated, an internal trap is created in the trap base register in which the current and next instructions are saved, the pipeline gets flushed and the processor turns into a supervisor mode.

9. When an external interrupt is generated, what type of mode does the processor supports?
a) real mode
b) virtual mode
c) protected mode
d) supervisor mode
View Answer

Answer: d
Explanation: In SPARC when an external interrupt is called, it creates an internal trap in which the current and next instructions get saved and mode of the processor switches to supervisor mode.
10. Where is trap vector table located in SPARC processor?
a) program counter
b) Y register
c) status register
d) trap base register
View Answer
Answer: d
Explanation: The trap vector table is located in the trap base register which supplies the address of the service routine. When it is completed REIT instructions are executed.

11. How many bits does SPARC-V9 processor have?
a) 16
b) 32
c) 64
d) 128
View Answer
Answer: c
Explanation: There are three major versions of SPARC which are SPARC-V7, SPARC-V8 and SPARC-V9. The former two are 32 bits processor and the later is a 64-bit processor.
12. What are the three modules in the SPARC processor?
a) IU, FPU, CU
b) SP, DI, SI
c) AX, BX, CX
d) CU, CH, CL
View Answer

Answer: a
Explanation: The SPARC processor has three modules which are Integer unit, Floating point unit, and coprocessor unit. Each module has its own functions and integer unit controls the overall operation of the processor.

13. How many floating point register does the FPU of the SPARC have?
a) 16 128-bit
b) 32 128-bit
c) 64 128-bit
d) 10 128-bit
View Answer
Answer: a
Explanation: It possesses 32 32-bit single precision, 32 64-bit double precision and 16 128-bit quads precise floating registers.

14. Which module of SPARC contains the general purpose registers?
a) IU
b) FPU
c) CU
d) control unit
View Answer
Answer: a

1. What shows the brightness of the pixel in a digital signal processor?
a) luminance
b) transparent
c) chrominance
d) opaque
View Answer

Answer: a
Explanation: The color image of a digital signal processor have multiple channels. The brightness of the pixel is determined by luminance and the color of the pixel is determined by chrominance.

2. What is the color format of chrominance in a digital signal processor?
a) VGBA
b) VIBGYOR
c) White
d) RGBA
View Answer
Answer: d
Explanation: RGBA colors have four channels red, green, blue, and alpha, which is transparent.

3. Which of the following processor are designed to perform calculations in graphics rendering?
a) GPU
b) digital signal processor
c) microprocessor
d) microcontroller
View Answer
Answer: a
Explanation: Graphics processing unit is designed to perform calculations in graphics rendering. Intel, NVIDIA, and AMD are dominant providers of GPU.

4. Which of the processor is a good match for applications such as video games?
a) GPU
b) VLIW
c) Coprocessor
d) Microcontroller
View Answer

Answer: a
Explanation: GPU is a graphics processing unit. Therefore, more graphical images can be created by GPU which is necessary for video games. Therefore, GPU is a good match for video games.

5. Which of the following statement is true for concurrency?
a) different parts of the program executes physically
b) different parts of the program executes sequentially
c) different parts of the program executes conceptually
d) different parts of the program executes sequentially and physically
View Answer
Answer: c
Explanation: A concurrent program executes different parts of the program conceptually, a parallel program executes different programs physically and a non-concurrent program executes the program in sequential order.

6. Which is an imperative language?
a) C program
b) SQL
c) XQuery
d) Concurrent model of HDL
View Answer
Answer: a
Explanation: Imperative language is one which executes the program in sequential order. C program is an example of imperative language, SQL and XQuery are examples of declarative languages or non-imperative language. Concurrent model in HDL is a hardware description language which executes the program concurrently.

7. Which of the following instructions supports parallel execution?
a) VLIW
b) TTA
c) ALU operation

d) Test-and-set instructions
View Answer
Answer: a
Explanation: VLIW is a very long instruction word which receives many instructions and is executed in one instructed word. VLIW is majorly designed for instruction-level parallel (ILP) that is, it can execute codes concurrently or parallel in some time. TTA is a transport triggered architecture which is a type of CPU design which programs controlling the internal buses of the processor. Test-and-set is used to write to a memory location and return its old values. ALU used to perform arithmetic and logic operations.

8. Who invented VLIW architecture?
a) Josh Fisher
b) John Ellis
c) John Ruttenberg
d) John O'Donnell
View Answer
Answer: a
Explanation: Josh Fisher from Yale Universities invented the concept of VLIW architecture. John Ellis described the VLIW compiler. John Ruttenberg develops some important algorithms in scheduling.

9. What is ILP?
a) instruction-level parallelism
b) instruction-level panel
c) instruction-language panel
d) inter-language parallelism
View Answer
Answer: a
Explanation: A processor which supports instruction-level parallelism can perform multiple independent operations in every instruction cycle. Basically, there are four types of instructions. These are CISC instructions, subword parallelism, superscalar, and VLIW.

10. Which ILP supports the ALU division?
a) Subword parallelism
b) CISC
c) Superscalar
d) VLIW
View Answer
Answer: a
Explanation: In subword parallelism, the wide ALU is divided into smaller slices which enable simultaneous arithmetic and logical operations.

11. Which is a vector processor?
a) Subword parallelism
b) CISC
c) Superscalar
d) VLIW
View Answer
Answer: a
Explanation: Subword parallelism is a form of a vector processing. A vector processor is the one whose instruction set includes operations on multiple data elements simultaneously.

12. Which of the following architecture supports out-of-order execution?
a) RISC
b) CISC
c) Superscalar
d) Subword parallelism
View Answer
Answer: c
Explanation: Superscalar architecture support out-of-order execution in which the instructions later in the stream are executed before earlier instructions.

13. Which is an example of superscalar architecture?
a) Pentium 4
b) 8086
c) 80386
d) Pentium pro
View Answer
Answer: a
Explanation: Pentium 4 is a single core CPU used in desktops, laptops which are proposed by Intel. It has Netburst architecture.

14. Which of the following is a combination of several processors on a single chip?
a) Multicore architecture
b) RISC architecture
c) CISC architecture
d) Subword parallelism
View Answer
Answer: a
Explanation: The Multicore machine is a combination of many processors on a single chip. The heterogeneous multicore machine also combines a variety of processor types on a single chip.

15. Which is an example of the multi-core processor which possesses 10 cores?
a) Intel Xeon E7-2850
b) AMD Phenom IIX2
c) Intel core duo
d) AMD Phenom IIX3
View Answer
Answer: a

1. Which is the most basic non-volatile memory?
a) Flash memory
b) PROM
c) EPROM
d) ROM
View Answer
Answer: d
Explanation: The basic non-volatile memory is ROM or mask ROM, and the content of ROM is fixed in the chip which is useful in firmware programs for booting up the system.

2. Who has invented flash memory?
a) Dr.Fujio Masuoka
b) John Ellis
c) Josh Fisher
d) John Ruttenberg
View Answer
Answer: a
Explanation: Flash memory is invented by Dr. Fujio Masuoka at Toshiba in the 1980s which are non-volatile memory.

3. Which of the following is serial access memory?
a) RAM
b) Flash memory
c) Shifters
d) ROM
View Answer
Answer: c
Explanation: The memory arrays are basically divided into three which are random access memory, serial access memory, and content address memory. Serial access memory is divided into two, theses are shifters and queues.

4. Which is the early form of non-volatile memory?
a) magnetic core memory
b) ferrimagnetic memory
c) anti-magnetic memory
d) anti-ferromagnetic
View Answer
Answer: a
Explanation: The early form of non-volatile memory is known as magnetic core memory in which the ferromagnetic ring was magnetised to store data.

5. Which of the following memories has more speed in accessing data?
a) SRAM
b) DRAM
c) EPROM
d) EEPROM
View Answer
Answer: a
Explanation: SRAM have more speed than DRAM because it has 4 to 6 transistors arranged as flip-flop logic gates, that is it can be flipped from one binary state to another but DRAM has a small capacitor as its storage element.

6. In which memory, the signals are multiplexed?
a) DRAM
b) SRAM
c) EPROM

d) EEPROM
View Answer
Answer: a
Explanation: The signals in address bus are multiplexed with DRAM non-multiplexed with SRAM.

7. How many main signals are used with memory chips?
a) 2
b) 4
c) 6
d) 8
View Answer
Answer: b
Explanation: The main signals associated with memory chips are four. These are the signals associated with address bus, data bus, chip select signals, and control signals for read and write operations.

8. What is the purpose of the address bus?
a) to provide data to and from the chip
b) to select a specified chip
c) to select a location within the memory chip
d) to select a read/write cycle
View Answer
Answer: c
Explanation: Address bus is used to choose a particular location in the memory chip. Data bus is used to provide data to and from the chip. Chip select signals are used to select a particular chip within the memory.

9. Which are the two main types of processor connection to the motherboard?
a) sockets and slots
b) sockets and pins
c) slots and pins

d) pins and ports

Answer: a
Explanation: The type of processor which connects to a socket on the bottom surface of the chip that connects to the motherboard by Zero Insertion Force Socket. Intel 486 is an example of this type of connection. The processor slot is one which is soldered into a card, which connects to a motherboard by a slot. Example for slot connection is Pentium 3.

10. Which of the following has programmable hardware?
a) microcontroller
b) microprocessor
c) coprocessor
d) FPGA
View Answer
Answer: d
Explanation: Field programmable gate arrays are a type of multi-core architecture whose hardware function can be programmed by using hardware design tools.

11. Who invented TriMedia processor?
a) Intel
b) IBM
c) Apple
d) NXP Semiconductor
View Answer
Answer: d

1. Why is SRAM more preferably in non-volatile memory?
a) low-cost
b) high-cost
c) low power consumption

d) transistor as a storage element
View Answer
Answer: c
Explanation: SRAM will retain data as long it is powered up and it does not need to be refreshed as DRAM. It is designed for low power consumption and used in preference. DRAM is cheaper than SRAM but it is based on refresh circuitry as it loses charge since the capacitor is the storage element.

2. Which of the following ahs refreshes control mechanism?
a) DRAM
b) SRAM
c) Battery backed-up SRAM
d) Pseudo-static RAM
View Answer
Answer: d
Explanation: Pseudo RAM uses DRAM cells because of its higher memory density and it have refresh control which is an additional function of DRAM and is suitable for low power consumption. It has both the advantages of SRAM and DRAM.

3. Which storage element is used by MAC and IBM PC?
a) CMOS
b) Transistor
c) Capacitor
d) Inductor
View Answer
Answer: a
Explanation: CMOS is complementary metal oxide semiconductor which is used by MAC and IBM PC as storage element because it contains configuration data of SRAM and is battery back-up to ensure that it is powered up when the computer is switched off.

4. Which type of storage element of SRAM is very fast in accessing data but consumes lots of power?
a) TTL

b) CMOS
c) NAND
d) NOR
View Answer
Answer: a
Explanation: TTL or transistor-transistor logic which is a type of bipolar junction transistor access data very fastly but consumes lots of power whereas CMOS is used in low power consumption.

5. What is approximate data access time of SRAM?
a) 4ns
b) 10ns
c) 2ns
d) 60ns
View Answer
Answer: a
Explanation: SRAM access data in approximately 4ns because of its flip-flop arrangement of transistors whereas the data access time in DRAM is approximately 60ns since it has a single capacitor for one-bit storage.

6. Who proposed the miniature card format?
a) Intel
b) IBM
c) MIPS
d) Apple
View Answer
Answer: a
Explanation: Miniature Card is an SRAM memory card proposed by Intel in the 1980s but it was no longer manufactured.

7. How many MOSFETs are required for SRAM?
a) 2

b) 4
c) 6
d) 8
View Answer
Answer: c
Explanation: Six MOSFETs are required for a typical SRAM. Each bit of SRAM is stored in four transistors which form two cross-coupled inverters.

8. Which of the following is an SRAM?
a) 1T-RAM
b) PROM
c) EEPROM
d) EPROM
View Answer
Answer: a
Explanation: 1T-RAM is a pseudo-static RAM which is developed by MoSyS, Inc. PROM, EPROM, and EEPROM are non-volatile memories.

9. Which of the following can access data even when the power supply is lost?
a) Non-volatile SRAM
b) DRAM
c) SRAM

d) RAM
View Answer
Answer: a
Explanation: Random Access Memory is the primary storage which can access data only when it is powered up. But non-volatile SRAM can access data even when the power supply is lost. It is used in many applications like networking, aerospace etc.

10. Which of the following can easily convert to a non-volatile memory?
a) SRAM
b) DRAM
c) DDR SRAM
d) Asynchronous DRAM
View Answer
Answer: a

1. Which memory storage is widely used in PCs and Embedded Systems?
a) SRAM
b) DRAM
c) Flash memory
d) EEPROM
View Answer
Answer: b
Explanation: DRAM is used in PCs and Embedded systems because of its low cost. SRAM, flash memory and EEPROM are more costly than DRAM.

2. Which of the following memory technology is highly denser?
a) DRAM
b) SRAM
c) EPROM
d) Flash memory
View Answer
Answer: a
Explanation: DRAM is highly denser and cheaper because it only uses a single capacitor for storing one bit.

3. Which is the storage element in DRAM?
a) inductor
b) capacitor
c) resistor
d) mosfet
View Answer
Answer: b
Explanation: DRAM uses a small capacitor whose voltage represents a binary zero which is used as a storage element in DRAM in which a single transistor cell is used to store each bit of data.

4. Which one of the following is a storage element in SRAM?
a) capacitor
b) inductor
c) transistor
d) resistor
View Answer
Answer: c
Explanation: Four to six transistors are used to store a single bit of data and form a flip-flop logic gate and thus SRAM is faster in accessing data.

5. Which of the following is more volatile?
a) SRAM
b) DRAM
c) ROM
d) RAM
View Answer
Answer: b
Explanation: DRAM is said to be more volatile because it has a capacitor as its storage element in which the data disappears when the capacitor loses its charge so even when the device is powered the data can be lost.

6. What is the size of a trench capacitor in DRAM?
a) 1 Mb
b) 4-256 Mb
c) 8-128 Mb
d) 64-128 Mb
View Answer
Answer: b
Explanation: Trench capacitor can store from 4-256 Mb but planar capacitor can store up to 1 Mb.

7. Which of the following capacitor can store more data in DRAM?
a) planar capacitor
b) trench capacitor
c) stacked-cell
d) non-polar capacitor
View Answer
Answer: c
Explanation: Stacked-cell can store greater than 1 Gb. Planar capacitor can store up to 1 Mb and trench capacitor can store 4-256 Mb.
8. In which of the memories, does the data disappear?
a) SRAM

b) DRAM
c) Flash memory
d) EPROM
View Answer
Answer: b
Explanation: Both SRAM and DRAM are volatile memories and flash memory and EPROM are non-volatile memories. DRAM has a storage element as a capacitor whose charge loses gradually thereby losing data.

9. Which of the following is the main factor which determines the memory capacity?
a) number of transistors
b) number of capacitors
c) size of the transistor
d) size of the capacitor
View Answer
Answer: a
Explanation: The chip capacity is dependent on the number of transistors which can be fabricated on the silicon, and DRAM offers more storage capacity than SRAM.

10. What does VRAM stand for?
a) video RAM
b) verilog RAM
c) virtual RAM
d) volatile RAM
View Answer
Answer: a
Explanation: Video RAM is a derivative of DRAM. It functions as a DRAM and has additional functions to access data for video hardware for creating the display.

11. What does TCR stand for?
a) temperature-compensated refresh
b) temperature-compensated recovery
c) texas CAS-RAS
d) temperature CAS-RAS
View Answer
Answer: a

1. How many data lines does 256*4 have?
a) 256
b) 8
c) 4
d) 32
View Answer
Answer: c
Explanation: There are four data lines in the memory and these different organisations of memory and these different organisations of memory are apparent when upgrading memory and it also determines how many chips are needed.

2. How is the number of chips required is determined?
a) number of data lines
b) the minimum number of data
c) width of the data path from the processor
d) number of data lines and the width of the data path from the processor
View Answer
Answer: d
Explanation: The minimum number of chips is determined by the number of data lines and the width of the data path from the processor. For example, MC6800 family have a 16-bit wide datapath, 16*1 devices, 4*4 or 2*8 devices are needed.

3. Where is memory address stored in a C program?
a) stack
b) pointer
c) register
d) accumulator
View Answer
Answer: b
Explanation: Memory model is defined by a range of memory address which is accessible to the program. For example, in the C program, the memory address is stored in the pointer.

4. Which is the term that is used to refer the order of bytes?
a) endianness
b) memory organisation
c) bit
d) register
View Answer
Answer: a
Explanation: Endianness defines the order of bytes, that is, whether it is big endian or little endian. The former represents the higher order bits and the latter represents the lower order bits.

5. Which of the following processors uses big endian representation?
a) 8086
b) ARM
c) PowerPC
d) Zilog Z80
View Answer

Answer: c
Explanation: The IBM's PowerPC uses big endian representation whereas 8086, ARM and Zilog Z80 use little representation.

6. Which statement is true for a cache memory?
a) memory unit which communicates directly with the CPU
b) provides backup storage
c) a very high-speed memory to increase the speed of the processor
d) secondary storage
View Answer
Answer: c
Explanation: The RAM is the primary storage which directly communicates with the CPU. ROM is the secondary storage. Disk drives are capable of providing backup storage and the cache memory is a small high-speed memory which increases the speed of the processor.

7. Which of the following memory organisation have the entire memory available to the processor at all times?
a) segmented addressing
b) paging
c) virtual address
d) linear address
View Answer
Answer: d
Explanation: There are two types of memory organisation, linear addressing in which the entire memory is available to the processor of all times as in Motorola 6800 and the other is segmented addressing where the memory space is divided into several segments and the processor is limited to access the program instructions and data which are located in particular segments.

8. How many memory locations can be accessed by 8086?
a) 1 M
b) 2 M

c) 3 M
d) 4 M
View Answer
Answer: a
Explanation: The 8086 processor has a 20-bit address bus, hence it can access a memory of 2^{20}-1 M locations.
9. Which of them is a memory that is allocated to the program in LIFO pattern?
a) stack
b) index
c) accumulator
d) base
View Answer
Answer: a
Explanation: A stack is a memory which is allocated to the program in last-in, first out pattern. Stack pointer contains the memory address of the stack.

10. What does SIMM stand for?
a) single in-line memory module
b) single interrupt memory module
c) single information memory module
d) same-in-line memory module
View Answer
Answer: a
Explanation: SIMM is single in-line memory module is a kind of memory module, which contains random access memory used in computers of the early 1980s and 1990s.

11. Which of the memory organisation is widely used in parity bit?
a) by 1 organisation
b) by 4 organisation
c) by 8 organisation

d) by 9 organisation
View Answer
Answer: a
Explanation: The use of By 1 organisation is declined because of the wider data path devices. But it is still used in parity bit and were used in SIMM memory.

12. Which configuration of memory organisation replaces By 1 organisation?
a) by 4 organisation
b) by 8 organisation
c) by 9 organisation
d) by 16 organisation
View Answer
Answer: a
Explanation: By 1 organisation is replaced with By 4 organisation because of its reduced address bus and complexity.

13. Which shifting helps in finding the physical address in 8086?
a) shifting the segment by 8
b) shifting the segment by 6
c) shifting the segment by 4
d) shifting the segment by 2
View Answer
Answer: c
Explanation: The address bus of the 8086 is 20-bit and the data bus is 16-bit in size. So the physical address can be calculated by shifting the segment register by 4 to left and by adding the address bus to it.
14. Which memory organisation is supported in wider memories?
a) by 8 organisation
b) by 16 organisation
c) by 9 organisation

d) by 4 organisation
View Answer
Answer: b
Explanation: The wider memories support 16-bits because it can integrate more number of the interface logic so that the time consumed by the latches and buffers removes the memory access thus allowing the slower parts to be used in wait state free designs.

15. Which of the following is a plastic package used primarily for DRAM?
a) SIMM
b) DIMM
c) Zig-zag
d) Dual-in-line
View Answer
Answer: c

1. Which of the following have a 16 Mbytes addressed range?
a) PowerPC
b) M68000
c) DSP56000
d) TMS 320
View Answer
Answer: b
Explanation: The M68000 family has a 16 Mbyte addressing range. The PowerPC family has a larger 4 Gbyte range and the DSP56000 has a 128-kilo word address space.

2. Which of the following can destroy the accuracy in the algorithms?
a) delays

b) error signal
c) interrupt
d) mmu
View Answer
Answer: a
Explanation: The delays occurring in the memory management unit can destroy the accuracy in the algorithms and in order to avoid this, the linear addressing range should be increased.

3. How many numbers of ways are possible for allocating the memory to the modular blocks?
a) 1
b) 2
c) 3
d) 4
View Answer
Answer: c
Explanation: Most of the systems have a multitasking operating system in which the software consists of modular blocks of codes which run under the control of the operating system. There are three ways for allocating memory to these blocks. The first way distributes the block in a predefined way. The second way for allocating memory includes relocation or position independency in the software and the other way of allocating memory to the block is the address translation in which the logical address is translated to the physical address.

4. Which of the following is replaced with the absolute addressing mode?
a) relative addressing mode
b) protective addressing mode
c) virtual addressing mode
d) temporary addressing mode
View Answer
Answer: a
Explanation: The memory allocation of the modular blocks can be done by the writing the software program in relocatable or

position independent manner which can execute anywhere in the memory map, but relocatable code must have the same address between its data and code segments. This is used to avoid the use of absolute addressing modes which is replaced by the relative addressing modes.

5. What is the main purpose of the memory management unit?
a) address translation
b) large storage
c) reduce the size
d) provides address space
View Answer
Answer: a
Explanation: The memory management unit handles with physical addresses. Therefore, the virtual or the logical address is first translated to the physical address.

6. Which of the following provides stability to the multitasking system?
a) memory
b) DRAM
c) SRAM
d) Memory partitioning
View Answer
Answer: d
Explanation: The memory partitioning provides stability to the multitasking system so that the errors within one task will not corrupt the other tasks.

7. Which of the following is used by the M68000 family?
a) M68000
b) 80386
c) 8086
d) 80286
View Answer

Answer: a
Explanation: The M68000 uses memory partitioning by the use of function code or by the combination of superscalar signals and the Harvard architecture.

8. What can be done for the fine grain protection of the processor?
a) add extra description bit
b) add error signal
c) add wait stage
d) remains unchanged
View Answer
Answer: a
Explanation: The finer grain protection of memory management is achieved by the addition of extra description bit to an address to declare its status. The memory management unit can detect an error if the task attempts to access memory that has not been allocated to it or a certain kind of mismatch occurs.

9. Which of the following technique is used by the UNIX operating system?
a) logical address memory
b) physical address memory
c) virtual memory technique
d) translational address
View Answer
Answer: c
Explanation: In the workstation and in the UNIX operating system virtual memory technique is frequently used in which the main memory is divided into different segments and pages. These pages will have a virtual address which can increase the address spacing.

10. Which of the following consist two lines of legs on both sides of a plastic or ceramic body?
a) SIMM
b) DIMM
c) Zig-zag
d) Dual in-line
View Answer
Answer: d
Explanation: The dual-in-line package consists of two lines of legs on both sides of the plastic or ceramic. Most commonly used are BIOS EPROMs, DRAM and SRAM.

11. Which package has high memory speed and change in the supply?
a) DIP
b) SIMM
c) DIMM
d) zig-zag
View Answer
Answer: c
Explanation: DIMM is a special version of SIMM which is 168-bits wider bus and looks similar to a larger SIMM. The wider bus increases the memory speed and change in supply voltage.

12. Which is a subassembly package?
a) dual-in-line
b) zig-zag
c) simm
d) ceramic shell
View Answer
Answer: c
Explanation: The SIMM is basically a subassembly, not a package. It is a small board which possesses finger connection on the bottom and sufficient memory on the board in order to make up the required configuration.

13. What is the required voltage of DIMM?
a) 2V
b) 2.2V
c) 5V
d) 3.3V
View Answer
Answer: d
Explanation: For increasing the speed and reducing the power consumption, it is necessary to reduce the power supply. Today's CPUs and memories have 3.3V supply or even lower instead of the signal level from 0 to 5V. DIMMS are described by its voltage, speed, and memory type respectively as 3.3V 133MHz SDRAM DIMM.

14. Which memory package has a single row of pins?
a) SIMM
b) DIP
c) SIP
d) zig-zag
View Answer
Answer: c
Explanation: The Single-in-line package is the same as that of SIMM, in which the finger connections are replaced by a single row of pins. SIP took the popularity of SIMM but nowadays it is rarely seen.
15. What is the access time of MCM51000AP10?
a) 100ns
b) 80ns
c) 60ns
d) 40ns
View Answer
Answer: a

1. Which is the very basic technique of refreshing DRAM?
a) refresh cycle

b) burst refresh
c) distributive refresh
d) software refresh
View Answer
Answer: a
Explanation: The DRAM needs to be periodically refreshed and the very basic technique is a special refresh cycle, during these cycles no other access is permitted. The whole chip is refreshed within a particular time period otherwise, the data will be lost.

2. How is the refresh rate calculated?
a) by refresh time
b) by the refresh cycle
c) by refresh cycle and refresh time
d) refresh frequency and refresh cycle
View Answer
Answer: c
Explanation: The time required for refreshing the whole chip is known as refresh time. The number of access needed to complete refresh is called as the number of cycles. The number of cycles divided by the refresh time gives the refresh rate.

3. Which is the commonly used refresh rate?
a) 125 microseconds
b) 120 microseconds
c) 130 microseconds
d) 135 microseconds
View Answer
Answer: a
Explanation: There are two refresh rates used in common. They are standard refresh rate of 15.6 microseconds and 125 microseconds which the extended form.

4. How can we calculate the length of the refresh cycle?
a) twice of normal access
b) thrice of normal access
c) five times of normal access
d) six times of normal access
View Answer
Answer: a
Explanation: Each of the refresh cycles is approximately as twice as the length of the normal access, for example, a 70ns DRAM has a refresh cycle time of 130ns.

5. What type of error occurs in the refresh cycle of the DRAM?
a) errors in data
b) power loss
c) timing issues
d) not accessing data
View Answer
Answer: c
Explanation: When the refresh cycle in a DRAM is running, it will not access data, so the processor will have to wait for its data. This arises some timing issues.

6. What is the worst case delay of the burst refresh in 4M by 1 DRAM?
a) 0.4ms
b) 0.2ms
c) 170ns
d) 180ns
View Answer
Answer: b
Explanation: A 4M by 1 DRAM have 1024 refresh cycles. Bursting delay will be 0.2ms that are, the worst case delay is 1024 times larger than that of the single refresh cycle. The distributed delay is about 170ns.

7. Which refresh techniques depends on the size of time critical code for calculating the refresh cycle?
a) burst refresh
b) distributed refresh
c) refresh cycle
d) software refresh
View Answer
Answer: b
Explanation: Most of the system uses the distributed method and depending on the size of the time critical code, the number of refresh cycles can be calculated.

8. Which of the following uses a timer for refresh technique?
a) RAS
b) CBR
c) software refresh
d) CAS
View Answer
Answer: c
Explanation: The software refresh performs the action by using a routine to periodically cycle through the memory and refreshes. It uses a timer in the program generating an interrupt. This interrupt performs the refreshing part in the DRAM.

9. What is the main disadvantage in the software refresh of the DRAM?
a) timer
b) delay
c) programming delay
d) debugging
View Answer
Answer: d
Explanation: Debugging in software refresh is very difficult to perform because they may stop the refreshing and if the refreshing is stopped, the contents get lost.

10. Which refresh technique is useful for low power consumption?
a) Software refresh
b) CBR
c) RAS
d) Burst refresh
View Answer
Answer: b
Explanation: CBR that is, CAS before RAS refresh is the one which is commonly used. It has low power consumption quality because it does not have address bus and the buffers can be switched off. It is worked by using an internal address counter which is stored on the memory chip itself and this can be incremented periodically.

11. Which refreshing techniques generate a recycled address?
a) RAS
b) CBR
c) Distributed refresh
d) Software refresh
View Answer
Answer: a
Explanation: The row address is placed on the address bus and the column address is held off which generates the recycle address. The address generation is done by an external hardware controller.

12. Which of the following uses a software refresh in the DRAM?
a) 8086
b) 80386
c) Pentium
d) Apple II personal computer
View Answer

Answer: d
Explanation: The Apple II personal computer has a particular memory configuration, periodically the DRAM gets blocked and is used for video memory accessing to update the screen which can refresh the DRAM.

13. How do CBR works?
a) by asserting CAS before RAS
b) by asserting CAS after RAS
c) by asserting RAS before CAS
d) by asserting CAS only
View Answer
Answer: a
Explanation: CBR works by an internal address counter which is periodically incremented. The mechanism is based on CAS before RAS. Each time when RAS is asserted, the refresh cycle performs and the counter is incremented.

14. Which of the refresh circuit is similar to CBR?
a) software refresh
b) hidden refresh
c) burst refresh
d) distribute refresh
View Answer
Answer: b
Explanation: In the hidden refresh, the refresh cycle is added to the end of a normal read cycle. The RAS signal goes high and is then asserted low. At the end of the read cycle, the CAS is still asserted. This is similar to the CBR mechanism, that is, toggling of the RAS signal at the end of the read cycle starts a CBR refresh cycle.

15. Which technology is standardized in DRAM for determining the maximum time interval between the refresh cycle?
a) IEEE
b) RAPID
c) JEDEC

d) UNESCO
View Answer
Answer: c

1. In which pin does the data appear in the basic DRAM interfacing?
a) dout pin
b) din pin
c) clock
d) interrupt pin
View Answer
Answer: a
Explanation: In the basic DRAM interfacing, the higher order bits asserts the RAS signal and the lower order bits asserts the CAS signal. When the access got expired, the data appears on the dout pin and is latched by the processor.

2. What is the duration for memory refresh to remain compatible?
a) 20 microseconds
b) 12 microseconds
c) 15 microseconds
d) 10 microseconds
View Answer
Answer: c
Explanation: The memory refresh is performed every 15 microseconds in order to remain compatible.

3. Which interfacing method lowers the speed of the processor?
a) basic DRAM interface
b) page mode interface
c) page interleaving

d) burst mode interface
View Answer
Answer: a
Explanation: The direct method access limits the wait state-free operation which lowers the processor speed.
4. What is EDO RAM?
a) extreme data operation
b) extended direct operation
c) extended data out
d) extended DRAM out
View Answer
Answer: c
Explanation: EDO RAM is a special kind of random access memory which can improve the time to read from the memory on faster microprocessors. The example of such a microprocessor is Intel Pentium.

5. What is RDRAM?
a) refresh DRAM
b) recycle DRAM
c) Rambus DRAM
d) refreshing DRAM
View Answer
Answer: c
Explanation: Rambus DRAM is a synchronous memory developed by Rambus. It can replace SDRAM and is useful in high bandwidth applications.

6. Which of the following can transfer up to 1.6 billion bytes per second?
a) DRAM
b) RDRAM
c) EDO RAM

d) SDRAM
View Answer
Answer: b
Explanation: The Rambus RAM can transfer up to 1.6 billion bytes per second. It possesses RAM controller, a bus which connects the microprocessor and the device, and random access memory.

7. Which of the following cycle is larger than the access time?
a) write cycle
b) set up time
c) read cycle
d) hold time
View Answer
Answer: c
Explanation: The read cycle in the DRAM interfacing is larger than the access time because of the precharge time.

8. Which mode of operation selects an internal page of memory in the DRAM interfacing?
a) page interleaving
b) page mode
c) burst mode
d) EDO RAM
View Answer
Answer: b
Explanation: In the page mode operation, the row address is provided as normal but the RAS signal is left asserted. This, in turn, selects an internal page within the DRAM memory where any bit of data can be accessed by placing the column address and asserting CAS.

9. What is the maximum time that the RAS signal can be asserted in the page mode operation?
a) 5 microseconds
b) 10 microseconds
c) 15 microseconds

d) 20 microseconds
View Answer
Answer: b
Explanation: The maximum time that the RAS signal can be asserted during the page mode operation is about 10 microseconds. But this is a major disadvantage for page mode operation, that is, the standard PCs have a maximum time of 15 microseconds for the refresh cycle.
10. Which of the following mode of operation in the DRAM interfacing has a page boundary?
a) burst mode
b) EDO RAM
c) page mode
d) page interleaving
View Answer
Answer: c
Explanation: The page mode operation have memory cycles that exhibit some form of locality, that is, stay within the page boundary which causes page missing when there is access outside the page boundary and two or more wait states.

11. Which mode offers the banking of memory in the DRAM interfacing technique?
a) page mode
b) basic DRAM interfacing
c) page interleaving
d) burst mode
View Answer
Answer: c
Explanation: The accessing of data outside the page boundary can cause missing of pages in the page mode operation. So a program has to operate for frequently accessing data thereby, increasing the efficiency in the page selection. One such mode is the page interleaving mode in which the memory is divided into different banks, depending on the number of memories installed.

12. Which of the following has a fast page mode RAM?
a) burst mode

b) page interleaving
c) EDO memory
d) page mode
View Answer
Answer: c
Explanation: Extended data out memory is a fast page mode RAM which has a faster cycling process which makes EDO memory a faster page mode access.

13. Which mode reduces the need for fast static RAMs?
a) page mode
b) page interleaving
c) burst mode
d) EDO memory
View Answer
Answer: c
Explanation: The page mode, nibble mode devices can provide data fastly when the new column address is given. In burst mode operation, the processor can fetch more data than it needs and keeps the remaining data in an internal cache for the future use which can reduce the need for fast static RAMs.

14. Which of the following is also known as hyper page mode enabled DRAM?
a) page mode
b) EDO DRAM
c) burst EDO DRAM
d) page interleaving
View Answer
Answer: b
Explanation: The EDO DRAM is also known as hyper page mode enable DRAM because of the faster page mode operation along with some additional features.

15. What does BEDO DRAM stand for?
a) burst EDO DRAM
b) buffer EDO DRAM
c) BIBO EDO DRAM
d) bilateral EDO DRAM
View Answer
Answer: a

1. Which of the following is more quickly accessed?
a) RAM
b) Cache memory
c) DRAM
d) SRAM
View Answer
Answer: b
Explanation: The cache memory is a small random access memory which is faster than a normal RAM. It has a direct connection with the CPU otherwise, there will be a separate bus for accessing data. The processor will check whether the copy of the required data is present in the cache memory if so it will access the data from the cache memory.

2. Which factor determines the effectiveness of the cache?
a) hit rate
b) refresh cycle
c) refresh rate
d) refresh time
View Answer
Answer: a
Explanation: The proportion of accesses of data that forms the cache hit, which measures the effectiveness of the cache memory.

3. Which of the following determines a high hit rate of the cache memory?
a) size of the cache
b) number of caches
c) size of the RAM
d) cache access
View Answer
Answer: a
Explanation: The size of the cache increases, a large amount of data can be stored, which can access more data which in turn increases the hit rate of the cache memory.

4. Which of the following is a common cache?
a) DIMM
b) SIMM
c) TLB
d) Cache
View Answer
Answer: c
Explanation: The translation lookaside buffer is common cache memory seen in almost all CPUs and desktops which are a part of the memory management unit. It can improve the virtual address translation speed.

5. Which factor determines the number of cache entries?
a) set commutativity
b) set associativity
c) size of the cache
d) number of caches
View Answer
Answer: b
Explanation: The set associativity is a criterion which describes the number of cache entries which could possibly contain the required data.

6. What is the size of the cache for an 8086 processor?
a) 64 Kb
b) 128 Kb
c) 32 Kb
d) 16 Kb
View Answer
Answer: a
Explanation: The 8086 processor have a 64 Kbytes cache, beyond this size, the cost will be extremely high.

7. How many possibilities of mapping does a direct mapped cache have?
a) 1
b) 2
c) 3
d) 4
View Answer
Answer: a
Explanation: The direct mapped cache only have one possibility to fetch data whereas a two-way system, there are two possibilities, for a three-way system, there are three possibilities and so on. It is also known as the one-way set associative cache.

8. Which of the following allows speculative execution?
a) 12-way set associative cache
b) 8-way set associative cache
c) direct mapped cache
d) 4-way set associative cache
View Answer
Answer: c
Explanation: The direct mapped cache has the advantage of allowing a simple and fast speculative execution.

9. Which of the following refers to the number of consecutive bytes which are associated with each cache entry?
a) cache size
b) associative set
c) cache line
d) cache word
View Answer
Answer: c
Explanation: The cache line refers to the number of consecutive bytes which are associated with each cache entry. The data is transferred between the memory and the cache in a particular size which is called a cache line.

10. Which factor determines the cache performance?
a) software
b) peripheral
c) input
d) output
View Answer
Answer: a
Explanation: The cache performance is completely dependent on the system and software. In software, the processor checks out each loop and if a duplicate is found in the cache memory, immediately it is accessed.

11. What are the basic elements required for cache operation?
a) memory array, multivibrator, counter
b) memory array, comparator, counter
c) memory array, trigger circuit, a comparator
d) memory array, comparator, CPU
View Answer
Answer: b
Explanation: The cache memory operation is based on the address tag, that is, the processor generates the address which is provided to the cache and this cache stores its data with an address tag. The tag is compared with the address, if they did not

match, the next tag is checked. If they match, a cache hit occurs, the data is passed to the processor. So the basic elements required is a memory array, comparator, and a counter.
12. How many divisions are possible in the cache memory based on the tag or index address?
a) 3
b) 2
c) 4
d) 5
View Answer
Answer: c

13. What does DMA stand for?
a) direct memory access
b) direct main access
c) data main access
d) data memory address
View Answer
Answer: a

1. Which of the following cache has a separate comparator for each entry?
a) direct mapped cache
b) fully associative cache
c) 2-way associative cache
d) 16-way associative cache
View Answer
Answer: b
Explanation: A fully associative cache have a comparator for each entry so that all the entries can be tested simultaneously.
2. What is the disadvantage of a fully associative cache?
a) hardware
b) software

c) memory
d) peripherals
View Answer
Answer: a
Explanation: The major disadvantage of the fully associative cache is the amount of hardware needed for the comparison increases in proportion to the cache size and hence, limits the fully associative cache.

3. How many comparators present in the direct mapping cache?
a) 3
b) 2
c) 1
d) 4
View Answer
Answer: c
Explanation: The direct mapping cache have only one comparator so that only one location possibly have all the data irrespective of the cache size.

4. Which mapping of cache is inefficient in software viewpoint?
a) fully associative
b) 2 way associative
c) 16 way associative
d) direct mapping
View Answer
Answer: d
Explanation: The direct mapping cache organization is simple from the hardware design aspects but it is inefficient in the software viewpoint.

5. Which mechanism splits the external memory storage into memory pages?
a) index mechanism
b) burst mode

c) distributive mode
d) a software mechanism
View Answer
Answer: a
Explanation: The index mechanism splits the external memory storage into a series of memory pages in which each page is the same size as the cache. Each page is mapped to the cache so that each page can have its own location in the cache.

6. Which of the following cache mapping can prevent bus thrashing?
a) fully associative
b) direct mapping
c) n way set associative
d) 2 way associative
View Answer
Answer: c
Explanation: Only one data can be accessed in direct mapping that is, if one word is accessed at a time, all other words are discarded at the same time. This is known as bus thrashing which can be solved by splitting up the caches so there are 2,4,..n possible entries available. The major advantage of the set associative cache is its capability to prevent the bus thrashing at the expense of hardware.
7. Which cache mapping have a sequential execution?
a) direct mapping
b) fully associative
c) n way set associative
d) burst fill
View Answer
Answer: d
Explanation: The burst fill mode of cache mapping have a sequential nature of executing instructions and data access. The instruction fetches and execution accesses to sequential memory locations until it has a jump instruction or a branch instruction. This kind of cache mapping is seen in the MC68030 processor.

8. Which address is used for a tag?
a) memory address
b) logical address
c) cache address
d) location address
View Answer
Answer: b
Explanation: The cache memory uses either a physical address or logical address for its tag data. For a logical cache, the tag refers to a logical address and for a physical cache, the tag refers to the physical address.

9. In which of the following the data is preserved within the cache?
a) logical cache
b) physical cache
c) unified cache
d) harvard cache
View Answer
Answer: b
Explanation: In the physical cache, the data is preserved within the cache because it does not flush out during the context switching but on the other hand, the logical cache flushes out the data and clear it during a context switching.

10. What is the disadvantage of the physical address?
a) debugging
b) delay
c) data preservation
d) data cleared
View Answer
Answer: b
Explanation: The physical address access the data through the memory management unit which causes a delay.

11. Which cache memory solve the cache coherency problem?
a) physical cache
b) logical cache
c) unified cache
d) harvard cache
View Answer
Answer: a
Explanation: The physical cache is more efficient and can provide the cache coherency problem solved and MMU delay is kept to a minimum. PowerPC is an example for this advantage.
12. What type of cache is used in the Intel 80486DX?
a) logical
b) physical
c) harvard
d) unified
View Answer
Answer: d
Explanation: The Intel 80486DX processor has a unified cache. Similarly, Motorola MPC601PC also uses the unified cache. The unified cache has the same mechanism to store both data and instructions.

13. Which of the following has a separate cache for the data and instructions?
a) unified
b) harvard
c) logical
d) physical
View Answer
Answer: b
Explanation: The Harvard cache have a separate cache for the data and the instruction whereas the unified cache has a same cache for the data and instructions.

14. Which type of cache is used the SPARC architecture?
a) unified
b) harvard
c) logical
d) physical
View Answer
Answer: c
Explanation: The SPARC architecture uses logical cache whereas most of the internal cache designed now, uses physical cache because data is not flushed out in this cache.

15. Which of the following approach uses more silicon area?
a) unified
b) harvard
c) logical
d) physical
View Answer
Answer: b

1. Which of the following is the biggest challenge in the cache memory design?
a) delay
b) size
c) coherency
d) memory access
View Answer
Answer: c
Explanation: The coherency is a major challenge in designing the cache memory. The cache has to be designed by solving the problem of data coherency while remaining hardware and software compatible.

2. What arises when a copy of data is held both in the cache and in the main memory?
a) stall data
b) stale data
c) stop data
d) wait for the state
View Answer
Answer: b
Explanation: The stale data arises when the copy is held both in the cache memory and in the main memory. If either copy is modified, the other data become stale and the system coherency can be destroyed.

3. In which writing scheme does all the data writes go through to main memory and update the system and cache?
a) write-through
b) write-back
c) write buffering
d) no caching of writing cycle
View Answer
Answer: a
Explanation: There are different writing scheme in the cache memory which increases the cache efficiency and one such is the write-through in which all the data go to the main memory and can update the system as well as the cache.

4. In which writing scheme does the cache is updated but the main memory is not updated?
a) write-through
b) write-back
c) no caching of writing cycle
d) write buffering
View Answer
Answer: b
Explanation: The cache write-back mechanism needs a bus snooping system for the coherency. In this write-back scheme, the cache is updated first and the main memory is not updated.

5. In which writing scheme does the cache is not updated?
a) write-through
b) write-back
c) write buffering
d) no caching of writing cycle
View Answer
Answer: d
Explanation: The no caching write cycle does not update the cache but the data is written to the cache. If the previous data had cached, that entry is invalid and will not use. This makes the processor fetch data directly from the main memory.

6. Which writing mechanism forms the backbone of the bus snooping mechanism?
a) write-back
b) write-through
c) no caching of write cycles
d) write buffer
View Answer

7. What is the main idea of the writing scheme in the cache memory?
a) debugging
b) accessing data
c) bus snooping
d) write-allocate
View Answer
Answer: c
Explanation: There are four main writing scheme in the cache memory which is, write-through, write-back, no caching of the write cycle and write buffer. All these writing schemes are designed for bus snooping which can reduce the coherency.

8. In which scheme does the data write via a buffer to the main memory?
a) write buffer
b) write-back
c) write-through
d) no caching of the write cycle
View Answer
Answer: a
Explanation: The write-buffer is slightly similar to the write-through mechanism in which data is written to the main memory but in write buffer mechanism data writes to the main memory via a buffer.

9. Which of the following can allocate entries in the cache for any data that is written out?
a) write-allocate cache
b) read-allocate cache
c) memory-allocate cache
d) write cache
View Answer
Answer: a
Explanation: A write-allocate cache allocates the entries in the cache for any data that is written out. If the data is transferred to the external memory so that, when it is accessed again, the data is already waiting in the cache. It works efficiently if the size of the cache is large and it does not overwrite even though it is advantageous.

10. Which of the following uses a bus snooping mechanism?
a) MC88100
b) 8086
c) 8051
d) 80286
View Answer
Answer: a
Explanation: The bus snooping mechanism uses a combination of cache tag status, write policies and bus monitoring to ensure coherency. MC88100 or MC88200 uses bus snooping mechanism.

11. What leads to the development of MESI and MEI protocol?
a) cache size
b) cache coherency
c) bus snooping
d) number of caches
View Answer
Answer: b
Explanation: The problem of cache coherency lead to the formation of two standard mechanisms called MESI and MEI protocol. MC88100 have MESI protocol and MC68040 uses an MEI protocol.

12. Which of the following is also known as Illinois protocol?
a) MESI protocol
b) MEI protocol
c) Bus snooping
d) Modified exclusive invalid
View Answer
Answer: a
Explanation: The MESI protocol is also known as Illinois protocol because of its formation at the University of Illinois.

13. What does MESI stand for?
a) modified exclusive stale invalid
b) modified exclusive shared invalid
c) modified exclusive system input
d) modifies embedded shared invalid
View Answer
Answer: b
Explanation: The MESI protocol supports a shared state which is a formal mechanism for controlling the cache coherency by using the bus snooping techniques. MESI refers to the states that cached data can access. In MESI protocol, multiple processors can cache shared data.

14. What does MEI stand for?
a) modified embedded invalid
b) modified embedded input
c) modified exclusive invalid
d) modified exclusive input
View Answer
Answer: c
Explanation: MEI protocol is less complex and is easy to implement. It does not allow shared state for the cache.

15. Which protocol does MPC601 use?
a) MESI protocol
b) MEI protocol
c) MOSI protocol
d) MESIF protocol
View Answer
Answer: a

1. Which of the following include special address generation and data latches?
a) burst interface
b) peripheral interface
c) dma
d) input-output interfacing
View Answer
Answer: a
Explanation: The burst interfacing has special memory interfaces which include special address generation and data latches that help in the high performance of the processors. It takes the advantages of both the nibble mode memories and paging.
2. Which of the following makes use of the burst fill technique?
a) burst interfaces

b) dma
c) peripheral interfaces
d) input-output interfaces
View Answer
Answer: a
Explanation: The burst interfaces use the burst fill technique in which the processor will access four words in succession, which fetches the complete cache line or written out to the memory.

3. How did burst interfaces access faster memory?
a) segmentation
b) dma
c) static column memory
d) memory
View Answer
Answer: c
Explanation: The speed of the memory can be improved by the page mode or the static column memory which offer a faster access in a single cycle.

4. Which of the following memory access can reduce the clock cycles?
a) bus interfacing
b) burst interfacing
c) dma
d) dram
View Answer
Answer: b
Explanation: The burst interfaces reduces the clock cycles. For fetching four words with a three clock memory, it will take 12 clock cycle but in the burst interface, it will only take five clocks to access the data.

5. How many clocks are required for the first access in the burst interface?
a) 1

b) 2
c) 3
d) 4
View Answer
Answer: b
Explanation: In the burst interface, the first access of the memory address requires two clock cycles and a single cycle for the remaining memory address.

6. In which of the following access, the address is supplied?
a) the first access
b) the second access
c) third access
d) fourth access
View Answer
Answer: a
Explanation: In the burst interface, the address is supplied only for the first access and not for the remaining accesses. An external logic is required for the additional addresses for the memory interface.

7. What type of timing is required for the burst interfaces?
a) synchronous
b) equal
c) unequal
d) symmetrical
View Answer
Answer: c
Explanation: The burst interfacing uses an unequal timing. It takes two clocks for the first access and only one for the remaining accesses which make it an unequal timing.

8. How can gate delays be reduced?
a) synchronous memory
b) asynchronous memory
c) pseudo asynchronous memory
d) symmetrical memory
View Answer
Answer: a
Explanation: The burst interfaced is associated with the SRAM and for the efficiency of the SRAM, it uses a synchronous memory on-chip latches to reduce the gate delays.

9. In which memory does the burst interfaces act as a part of the cache?
a) DRAM
b) ROM
c) SRAM
d) Flash memory
View Answer
Answer: c
Explanation: The burst interface is associated with the static RAM.

10. Which of the following uses a wrap around burst interfacing?
a) MC68030
b) MC68040
c) HyperBus
d) US 5729504 A
View Answer
Answer: b
Explanation: MC68040 is developed by the Motorola which uses a wrap around burst interfacing. MC68030 is also developed by Motorola but it uses a linear line fill burst. HyperBus can switch to both linear and wrap around burst. US 5729504 A uses a linear burst fill.

11. Which of the following is a Motorola’s protocol product?
a) MCM62940
b) Avalon
c) Slave interfaces
d) AXI slave interfaces
View Answer
Answer: a
Explanation: MCM62940 protocol is developed by Motorola, whereas Slave interfaces, AXI slave interfaces are for ARM. Avalon is developed by Altera.

12. Which of the following uses a linear line fill interfacing?
a) MC68040
b) MC68030
c) US 74707 B2
d) Hyper Bus
View Answer
Answer: b
Explanation: MC68030 uses a linear burst fill whereas MC68040, US 74707 B2 uses to wrap around burst interfacing. HyperBus can switch to both linear and wrap around interfacing.

13. Which of the following protocol matches the Intel 80486?
a) MCM62940
b) MCM62486
c) US 74707 B2
d) Hyper Bus
View Answer
Answer: b
Explanation: The MCM62486 has an on-chip counter that matches the Intel 80486 and is developed by the Motorola.

14. Which of the following protocol matches the MC68040?
a) MCM62486
b) US 5729504 A
c) HyperBus
d) MCM62940
View Answer
Answer: d

1. The modified bit is also known as
a) dead bit
b) neat bit
c) dirty bit
d) invalid bit
View Answer
Answer:c
Explanation: The dirty bit is said to be set if the processor modifies its memory. This bit indicates that the associative set of blocks regarding the memory is modified and has not yet saved to the storage.

2. Which of the following have an 8 KB page?
a) DEC Alpha
b) ARM
c) VAX
d) PowerPC
View Answer
Answer:a
Explanation: DEC Alpha divides its memory into 8KB pages whereas VAX is a small page which is only 512 bytes in size. PowerPC pages are normally 4 KB and ARM is having 4 KB and 64 KB pages.

3. Which of the following address is seen by the memory unit?
a) logical address
b) physical address
c) virtual address
d) memory address
View Answer
Answer: b
Explanation: The logical address is the address generated by the CPU. It is also known as virtual address. The physical address is the address which is seen by the memory unit.

4. Which of the following modes offers segmentation in the memory?
a) virtual mode
b) real mode
c) protected mode
d) memory mode
View Answer
Answer: c
Explanation: The main memory can split into small blocks by the method of paging and segmentation and these mechanisms are possible only in protected mode.

5. Which of the following is necessary for the address translation in the protected mode?
a) descriptor
b) paging
c) segmentation
d) memory
View Answer
Answer: a
Explanation: The address translation from the logical address to physical address partitions the main memory into different blocks which is called segmentation. Each of these blocks have a descriptor which possesses a descriptor table. So the size of every block is very important for the descriptor.

6. What does “G” in the descriptor entry describe?
a) gain
b) granularity
c) gate voltage
d) global descriptor
View Answer
Answer: b
Explanation: The granularity bit controls the resolution of the segmented memory. When it is set to logic one, the resolution is 4 KB. When the granularity bit is set to logic zero, the resolution is 1 byte.

7. How many types of tables are used by the processor in the protected mode?
a) 1
b) 2
c) 3
d) 4
View Answer
Answer: b
Explanation: There are two types of descriptor table used by the processor in the protected mode which are GDT and LDT, that is global descriptor table and local descriptor table respectively.

8. What does the table indicator indicate when it is set to one?
a) GDT
b) LDT
c) remains unchanged
d) toggles with GTD and LTD
View Answer
Answer: b
Explanation: The table indicator is a part of selector that selects which table is to be used. If the table indicator is set to logic one, the will use the local descriptor table and if the table indicator is set to logic zero, it will use the global descriptor table.

9. What does GDTR stand for?
a) global descriptor table register
b) granularity descriptor table register
c) gate register
d) global direct table register
View Answer
Answer: a
Explanation: The global descriptor table register is a special register which have the linear address and the size of its own GDT. Both the global descriptor table register and local descriptor table register are located in the global descriptor table.

10. What does PMMU stands for?
a) protection mode memory management unit
b) paged memory management unit
c) physical memory management unit
d) paged multiple management unit
View Answer
Answer: b
Explanation: The paged memory management unit is used to decrease the amount of storage needed in the page tables, that is, a multi-level tree structure is used. MC68030, PowerPC, ARM 920 uses a paged memory management unit.

11. Which of the following support virtual memory?
a) segmentation
b) descriptor
c) selector
d) paging
View Answer
Answer: d
Explanation: The paging mechanism supports the virtual memory. Paging helps in creating virtual address space which has a major role in memory management.

12. What does DPL in the descriptor describes?
a) descriptor page level
b) descriptor privilege level
c) direct page level
d) direct page latch
View Answer
Answer: b
Explanation: The descriptor privilege level is used to restrict access to the segment which helps in protection mechanism. It acquires two bit of the descriptor.

13. What does “S” bit describe in a descriptor?
a) descriptor type
b) small type
c) page type
d) segmented type
View Answer
Answer: a

1. How many regions are created by the memory range in the ARM architecture?
a) 4
b) 8
c) 16
d) 32
View Answer
Answer: b

2. How many bits does the memory region in the ARM memory protection unit have?
a) 1
b) 2
c) 3
d) 4
View Answer
Answer: c
Explanation: The memory region possesses three bits which are the cacheable bit, bufferable bit and access permission bit.

3. Which of the following uses a priority level for permitting data?
a) ARM memory management unit
b) ARM protection memory management unit
c) Bus interface unit
d) Execution unit
View Answer
Answer: b
Explanation: In the ARM protection architecture, the memory is divided into some regions of size 4 Kbytes to 4 Gbytes. These regions possess bits called the cacheable bit, buffer bit, and access permitted bits. The regions are numbered as per priority level for which the permission bits takes the precedence if any of the regions gets overlapped.

4. What type of bit in the ARM memory mimics to that of the protection unit of ARM management unit?
a) permission bit
b) buffer bit
c) cacheable bit
d) access permission bit
View Answer
Answer: a

5. Which of the following bits are used to control the cache behaviour?
a) cacheable bit

b) buffer bit
c) cacheable bit and buffer bit
d) cacheable bit, buffer bit and permission access bit
View Answer
Answer: c
Explanation: The cacheable bit and the buffer bit are used to control the behaviour of cache. Depending on the cacheable bit and the buffer bit, the memory access will complete successfully.

6. Which of the following unit provides security to the processor?
a) bus interface unit
b) execution unit
c) peripheral unit
d) memory protection unit
View Answer
Answer: d
Explanation: The memory management unit and the memory protection unit provides security to the processor by trapping the invalid memory accesses before they corrupt other data.

7. Which of the following includes a tripped down memory management unit?
a) memory protection unit
b) memory real mode
c) memory management unit
d) bus interface unit
View Answer
Answer: a
Explanation: The memory protection unit allows a tripped memory down memory management unit in which the memories are partitioned and protected without any address translation. This can remove the time consumption in the address translation thereby increases the speed.
8. Which of the following can reduce the chip size?
a) memory management unit

b) execution unit
c) memory protection unit
d) bus interface unit
View Answer
Answer: c
Explanation: The memory protection unit have many advantages over the other units. It can reduce the chip size, cost and power consumption.

9. How does the memory management unit provide the protection?
a) disables the address translation
b) enables the address translation
c) wait for the address translation
d) remains unchanged
View Answer
Answer: a
a) error signal
b) default signal
c) wait for the signal
d) interrupt signal
View Answer
Answer: a
Explanation: If memory access from the software does not access the correct data, an error signal is generated which will start a supervisor level software for the decision.
11. What happens when a task attempts to access memory outside its own address space?
a) paging fault
b) segmentation fault
c) wait
d) remains unchanged
View Answer

Answer: b

1. Which of the following can transfer multiple bits of data simultaneously?
a) serial port
b) sequential port
c) concurrent unit
d) parallel port
View Answer
Answer: d
Explanation: The parallel port can transfer multiple bits of data simultaneously. It provides the input or output binary data with a single bit allocated to each pin within the port.
2. Which of the following are interfaced as inputs to the parallel ports?
a) LEDs
b) switch
c) alphanumeric display
d) seven segmented display
View Answer
Answer: b
Explanation: The LEDs, alphanumeric displays, seven segment displays are interfaced for the output whereas the switch is an input port.
3. Which of the following are interfaced as the outputs to the parallel ports?
a) keyboards
b) switches
c) LEDs
d) knobs
View Answer
Answer: c
Explanation: The keyboards, switches, and knobs are used as output whereas the LEDs are used as the input port.

4. How many registers are there to control the parallel port in the basic form?
a) 1
b) 3
c) 2
d) 5
View Answer
Answer: c
Explanation: The basic operation of the parallel port dealt with two types of registers which are called data direction register and the data register.
5. Which of the following is also known as tri-state?
a) output port
b) input port
c) parallel port
d) output-input port
View Answer
Answer: a
Explanation: The progression in the parallel ports provides a third register or an individual control bit which can make the pin in a high impedance state. An output port which can do this is also known as tri-state, that is, logic high, logic low and a high impedance state.
6. How buffers are enabled in the parallel ports?
a) by the data register
b) by data direction register
c) by individual control register
d) by data and individual control register
View Answer
Answer: b
Explanation: The implementation of parallel port uses a couple of buffers which are enabled by the data direction register by setting the corresponding bit of the register.
7. Which of the following registers offers high impedance?
a) data register

b) data direction register
c) individual control bit
d) data register and data direction register
View Answer
Answer: c
Explanation: The register which offers high impedance is the individual control bit or the third register which can be implemented by switching off both the buffers and putting their connections to the pin which offers high impedance.
8. Which of the following can be used as a chip select?
a) multifunction I/O port
b) parallel port
c) DMA port
d) memory port
View Answer
Answer: a
Explanation: The multifunction I/O port can also be used a chip select for the memory design. The function that the pin performs is set up internally through the use of a function register which internally configures how the external pins are connected internally.
9. Which of the following is necessary for the parallel input-output port?
a) inductor
b) pull-up resistor
c) push-up resistor
d) capacitor
View Answer
10. Which of the following can be described as general-purpose?
a) multifunction I/O port
b) input port
c) dma port
d) output port
View Answer

Answer: a

1. Which of the following helps in the generation of waveforms?
a) timer
b) inputs
c) outputs
d) memory
View Answer
Answer: a
Explanation: The embedded systems have a timing component called timer or counter which helps in the timing reference for control sequence, provides system tick for the operating system and also helps in the generation of waveforms for the serial port baud rate generation.
2. Which bit size determines the slowest frequency?
a) counter size
b) pre-scalar value
c) counter
d) timer
View Answer
Answer: b
Explanation: The pre-scalar value determines the slowest frequency that can be generated from a given clock input. Actually the bit size are determined by the pre-scalar value and the conuter size.
3. Which bit size determines the maximum value of the counter-derived period?
a) counter size
b) pre-scalar value
c) bit size
d) byte size
View Answer

Answer: a
Explanation: The bit size are basically determined by its fundamental properties, that is, the pre-scalar value and the counter size. The counter size determines the maximum value of the counter derived period.
4. Which of the following timer is suitable for IBM PC?
a) IA-32
b) Intel 8253
c) Intel 64
d) 8051 timer
View Answer
Answer: b
Explanation: The Intel 8253 timer is suitable for the IBM PC. IA-32 and Intel 64 are the offload timers used only for Intel. The 8051 timer is used for the timing program in 8051.
5. Which of the following is mode 0 in 8253?
a) interrupt on start count
b) interrupt for wait statement
c) interrupt on terminal count
d) no interrupt
View Answer
Answer: c
Explanation: The interrupt on the terminal count is known as mode 0 for the 8253. An initial value is loaded into the count register and then starts to count down at the frequency which is determined by the clock input. When the count reaches zero, an interrupt is generated.
6. Which determines the mode 1 in the Intel 8253?
a) interrupt on terminal count
b) programmable one-shot
c) rate generator
d) square wave rate generator
View Answer
Answer: b
Explanation: Programmable one-shot is also known as mode 1 in the Intel 8253. In mode 1, a single pulse with a

programmable duration is created first and then the pulse length is loaded into the counter and when the external gate signal is high, the rising edge starts the counter to count down to zero and the counter output signal goes high to start the external pulse. When the counter reaches to zero, the counter output goes low and thus the ending of the pulse.

7. Which mode of 8253 can provide pulse width modulation?

a) programmable one-shot
b) square wave rate generator
c) software triggered strobe
d) hardware triggered strobe

View Answer

Answer: a

Explanation: Mode 1 of the Intel 8253 can provide pulse width modulation for the power control where the gate is connected to a zero crossing detector or a clock source.

8. Which of the following is the mode 3 in the Intel timer 8253?

a) rate generator
b) hardware triggered strobe
c) square wave rate generator
d) software triggered strobe

View Answer

Answer: a

Explanation: The rate generator is the mode 3 in Intel 8253 timer. The square wave generator is the mode 4 and the hardware triggered strobe is the mode 5 in the Intel 8253 timer.

9. Which of the following determines the rate generation?

a) divide by N
b) multiply by N
c) addition by N
d) subtraction by N

View Answer

Answer: a

Explanation: The rate generator mode is determined by the mode 3 with the Intel 8253. It is a simple divide by N mode where N is the initial value loaded into the counter.

10. Which mode of the Intel 8253 timer can generate a square wave?
a) mode 1
b) mode 2
c) mode 3
d) mode 4
View Answer
Answer: d

1. Which mode of the Intel timer 8253 provides a software watchdog timer?
a) rate generator
b) hardware triggered strobe
c) square wave rate generator
d) software triggered strobe
View Answer
Answer: d
Explanation: The software triggered strobe can be used as a software-based watchdog timer in which the output is connected to a non maskable interrupt.
2. Which of the following mode is similar to the mode 4 of the 8253 timer?
a) mode 5
b) mode 6
c) mode 0
d) mode 1
View Answer
Answer: a
Explanation: The mode 5 or the hardware triggered strobe is similar to the mode 4 or the square wave rate generator expect that the retriggering is done by the external gate pin.
3. Which pin of 8253 is used for the generation of an external interrupt signal?
a) OUT pin

b) IN pin
c) Interrupt pin
d) Ready pin
View Answer
Answer: a
Explanation: The Intel 8253 timer has no interrupt pins. Therefore, the timer OUT pin is used to generate an external interrupt signal.
4. Which timer architecture can provide a higher resolution than Intel 8253?
a) Intel 8253
b) Intel 8254
c) 8051 timer
d) MC68230
View Answer
Answer: d
Explanation: The Intel 8253 and 8254 have same pin configuration and functions. 8051 timer is a programmable timer in the 8051 microcontroller. The MC68230 timer developed by Motorola can provide a powerful timer architecture which can provide higher resolution than the Intel 8253.
5. How many bit architecture does MC68230 have?
a) 16
b) 24
c) 32
d) 40
View Answer
Answer: b
Explanation: The MC68230 timer have a 24-bit architecture which is split into three 8-bit components because of the 8-bit bus in the MC68000 CPU.
6. How many bit bus does MC68230 have?
a) 2
b) 4
c) 8

d) 16
View Answer
Answer: c
Explanation: The MC68230 timer have a 24-bit architecture which is split into three 8-bit components because of the 8-bit bus which is used for the communication with the host processor like MC68000 CPU which have an 8-bit architecture.
7. Which of the following is a timer processor?
a) Intel 8253
b) MC146818
c) MC68332
d) Intel 8259
View Answer
Answer: c
Explanation: Intel 8253 and 8259 are timers or counters which supports the processors. MC146818 is a real-time clock. MC68332 which is developed by Motorola is a 32 bit timer processor which can support MC68020.
8. What is the running frequency of MC68332?
a) 12 MHz
b) 14 MHz
c) 16 MHz
d) 18 MHz
View Answer
Answer: c
Explanation: The running frequency of the MC68332 is 16 MHz.
9. Which of the following is a real time clock?
a) MC146818
b) 8253
c) 8259
d) 8254
View Answer
Answer: a

1. Which of the following is the pin efficient method of communicating between other devices?
a) serial port
b) parallel port
c) peripheral port
d) memory port
View Answer
Answer: a
Explanation: The serial ports are considered to be the pin efficient method of communication between other devices within an embedded system.
2. Which of the following depends the number of bits that are transferred?
a) wait statement
b) ready statement
c) time
d) counter
View Answer
Answer: c
Explanation: The time taken for the data transmission within the system depends on the clock frequency and the number of bits that are transferred.
3. Which of the following is the most commonly used buffer in the serial porting?
a) LIFO
b) FIFO
c) FILO
d) LILO
View Answer
Answer: b
Explanation: Most of the serial ports uses a FIFO buffer so that the data is not lost. The FIFO buffer is read to receive the data, that is, first in first out.

4. What does SPI stand for?
a) serial parallel interface
b) serial peripheral interface
c) sequential peripheral interface
d) sequential port interface
View Answer
Answer: b
Explanation: The serial parallel interface bus is a commonly used interface which involves master slave mechanism. The shift registers are worked as master and the slave devices are driven by a common clock.
5. Which allows the full duplex synchronous communication between the master and the slave?
a) SPI
b) serial port
c) I2C
d) parallel port
View Answer
Answer: a
Explanation: The serial peripheral interface allows the full duplex synchronous communication between the master and the slave devices. MC68HC05 developed by Motorola uses SPI for interfacing the peripheral devices.
6. Which of the following processor uses SPI for interfacing?
a) 8086
b) 8253
c) 8254
d) MC68HC11
View Answer
Answer: d
Explanation: The MC68HC05 and MC68HC11 microcontrollers use the serial peripheral interface for the peripheral interfacing.
7. In which register does the data is written in the master device?
a) index register
b) accumulator
c) SPDR

d) status register
View Answer
Answer: c
Explanation: The serial peripheral interface follows a master slave mechanism in which the data is written to the SPDR register in the master device and clocked out into the slave device SPDR by using a common clock signal called SCK.
8. What happens when 8 bits are transferred in the SPI?
a) wait statement
b) ready statement
c) interrupt
d) remains unchanged
View Answer
Answer: c
Explanation: The interrupts are locally generated when 8-bits are transferred so that the data can be read before the next byte is clocked through.
9. Which signal is used to select the slave in the serial peripheral interfacing?
a) slave select
b) master select
c) interrupt
d) clock signal
View Answer
Answer: a
Explanation: The slave select signal selects which slave is to receive data from the master.
10. How much time period is necessary for the slave to receive the interrupt and transfer the data?
a) 4 clock time period
b) 8 clock time period
c) 16 clock time period
d) 24 clock time period
View Answer
Answer: b

1. What does I2C stand for?
a) inter-IC
b) intra-IC
c) individual integrated chip
d) intel IC
View Answer
Answer: a
Explanation: The I2C is known as inter-IC, which is developed by Philips for interfacing with the peripheral devices.
2. Which company developed I2C?
a) Intel
b) Motorola
c) Phillips
d) IBM
View Answer
Answer: c
Explanation: The I2C is developed by Philips for use within the television sets.
3. Which of the following is the most known simple interface?
a) I2C
b) Serial port
c) Parallel port
d) SPI
View Answer
Answer: a
Explanation: The I2C is the most known simple interface which is used currently. It can combine both the hardware and the software protocols to provide a bus interface which helps in the communication with many peripherals.
4. Which are the two lines used in the I2C?
a) SDA and SPDR
b) SPDR and SCL
c) SDA and SCL

d) SCL and status line
View Answer
Answer: c
Explanation: The I2C bus consists of two lines which are called SDA and SCL. The master and slave devices are attached to these lines.
5. Which of the following developed P82B715?
a) Philips
b) Intel
c) IBM
d) Motorola
View Answer
Answer: a
Explanation: The special buffer chip, P82B715 for increasing the current drive is developed by Philips.
6. Which pin provides the reference clock for the transfer of data?
a) SDA
b) SCL
c) SPDR
d) Interrupt pin
View Answer
Answer: b
Explanation: The SCL pin can provide the reference clock for the transmission of data but it is not a free running clock.
7. Which of the following are the three hardware signals?
a) START, STOP, ACKNOWLEDGE
b) STOP, TERMINATE, END
c) START, SCL, SDA
d) STOP, SCL, SDA
View Answer

Answer: a
Explanation: The three hardware signals are START, STOP and ACKNOWLEDGE. These signals help in the transmission of data between the slave and the masters.
8. Which of the following performs the START signal?
a) master
b) slave
c) CPU
d) memory
View Answer
Answer: a
Explanation: The START signal is performed by the master by making the SCL and SDA pin high.
9. Which of the following are handshake signals?
a) START
b) STOP
c) ACKNOWLEDGE
d) START and STOP
View Answer
Answer: c
Explanation: The START signal and ACKNOWLEDGE signals are almost similar but there exhibits a small change. The START signal is initiated by the master only but the ACKNOWLEDGE signal is a handshake between both the master and slave.
10. A packet is also referred to as
a) postcard
b) telegram
c) letter
d) data
View Answer
Answer: b
Explanation: The data is transmitted in packets with a having one or more bytes. These packets of data are also known as a telegram.

11. Which of the following byte performs the slave selection?
a) first byte
b) second byte
c) terminal byte
d) eighth byte
View Answer
Answer: a

1. Which of the following indicates the type of operation that the master requests?
a) address value
b) initial value
c) terminal count
d) first byte
View Answer
Answer: a
Explanation: The address value helps the master to select the device and indicates what operation should be taken. If the 8th bit is logic one, read operation takes out and if it is logic zero, write operation takes out.
2. How can both single byte and the double byte address slave use the same bus?
a) extended memory
b) extended address
c) peripheral count
d) slave bus
View Answer
Answer: b
Explanation: For providing more addressing, an extended address is developed which possesses two bytes in which the first byte uses a special code to distinguish it from a single byte address so that the single byte and double byte address slaves can use a shared bus.

3. Which counter selects the next register in the I2C?
a) auto-incrementing counter
b) decrementing counter
c) auto-decrementing counter
d) terminal counter
View Answer
Answer: a
Explanation: The peripheral having a small number of locations can use auto-incrementing counter for accessing the next register. But this will not be applicable in bigger memory devices.
4. Which is an efficient method for the EEPROM?
a) combined format
b) auto-incrementing counter
c) register set
d) single format
View Answer
Answer: a
Explanation: Combined format is an efficient method for the EEPROM because it is having a large number of registers.
5. Which of the following uses two data transfers?
a) auto-incrementing counter
b) auto-decrementing counter
c) combined format
d) single format
View Answer
Answer: c
Explanation: The EEPROM is having a large number of registers, so auto incrementing counter will not be applicable. So there is an alternative method which uses index value that is written to the chip, prior to accessing the data. This is called combined format and this combined format uses two data transfer. One is to write the data and the other is to read.
6. Which of the following is efficient for the small number of registers?
a) auto-incrementing counter
b) auto-decrementing counter

c) combined format
d) single format
View Answer
Answer: a
Explanation: The peripherals which have a small number of locations can use auto-increment counter within the peripheral in which each access selects the next register.
7. Which can determine the timeout value?
a) polling
b) timer
c) combined format
d) watchdog timer
View Answer
Answer: a
Explanation: The polling can be used along with the counter to determine the timeout value.
8. How is bus lockup avoided?
a) timer and polling
b) combined format
c) terminal counter
d) counter
View Answer
Answer: a
Explanation: The timeout value can be changed by the peripheral devices, so for a sophisticated system a combination of polling and timer is used to check for the signal n times within a predefined interval. This can avoid the bus lock.
9. Which of the following can determine if two masters start to use the bus at the same time?
a) counter detect
b) collision detect
c) combined format
d) auto-incremental counter
View Answer

Answer: b
Explanation: The collision detects technique helps to determine whether two or more masters are using the same bus in a multi-master device.
10. Which ports are used in the multi-master system to avoid errors?
a) unidirectional port
b) bidirectional port
c) multi directional port
d) tridirectional port
View Answer
Answer: b

1. Which of the following is the pin efficient method of communicating between other devices?
a) serial port
b) parallel port
c) peripheral port
d) memory port
View Answer
Answer: a
Explanation: The serial ports are considered to be the pin efficient method of communication between other devices within an embedded system.
2. Which of the following depends the number of bits that are transferred?
a) wait statement
b) ready statement
c) time
d) counter
View Answer

Answer: c
Explanation: The time taken for the data transmission within the system depends on the clock frequency and the number of bits that are transferred.
3. Which of the following is the most commonly used buffer in the serial porting?
a) LIFO
b) FIFO
c) FILO
d) LILO
View Answer
Answer: b
Explanation: Most of the serial ports uses a FIFO buffer so that the data is not lost. The FIFO buffer is read to receive the data, that is, first in first out.
4. What does SPI stand for?
a) serial parallel interface
b) serial peripheral interface
c) sequential peripheral interface
d) sequential port interface
View Answer
Answer: b
Explanation: The serial parallel interface bus is a commonly used interface which involves master slave mechanism. The shift registers are worked as master and the slave devices are driven by a common clock.
5. Which allows the full duplex synchronous communication between the master and the slave?
a) SPI
b) serial port
c) I2C
d) parallel port
View Answer
Answer: a
Explanation: The serial peripheral interface allows the full duplex synchronous communication between the master and the slave devices. MC68HC05 developed by Motorola uses SPI for interfacing the peripheral devices.

6. Which of the following processor uses SPI for interfacing?
a) 8086
b) 8253
c) 8254
d) MC68HC11
View Answer
Answer: d
Explanation: The MC68HC05 and MC68HC11 microcontrollers use the serial peripheral interface for the peripheral interfacing.
7. In which register does the data is written in the master device?
a) index register
b) accumulator
c) SPDR
d) status register
View Answer
Answer: c
Explanation: The serial peripheral interface follows a master slave mechanism in which the data is written to the SPDR register in the master device and clocked out into the slave device SPDR by using a common clock signal called SCK.
8. What happens when 8 bits are transferred in the SPI?
a) wait statement
b) ready statement
c) interrupt
d) remains unchanged
View Answer
Answer: c
Explanation: The interrupts are locally generated when 8-bits are transferred so that the data can be read before the next byte is clocked through.
9. Which signal is used to select the slave in the serial peripheral interfacing?
a) slave select
b) master select
c) interrupt

d) clock signal
View Answer
Answer: a
Explanation: The slave select signal selects which slave is to receive data from the master.
10. How much time period is necessary for the slave to receive the interrupt and transfer the data?
a) 4 clock time period
b) 8 clock time period
c) 16 clock time period
d) 24 clock time period
View Answer
Answer: b

1. Which of the following can be used for long distance communication?
a) I2C
b) Parallel port
c) SPI
d) RS232
View Answer
Answer: d
Explanation: A slightly different serial port called RS232 is used for long distance communication, otherwise the clock may get skewed. The low voltage signal also affects the long distance communication.
2. Which of the following can affect the long distance communication?
a) clock
b) resistor
c) inductor
d) capacitor
View Answer
Answer: a
Explanation: For small distance communication, the clock signal which allows a synchronous transmission of data is more than

enough, and the low voltage signal of TTL or CMOS is sufficient for the operation. But for long distance communication, the clock signal may get skewed and the low voltage can be affected by the cable capacitance. So for long distance communication RS232 can be used.

3. Which are the serial ports of the IBM PC?

a) COM1

b) COM4 and COM1

c) COM1 and COM2

d) COM3

View Answer

Answer: c

Explanation: The IBM PC has one or two serial ports called the COM1 and the COM2, which are used for the data transmission between the PC and many other peripheral units like a printer, modem etc.

4. Which of the following can provide hardware handshaking?

a) RS232

b) Parallel port

c) Counter

d) Timer

View Answer

Answer: a

Explanation: In RS232, several lines are used for transmitting and receiving data and these also provide control for the hardware handshaking.

5. Which of the following have an asynchronous data transmission?

a) SPI

b) RS232

c) Parallel port

d) I2C

View Answer

Answer: b

Explanation: The data is transmitted asynchronously in RS232 which enhance long distance communication, whereas SPI, I2C offers short distance communication, and therefore, they are using synchronous data transmission.

6. How many areas does the serial interface have?
a) 1
b) 3
c) 2
d) 4
View Answer
Answer: c
Explanation: The serial interface is divided into two, physical interface and the electrical interface.
7. The RS232 is also known as
a) UART
b) SPI
c) Physical interface
d) Electrical interface
View Answer
Answer: d
Explanation: The RS232 is also known as the physical interface and it is also known as EIA232.

8. How much voltage does the MC1489 can take?
a) 12V
b) 5V
c) 3.3V
d) 2.2V
View Answer
Answer: b
Explanation: The MC1489 is an interface chip which can take a 5V and generate internally the other voltages which are needed to meet the interface specification.
9. Which of the following is not a serial protocol?
a) SPI
b) I2C
c) Serial port

d) RS232
View Answer
Answer: d
Explanation: The RS232 is a physical interface. It does not follow the serial protocol.
10. Which of the following is an ideal interface for LCD controllers?
a) SPI
b) parallel port
c) Serial port
d) M-Bus
View Answer
Answer: d

1. What does UART stand for?
a) universal asynchronous receiver transmitter
b) unique asynchronous receiver transmitter
c) universal address receiver transmitter
d) unique address receiver transmitter
View Answer
Answer: a
Explanation: The UART or universal asynchronous receiver transmitter is used for the data transmission at a predefined speed or baud rate.
2. How is data detected in a UART?
a) counter
b) timer
c) clock
d) first bit
View Answer

Answer: c
Explanation: The data can be detected by the local clock reference which is generated from the baud rate generator.
3. Which of the signal is set to one, if no data is transmitted?
a) READY
b) START
c) STOP
d) TXD
View Answer
Answer: d
Explanation: The TXD signal goes to logic one when no data is transmitted. When data transmit, it sets to logic zero.
4. What rate can define the timing in the UART?
a) bit rate
b) baud rate
c) speed rate
d) voltage rate
View Answer
Answer: b
Explanation: The timing is defined by the baud rate in which both the transmitter and receiver are used. The baud rate is supplied by the counter or an external timer called baud rate generator which generates a clock signal.
5. How is the baud rate supplied?
a) baud rate voltage
b) external timer
c) peripheral
d) internal timer
View Answer
Answer: b
Explanation: The baud rate is supplied by the counter or an external timer called baud rate generator which generates a clock signal.
6. Which is the most commonly used UART?
a) 8253

b) 8254
c) 8259
d) 8250
View Answer
Answer: d
Explanation: The Intel 8253, 8254 and 8259 are timers whereas Intel 8250 is a UART which is commonly used.
7. Which company developed 16450?
a) Philips
b) Intel
c) National semiconductor
d) IBM
View Answer
Answer: c
8. What does ADS indicate in 8250 UART?
a) address signal
b) address terminal signal
c) address strobe signal
d) address generating signal
View Answer
Answer: c

9. Which of the following signals are active low in the 8250 UART?
a) BAUDOUT
b) DDIS
c) INTR
d) MR
View Answer
Answer: a

10. Which of the signal can control bus arbitration logic in 8250?
a) MR
b) DDIS
c) INTR
d) RCLK

Answer: b

1. Which of the following is used to reset the device in 8250?
a) MR
b) DDIS
c) INTR
d) RCLK
View Answer
Answer: a
Explanation: MR is the master reset pin which helps to reset the device and restore the internal registers.
2. Which provides an input clock for the receiver part of the UART 8250?
a) RD
b) RCLK
c) MR
d) DDIS
View Answer
Answer: b
Explanation: RCLK provides an input clock for the receiver part of the UART. RD is the read signal. MR is the master reset pin and DDIS is used to control bus arbitration logic.
3. Which of the following is a general purpose I/O pin?
a) OUT1
b) RD
c) ADS

d) MR
View Answer
Answer: a
Explanation: There are two general purposes I/O pin OUT1 and OUT2. OUT1 is set by the programming bit 2 of the MCR to a ‘1’ whereas OUT2 is set by the programming bit 3 of the MCR to ‘1’. These are active low pins in 8250.
4. Which of the following indicate the type of access that the CPU needs to perform?
a) MR
b) RD
c) ADS
d) RCLK
View Answer
Answer: b
Explanation: RD and WR signals are indicating the type of access that the CPU needs to perform, that is, whether it is a read cycle or write cycle.
5. Which pins are used for additional DMA control?
a) RXRDY
b) RD
c) MR
d) INR
View Answer
Answer: a
Explanation: The RXRDY and TXRDY are two active low pins which are used for additional DMA control. It can be used for DMA transfers to and from the read and write buffers.
6. Which of the following are not used within the IBM PC?
a) TXRDY
b) BAUDOUT
c) ADS
d) OUT2
View Answer

Answer: a
Explanation: The CPU is responsible for moving data to and from the UART in the IBM PC, therefore it does not have TXRDY and RXRDY pins which are used for DMA accessing.
7. Which pins are used to connect an external crystal?
a) INR
b) ADS
c) XIN
d) SIN
View Answer
Answer: c
Explanation: The XIN and XOUT pins are used to connect an external crystal. These pins can also connect an external clock.
8. Which UART is used in MC680 by 0 design?
a) Intel 8250
b) 16450
c) 16550
d) MC68681
View Answer
Answer: d
Explanation: The MC68681 is a standard UART developed by Motorola. It has been used in many MC680 by 0 designs.
9. Which of the following have large FIFO buffer?
a) 8253
b) 8250
c) 16550
d) 16450
View Answer
Answer: c
Explanation: The largest buffer of 16 bytes is available on 16550 UART which is used for high speed data communications.
10. Which of the following has a quadruple buffered receiver and a double buffered transmitter?
a) Intel 8250
b) 16450

c) 16550
d) MC68681
View Answer
Answer: d

1. Which can prevent the terminal of data transmission?
a) flow control
b) increasing flow
c) increasing count
d) terminal count
View Answer
Answer: a
Explanation: The flow control can prevent data transmission. It can also prevent the computer from sending more data than the other can cope with.
2. Which of the following is the first flow control method?
a) software handshaking
b) hardware handshaking
c) UART
d) SPI
View Answer
Answer: b
Explanation: The first flow control method is the hardware handshaking in which the hardware in the UART detects the potential overrun and it will assert a handshake line to tell the other UART to stop the transmission.
3. Which one of the following is the second method for flow controlling?
a) hardware
b) peripheral
c) software

d) memory
View Answer
Answer: c
Explanation: In the first method of flow control, there is a chance of data loss. So the second method of the flow control is adopted in which it uses software to send characters XON and XOFF. XOFF can stop the data transfer and XON can restart the data transfer.
4. Which can restart the data transmission?
a) XON
b) XOFF
c) XRST
d) restart button
View Answer
Answer: a
Explanation: The second method of flow control is called software which is based on certain characters called XON and XOFF. XOFF can stop the data transfer and XON can restart the data transfer.
5. Which of the following is a common connector?
a) UART
b) SPI
c) I2C
d) DB-25
View Answer
Answer: d
Explanation: There are two connectors which are used very commonly. They are DB-25 and DB-9 which has 25 pins and 9 pins respectively.
6. What does pin 22 in DB-25 indicate?
a) transmit data
b) receive data
c) ring indicator

d) signal ground
View Answer
Answer: c
Explanation: The 22nd pin in DB-25 and the 9th pin in the DB-9 indicates a ring indicator which is asserted when a connected modem has detected an incoming call.
7. Which pin indicates the DSR in DB-25?
a) 1
b) 2
c) 4
d) 6
View Answer
Answer: d
Explanation: The 6th pin in DB-25 indicates DSR, that is, data set ready which indicates that each side is powered on and is ready to access data.
8. Which of the following connections are one to one?
a) Modem cables
b) SPI
c) UART
d) I2C
View Answer
Answer: a
Explanation: The modem cables are straight cables which allow one to one connections without crossover.
9. Which of the following are used to link PCs?
a) modem cable
b) null modem cable
c) serial port
d) parallel port
View Answer

Answer: b
Explanation: The modem cables are used to link PC with other peripherals like printers, plotters, modems etc. But it cannot link with other PCs. So an alternative method is adopted to link PCs which is called null modem cable.

10. Which of the following method is used by Apple Macintosh?
a) hardware handshaking
b) software handshaking
c) no handshaking
d) null modem cable
View Answer
Answer: b

1. Which of the following provides an efficient method for transferring data from a peripheral to memory?
a) dma controller
b) serial port
c) parallel port
d) dual port
View Answer
Answer: a
Explanation: The DMA controllers or direct memory access controller provides an efficient method for transferring data from the peripheral to the memory.
2. Which of the following can be adopted for the systems which does not contain DMA controller for data transmission?
a) counter
b) timer
c) polling
d) memory
View Answer

Answer: c
Explanation: The polling and interrupt helps for data transmission for the systems which do not have DMA controller.
3. Which of the following have low-level buffer filling?
a) output
b) peripheral
c) dma controller
d) input
View Answer
Answer: c
Explanation: The DMA controller can initiate and control the bus access between I/O devices and memory, and also between two different memory areas. Therefore, the DMA controller can act as a hardware implementation of low-level buffer filling or emptying the interrupt.
4. How many classifications of DMA controllers are made based on the addressing capability?
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: b
Explanation: There are three classifications for the DMA controllers based on the address capability. These are 1D, 2D and 3D.
5. How many address register are there for the 1D type DMA controller?
a) 1
b) 2
c) 3
d) 4
View Answer
Answer: a
Explanation: The 1D controller only have a single address register whereas 2D controller have two address register and 3D controller have three or more address register.

6. Which of the following of a generic DMA controller contain a base address register and an auto-incrementing counter?
a) address bus
b) data bus
c) bus requester
d) address generator
View Answer
Answer: d
Explanation: The generic controller have several components associated with it for controlling the operation and one such is the address generator. It consists of the base address register and an auto-incrementing counter which increment the address after every transfer.
7. Which of the following is used to transfer the data from the DMA controller to the destination?
a) data bus
b) address bus
c) request bus
d) interrupt signal
View Answer
Answer: a
Explanation: The data bus is used for the transmission of data from the DMA controller to the destinal. The DMA controller can directly select the peripheral in some cases in which the data transfer is made from the peripheral to the memory.
8. Which of the following is used to request the bus from the main CPU?
a) data bus
b) address bus
c) bus requester
d) interrupt signal
View Answer
Answer: c
Explanation: The bus requester requests the bus from the main CPU. In earlier design, the processor bus does not support the multi master system and there were no bus request signals. In such cases, the processor clock was extended.
9. Which signal can identify the error?
a) data bus

b) address bus
c) bus requester
d) interrupt signal
View Answer
Answer: d
Explanation: The interrupt signal can identify the error occurred in the DMA controller. This makes the processor to reprogram the DMA controller for a different transfer.
10. Which signal allows the DMA controller to select the peripheral?
a) local peripheral control
b) global peripheral control
c) address bus
d) data bus
View Answer
Answer: a

1. Which of the following is also known as implicit address?
a) dual address model
b) single address model
c) 1D model
d) 2D model
View Answer
Answer: b
Explanation: The single address model is also known as implicit model because the second address is implied and is not directly given, that is, the source address is not supplied.
2. Which address mode uses two addresses and two accesses to transfer the data between the peripheral and the memory?
a) dual address model
b) 1D model
c) 2D model

d) 3D model
View Answer
Answer: a
Explanation: The dual address mode supports two addresses and two accesses for transferring data between a peripheral or memory and another memory location.
3. Which of the following address mode uses a buffer to hold data temporarily?
a) 1D model
b) 2D model
c) dual address model
d) 3D model
View Answer
Answer: c
Explanation: The dual address mode supports two addresses and two accesses for transferring data between a peripheral or memory and another memory location, which also consumes two bus cycles and a buffer within the DMA controller to hold data temporarily.
4. Which of the following model can implement a circular buffer?
a) dual address mode
b) 1D model
c) 2D model
d) 3D model
View Answer
Answer: b
Explanation: The 1D model can implement a circular buffer which makes an automatic reset to bring the address back to the beginning.
5. Which of the following uses an address and a counter to define the sequence of addresses?
a) dual address mode
b) 2D model
c) 1D model

d) 3D model
View Answer
Answer: c
Explanation: The 1D model of the DMA controller uses an address location and a counter to define the address sequence which is used during the DMA cycles.
6. Which of the following is used to calculate an offset to base address?
a) single address mode
b) dual address mode
c) 1D model
d) 2D model
View Answer
Answer: d
Explanation: An address stride is specified which can be used for calculating the offset to the base address at the terminal of count. This address stride is used in the 2D model of the DMA controller.
7. Which can provide an address stride?
a) single address mode
b) dual address mode
c) 1D model
d) 2D model
View Answer
Answer: d
Explanation: In the 2D model of the DMA controller, an address stride is specified which can be used for calculating the offset to the base address at the terminal of count.
8. How is the count register can be splitted?
a) 2
b) 3
c) 4
d) 5
View Answer

Answer: a
Explanation: In the 2D model of the DMA controller, in addition to the address stride there is a count register which can be split into two, in which one register is used to specify the count for the block and the second register is used to define the total number of blocks or the bytes to be transferred.
9. Which of the following has the ability to change the stride automatically?
a) 1D model
b) 2D model
c) 3D model
d) dual address mode
View Answer
Answer: c
Explanation: In the 3D model of the DMA controller, it have the ability to change the address stride automatically so that blocks of different sizes and stride can be created.
10. Which is used to prioritise multiple requests?
a) dual address mode
b) single address mode
c) arbitration
d) chaining
View Answer
Answer: c

1. Which of the following DMA is used in the IBM PC?
a) Intel 8253
b) Intel 8254
c) Intel 8237
d) Intel 8259
View Answer
Answer: c
Explanation: The Intel 8237 is the DMA used in the IBM PC. 8253, 8254 and 8259 are timers developed by Intel.

2. Which of the following have four transfer modes?
a) Intel 8253
b) Intel 8254
c) Intel 8259
d) Intel 8237
View Answer
Answer: d
Explanation: The Intel 8237 have four transfer modes. These are single mode, block transfer mode, demand mode and cascade mode.
3. Identify the additional transfer mode in the Intel 8237?
a) single transfer mode
b) demand transfer mode
c) verify transfer mode
d) block transfer mode
View Answer
Answer: c
Explanation: In addition to the four main transfer mode, there is a verify transfer mode which is used within the PC to create dummy addresses which are used for refreshing the DRAM.
4. Which of the following transfer mode can refresh the DRAM memory?
a) verify transfer mode
b) bloch transfer mode
c) demand transfer mode
d) cascade mode
View Answer
Answer: a
Explanation: The verify address transfer mode can generate dummy addresses which are used for the DRAM refreshing.
5. Which of the following is used for supporting the priority scheme?
a) address transfer mode
b) arbitration
c) counter

d) timer
View Answer
Answer: b
Explanation: The arbitration is used for providing priority to the DMA requests. The DMA request is simultaneously generating, so in order to avoid the errors, a priority scheme is necessary which is done by the arbitration scheme in the DMA controller.
6. Which of the following consist of a fully programmable DMA controller of two channels?
a) MC68300
b) Intel 8237
c) Intel 8253
d) Intel 8254
View Answer
Answer: a
Explanation: The MC68300 is developed by Motorola, which consists of a two channel fully programmable DMA controller which can support high speed data transfer.
7. Which cycle can support the burst and single transfer mode?
a) internal
b) external
c) both internal and external
d) address cycle
View Answer
Answer: b
Explanation: The internal cycles can be programmed to occupy the partial or complete fulfillment of the available internal bus bandwidth while the external cycles provides support to the single transfer modes and burst mode.
8. Which of the following requires its own local memory and program?
a) DMA controller
b) DMA address
c) DMA CPU
d) DMA peripheral
View Answer

Answer: c
Explanation: The DMA CPU has its own address local memory and program so that it will not harm main memory bus and it is completely isolated.
9. Which DMA is programmed with higher level software?
a) DMA controller
b) DMA address
c) DMA peripheral
d) DMA CPU
View Answer
Answer: d
Explanation: The DMA CPU is programmed with higher level software which is used to transfer the data and for processing it.
10. Which of the following combine an MC68000/MC68020 type of processor with peripheral and DMA controllers?
a) Intel 8237
b) Intel 8253
c) MC68300
d) MC68000
View Answer
Answer: c

1. Which signal is sampled at regular intervals for the purpose of ADC?
a) analog signal
b) digital signal
c) quantised signal
d) sampled signal
View Answer
Answer: a
Explanation: The analog signal is sampled at regular intervals for the analog to digital conversion. Each sample is then quantised to divided by a given value in order to identify the number of approximate analogue value.

2. Which factor depends on the quantisation error?
a) number of error
b) number of bits
c) size of error
d) conversion process
View Answer
Answer: b
Explanation: The quantisation error depends on the number of bits which is used to represent the analogue vale.
3. Which is the first type of error caused during the conversion process?
a) sampling error
b) interrupt signal
c) counter error
d) quantisation error
View Answer
Answer: d
Explanation: The quantisation error is the first type of error caused in the conversion process. This error is caused because the samples are converted to a slightly higher value instead of zero.
4. Which of the following defines the number of samples that are taken in the time period?
a) sample size
b) sample nature
c) sample rate
d) sample frequency
View Answer
Answer: c
Explanation: The sample rate is defined by the number of samples that are taken in a time period. The sample rate is usually measured in Hertz. It can determine the speed of the conversion device itself.
5. Which of the following can determine the speed of conversion device itself?
a) sample rate
b) sampled data
c) sample size

d) sample nature
View Answer
Answer: a
Explanation: The sample rate determines the various aspect of the conversion process and one such is the conversion speed.
6. Which of the following can determine the maximum frequency that can be converted?
a) sample frequency
b) sample rate
c) sample size
d) sample nature
View Answer
Answer: b
Explanation: The sample rate can determine the maximum frequency that can be converted as per the Nyquist theorem. The theorem states that the minimum sampling rate frequency should be twice the maximum frequency of the analog signal.
7. Which term determines the random timing error?
a) jitter
b) quantisation error
c) sample error
d) delay
View Answer
Answer: a
Explanation: Jitter is a random timing error. Jitter can cause irregular sampling errors.
8. Which of the following introduce a phase error?
a) conversion time
b) sampling rate
c) sample size
d) sample nature
View Answer

Answer: a
Explanation: The conversion time always introduces a phase error. The conversion time will delay the digital output and hence introduce a phase error.
9. Which of the following can generate an interrupt?
a) timer
b) trigger
c) delay
d) counter
View Answer
Answer: a
Explanation: The timer can generate an interrupt to the processor at the rate of sampling frequency.
10. Which filter is used for filtering out the high frequency components?
a) bandpass filter
b) band reject filter
c) analogue filter
d) digital filter
View Answer
Answer: c
Explanation: The higher frequency components can be filtered out by using an analog filter after sampling.
11. Which theorem describes the sampling rate with the frequency of the analogue signal?
a) Nyquist theorem
b) Bayes theorem
c) Sampling theorem
d) Parseval's theorem
View Answer
Answer: a

1. From which of the following words does codecs is derived?
a) coder

b) decoder
c) coder-decoder
d) coder-encoder
View Answer
Answer: c
Explanation: The codec is derived coder-decoder and is coupled to perform the coding. It can support both analogue to digital conversion and digital to analogue conversion.
2. Which codec is used in digital audio?
a) A-law
b) μ-law
c) linear
d) PCM
View Answer
Answer: c
Explanation: In the linear codec, the relationship between the analogue and digital values are linear. This method is commonly used in digital audio communication.
3. Which of the following have the same quantisation step throughout the range?
a) linear
b) PCM
c) DPCM
d) ADPCM
View Answer
Answer: a
Explanation: The quantisation step is same throughout the dynamic range in the linear codec and thus any increase in the analogue value increases the digital value, that is, the overall performance is linear.
4. Which is used in the telecommunication applications which has a limited bandwidth of 300 to 3100 HZ?
a) linear codec
b) logarithmic codec
c) PCM

d) DPCM
View Answer
Answer: b
Explanation: The logarithmic codec is frequently used in the telecommunication system which have a limited bandwidth of 300 to 3100 Hz. this can provide an 8-bit sample at 8 KHz, which are used in the telephones. The commonly used are A-law and μ-law.
5. Which codec is used in the UK?
a) a-law
b) μ-law
c) linear codec
d) PCM
View Answer
Answer: a
Explanation: The a-law is a logarithmic codec which is commonly used in the UK whereas μ-law is used in the US.
6. What does PCM stand for?
a) pulse codec machine
b) pulse code modulation
c) peripheral code machine
d) peculiar code modulation
View Answer
Answer: b
Explanation: The linear codec is also known as pulse code modulation which is commonly used in the telecommunications industry.
7. Which of the following conversion is performed by using a lookup table?
a) DPCM
b) ADPCM
c) Between DPCM and ADPCM
d) Linear cdec and a-law
View Answer

Answer: d
Explanation: The conversion between a-law/μ-law and a linear digital signal or between μ-law and a-law is performed by a lookup table.
8. What does DPCM stand for?
a) differential pulse code modulation
b) data pulse code modulation
c) dynamic pulse code machine
d) dynamic pulse code modulation
View Answer
Answer: a
Explanation: The differential pulse code modulation is similar to pulse code modulation, but DPCM uses an encoded value which is the difference between the current and the previous sample.
9. Which of the following have a 16-bit digital dynamic range?
a) PCM
b) DPCM
c) linear codec
d) logarithmic codec
View Answer
Answer: b
Explanation: The differential pulse code modulation can improve the accuracy and resolution by having a 16-bit dynamic range. It works by the increasing dynamic range.
10. How many types of logarithmic codecs are used commonly?
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: a
Explanation: There are two types of logarithmic codec which are commonly used. They are a-law which is used in UK and μ-law codec which is used in the US.

11. What does ADPCM stand for?
a) address differential pulse code modulation
b) adaptive differential pulse code modulation
c) address dynamic pulse code machine
d) adaptive dynamic pulse code modulation
View Answer
Answer: b
Explanation: The adaptive differential pulse code modulation is used in telecommunications and is based on non-linear quantisation values.
12. Which of the following uses a non-linear quantisation value?
a) PCM
b) DPCM
c) ADPCM
d) linear codec
View Answer
Answer: c
Explanation: The adaptive differential pulse code modulation is based on non-linear quantisation values. In the ADPCM, instead of using all bit for encoding, only a few bits are used for encoding which makes it non linear.
13. Which of the following works by increasing the dynamic range?
a) logarithmic codec
b) linear codec
c) DPCM
d) PCM
View Answer
Answer: c
Explanation: The differential pulse code modulation can improve the accuracy and resolution by having a 16-bit dynamic range. It works by the increasing dynamic range.
14. Which device can make the PWM operation easier?
a) timer
b) software

c) hardware
d) transistor
View Answer
Answer: a

1. Which of the following can be used for providing high gain?
a) transistor
b) darlington transistor pair
c) resistor
d) capacitor
View Answer
Answer: b
Explanation: The darlington pair of transistors can provide high gain than a single transistor. This is one of the method used to avoid voltage mismatches that the system produces. By using high gain transistors the voltage mismatches can be reduced upto a limit.
2. Which devices have high drive capability?
a) transistor
b) fet
c) buffer pack
d) darlington amplifier
View Answer
Answer: c
Explanation: The buffer pack is used to avoid the voltage mismatches which possesses a high drive capacity and it can also provide high drive currents than the normal logic outputs.
3. Which of the following is used to switch heavy loads?
a) fet
b) transistor
c) buffer pack

d) darlington pair
View Answer
Answer: a
Explanation: The field effect transistor can be used to provide a very high effective gain and hence they can be used to switch heavy loads easily from a logic device. These are also voltage controlled transistors.
4. Which allows the switching of DC motor by using two outputs and four FETs?
a) transistor
b) H bridge
c) darlington pair
d) buffer pack
View Answer
Answer: b
Explanation: The H bridge can be created by using several switches which allows a DC motor to be switched on and reversed in the direction. The switching can be done by using two outputs and four FETs.
5. Which of the following is used to create H bridge?
a) switches
b) led
c) capacitor
d) inductor
View Answer
Answer: a
Explanation: The H bridge can be created by using several switches. This allows a DC motor to be switched on and reversed in the direction and the switching of DC motor can be done by using two outputs and four FETs.
6. Which of the following allows voltage reversing?
a) H bridge
b) Relays
c) LEDs
d) LCDs
View Answer

Answer: a
Explanation: The H bridge is used in controlling DC motors or any other loads which need voltage reversing.
7. Which devices are used as indicators in a digital system?
a) LCD
b) LED
c) Varactor diode
d) Gunn diode
View Answer
Answer: b
Explanation: The light emitting diodes are used as indicators in the digital system and can be directly driven from a logic output.
8. How is the biasing done in LEDs?
a) forward bias
b) no bias
c) supply voltage
d) reverse bias
View Answer
Answer: d
Explanation: The LEDs will light up only when the diode reverse breakdown is achieved. It is usually about 2 to 2.2V.
9. Which of the following determines the brightness of LEDs?
a) current
b) voltage
c) resistance
d) conductance
View Answer
Answer: a
Explanation: The current drive determines the brightness of the LEDs and it is usually associated with a current limiting resistor in series with the LED to prevent the overheating.
10. Which of the following is a current limiting device?
a) voltage
b) current

c) buffer
d) inductor
View Answer
Answer: c
Explanation: A buffer can be used as a current limiting device. Similarly, a transistor can also be used as a current limiting device.
11. Which of the following can switch the current by a make or break contact?
a) transistor
b) relay
c) buffer
d) fet
View Answer
Answer: b
Explanation: The relays are a kind of switching power in which the logic signal is used to energise the relay. The relay contacts are break or make accordingly and helps in switching the current.
12. Which of the following generates a back EMF?
a) relay
b) buffer
c) transistor
d) FET
View Answer
Answer: a
Explanation: The relay generates a back voltage across its terminals when the logic output switches from a high to low state.
13. Which of the following is used to avoid the back EMF in the relay?
a) resistor
b) capacitor
c) inductor
d) diode
View Answer

Answer:d
Explanation: In order to get rid of the back EMF which is generated by the relay a diode is connected across the terminals which operate in the reverse bias so that nothing can harm the relay.
14. Which of the following can provide a speed control technique in the DC motor interfacing?
a) PCM
b) DPCM
c) ADPCM
d) PWM
View Answer
Answer: d
Explanation: The pulse width modulation can provide a speed control technique in the DC motor interfacing by changing its mark/space ratio.
15. Which of the following possesses some loops for providing timing functions?
a) hardware
b) software
c) timer
d) counter
View Answer
Answer: b

1. The time taken to respond to an interrupt is known as
a) interrupt delay
b) interrupt time
c) interrupt latency
d) interrupt function
View Answer
Answer: c
Explanation: The interrupts are the most important function of the embedded system and are responsible for many problems while debugging the system. The time taken to respond to an interrupt is called the interrupt latency.

2. Into how many parts does the interrupt can split the software?
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: a
Explanation: The software interrupt can split into two parts. These are foreground work and background work.
3. Which of the following allows the splitting of the software?
a) wait statement
b) ready
c) interrupt
d) acknowledgement
View Answer
Answer: c
Explanation: The interrupt can make the software into two main parts and these are foreground work and background work.
4. Which part of the software is transparent to the interrupt mechanism?
a) background
b) foreground
c) both background and foreground
d) lateral ground
View Answer
Answer: a
Explanation: The interrupt mechanism is transparent to the background software, that is, the background software is not aware of the existence of the foreground software.
5. Which part of the software performs tasks in response to the interrupts?
a) background
b) foreground
c) lateral ground

d) both foreground and background
View Answer
Answer: b
Explanation: In the foreground work, the tasks are performed in response to the interrupts but in the background work, the tasks are performed while waiting for an interrupt.
6. In which of the following method does the code is written in a straight sequence?
a) method 1
b) timing method
c) sequence method
d) spaghetti method
View Answer
Answer: d
Explanation: In the spaghetti method, the code is written in a straight sequence in which the analysis software goes and polls the port to see if there is data.
7. Which factor depends on the number of times of polling the port while executing the task?
a) data
b) data transfer rate
c) data size
d) number of bits
View Answer
Answer: b
Explanation: The data transfer rate can determine the number of times the port is polled while executing the task.
8. Which of the following can improve the quality and the structure of a code?
a) polling
b) subroutine
c) sequential code
d) concurrent code
View Answer

Answer: b
Explanation: The subroutine can improve the quality and the structure of the code. By using the polling method, as the complexity increases the software structure rapidly fall and it will become inefficient. So the subroutine method is adopted.
9. Which of the following are asynchronous to the operation?
a) interrupts
b) software
c) DMA
d) memory
View Answer
Answer: a
Explanation: The interrupts are asynchronous to the operation and therefore can be used with systems that are the event as opposed to the time driven.
10. Which of the following can be used to create time-driven systems?
a) memory
b) input
c) output
d) interrupts
View Answer
Answer: d
Explanation: The interrupts which are asynchronous can be used with systems that are the event as opposed to the time driven.
11. What does ISR stand for?
a) interrupt standard routine
b) interrupt service routine
c) interrupt software routine
d) interrupt synchronous routine
View Answer
Answer: b
Explanation: The data transfer codes are written as part of the interrupt service routine which is associated with the interrupt generation by the hardware.

12. Which can activate the ISR?
a) interrupt
b) function
c) procedure
d) structure
View Answer
Answer: a
Explanation: When the port receives the data, it will generate an interrupt which in turn activates the ISR.
13. Which code is written as part of the ISR?
a) data receive code
b) sequential code
c) data transfer code
d) concurrent code
View Answer
Answer: c

. Which interrupts are generated by the on-chip peripherals?
a) internal
b) external
c) software
d) hardware
View Answer
Answer: a
Explanation: The internal interrupts are generated by the serial and parallel ports which are on-chip peripherals.
2. Which of the following is the common method for connecting the peripheral to the processor?
a) internal interrupts
b) external interrupts
c) software

d) exception
View Answer
Answer: b
Explanation: The common method for connecting the peripheral to the processor is the external interrupts. The external interrupts are provided through the external pins which are connected to the peripherals.
3. Which interrupt can make a change in the processor’s mode?
a) internal interrupt
b) external interrupts
c) exceptions
d) software mode
View Answer
Answer: c
Explanation: An exception is an event which changes the software flow to process the event. It includes both internal and external interrupts which cause the processor to change to a service routine.
4. How many exceptions does an MC68000 have?
a) 256
b) 128
c) 90
d) 70
View Answer
Answer: c
Explanation: The MC68000 have 256 table entries which describe 90 exceptions.
5. Which interrupts allows a protected state?
a) internal interrupt
b) external interrupt
c) software interrupt
d) both internal and external interrupts
View Answer

Answer: c
Explanation: The software interrupt can change the processor into a protected state by changing the program flow.
6. How a software interrupt is created?
a) instruction set
b) sequential code
c) concurrent code
d) porting
View Answer
Answer: a
Explanation: The software interrupts includes a set of instructions for handling interrupts. The instruction set allows a currently executing program to change its flow.
7. What does SWI stand for?
a) standard interrupt instruction
b) sequential interrupt instruction
c) software interrupt instruction
d) system interrupt instruction
View Answer
Answer: c
Explanation: The instruction set of software interrupts are provided by the special instruction set. One such is the SWI which is commonly used in Z80.
8. Which of the following use SWI as interrupt mechanism?
a) PowerPC
b) MC68000
c) Z80
d) IBM PC
View Answer
Answer: c
Explanation: The PowerPC and MC68000 use TRAP instruction set for accessing software interrupt. IBM PC uses 8086 NMI. Z80 uses SWI for accessing software interrupts.

9. Which of the following supplies additional data to the software interrupt?
a) internal interrupt
b) external interrupt
c) software interrupt
d) nmi
View Answer
Answer: c
Explanation: For using the software interrupt more effectively, the additional data are used, which specifies the type of the request and data parameters are passed to the specific ISR. This additional data are offered by certain registers.
10. Which software interrupt is used in MC68000?
a) Internal interrupt
b) TRAP
c) SWI
d) NMI
View Answer
Answer: b
Explanation: The MC68000 uses a software interrupt mechanism for accessing interrupts from the peripheral in which the instruction are created using the TRAP mechanism.
11. Which of the following are accessible by the ISR in software interrupt mechanism?
a) register
b) interrupt
c) nmi
d) memory
View Answer
Answer: a
Explanation: The additional data are offered by certain registers and these additional data are used to specify the type of the data parameter and the request with the specific ISR when running in the software interrupt mode.
12. What allows the data protection in the software interrupt mechanism?
a) Different mode
b) Same mode

c) SWI
d) TRAP
View Answer
Answer: a
Explanation: The switching between user mode and supervisor mode provides protection for the processor, that is, the different modes in the software interrupt allows the memory and the associated code and data to be protected from each other.
13. What does NMI stand for?
a) non-machine interrupt
b) non-maskable interrupt
c) non-massive interrupt
d) non-memory interrupt
View Answer
Answer: b
Explanation: The NMI stand for the non-maskable interrupt in which the external interrupts cannot be masked out.
14. Which NMI is used in the IBM PC?
a) SWI
b) TRAP
c) 80×86 NMI
d) Maskable interrupt
View Answer
Answer: c
Explanation: The most commonly used non-maskable interrupt is the 80×86 NMI, which is implemented in the IBM PC.
15. Which can be used to pass the status information to the calling software in the software interrupt mechanism?
a) register
b) memory
c) flag
d) nmi
View Answer
Answer: a

1. Which of the following uses clock edge to generate an interrupt?
a) edge triggered
b) level-triggered
c) software interrupt
d) nmi
View Answer
Answer: a
Explanation: In the edge-triggered interrupt, the clock edge is used to generate an interrupt. The transition is from a logical low to high or vice versa.
2. In which interrupt, the trigger is dependent on the logic level?
a) edge triggered
b) level-triggered
c) software interrupt
d) nmi
View Answer
Answer: b
Explanation: In the level-triggered interrupt, the trigger is completely dependent on the logic level. The processors may require the level to be in a certain clock width so that the shorter pulses which are shorter than the minimum pulse width are ignored.
3. At which point the processor will start to internally process the interrupt?
a) interrupt pointer
b) instruction pointer
c) instruction boundary
d) interrupt boundary
View Answer
Answer: c
Explanation: After the recognition of the interrupt, and finds that it is not an error condition with the currently executing interrupt, then the interrupt will not be internally executed until the current execution has completed. This point is known as the instruction boundary. At this point, the processor will start to internally process the interrupt.

4. What does 80×86 use to hold essential data?
a) stack frame
b) register
c) internal register
d) flag register
View Answer
Answer: a
Explanation: The MC68000 and 80×86 family use stack frame for holding the data whereas RISC processors use special internal registers.
5. What does the RISC processor use to hold the data?
a) flag register
b) accumulator
c) internal register
d) stack register
View Answer
Answer: c
Explanation: The RISC processors uses special internal registers to hold data whereas the 80×86 and MC68000 family uses stack register to hold the data.
6. Which of the following is a stack-based processor?
a) MC68000
b) PowerPC
c) ARM
d) DEC Alpha
View Answer
Answer: a
Explanation: The MC68000, Intel 80×86 and most of the b-bit controllers are based on the stack-based processors whereas PowerPC, DEC alpha, and ARM are RISC families which have a special internal register for holding the data.
7. Which of the following is used to reduce the external memory cycle?
a) internal hardware stack
b) internal software stack

c) external software stack
d) internal register
View Answer
Answer: a
Explanation: Some of the processors use internal hardware stack which helps in reducing the external memory cycle necessary to store the stack frame.
8. How many interrupt levels are supported in the MC68000?
a) 2
b) 3
c) 4
d) 7
View Answer
Answer: d
Explanation: The MC68000 has an external stack for holding the data. The MC68000 family supports a seven interrupt level which are encoded into three interrupt pins.
9. How many interrupt pins are used in MC68000?
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: b
Explanation: The MC68000 family supports a seven interrupt level which are encoded into three interrupt pins. These interrupt pins are IP0, IP1, and IP2.
10. Which priority encoder is used in MC68000?
a) 4-to-2 priority encoder
b) LS148 7-to-3
c) 2-to-4 priority encoder

d) LS148 3-to-7
View Answer
Answer: b
Explanation: The LS148 7-to-3 priority encoder is used in MC68000. This converts the seven external pins into a three-bit binary code.
11. Which of the following converts the seven external pins into a 3-bit binary code?
a) priority encoder
b) 4-to-2 priority encoder
c) LS148 7-to-3
d) 2-to-4 priority encoder
View Answer
Answer: c
Explanation: The LS148 7-to-3 priority encoder can convert the seven external pins into a three-bit binary code.
12. Which of the following ensures the recognition of the interrupt?
a) interrupt ready
b) interrupt acknowledge
c) interrupt terminal
d) interrupt start
View Answer
Answer: b
Explanation: The interrupt level remains asserted until its interrupt acknowledgment cycle ensures the recognition of the interrupt.
13. Which of the following is raised to the interrupt level to prevent the multiple interrupt request?
a) internal interrupt mask
b) external interrupt mask
c) non-maskable interrupt
d) software interrupt
View Answer
Answer: a

1. What does MSR stand for?
a) machine state register
b) machine software register
c) minimum state register
d) maximum state register
View Answer
Answer: a
Explanation: The MSR is a machine state register. When the exception is recognised, the address of the instruction and the MSR are stored in the supervisor registers while handling an exception.
2. How many supervisor registers are associated with the exception mode?
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: a
Explanation: When the exception is recognised, the address of the instruction and the machine state register(MSR) are stored in the supervisor registers in the exception mode. There are two supervisor registers SRR0 and SRR1.
3. What happens when an exception is completed?
a) TRAP instruction executes
b) SWI instruction executes
c) RFI instruction executes
d) terminal count increases
View Answer
Answer: c
Explanation: When an exception is recognised, the address of the instruction and the MSR are stored in the supervisor registers and the processor moves to the supervisor mode and starts to execute the handler which is associated with the

vector table. The handler examines the DSISR and FPSCR registers and carries out the required function. When it gets completed the RFI or return-from-interrupt instruction is executed.

4. How many general types of exceptions are there?

a) 2
b) 3
c) 6
d) 4

View Answer

Answer: d

Explanation: There are four general types of exceptions. They are synchronous precise, asynchronous precise, synchronous imprecise and asynchronous imprecise.

5. In which of the exceptions does the external event causes the exception?

a) synchronous exception
b) asynchronous exception
c) precise
d) imprecise

View Answer

Answer: b

Explanation: The asynchronous exception is the one in which an external event causes an exception and is independent of the instruction flow. On the other hand, the synchronous exceptions are synchronised, that is, it is caused by the instruction flow.

6. Which of the exceptions are usually a catastrophic failure?

a) imprecise exception
b) precise exception
c) synchronous exception
d) asynchronous exception

View Answer

Answer: a

Explanation: An imprecise exception is a catastrophic failure in which the processor cannot continue processing or allow a particular task or program to continue.

7. Which of the exceptions allows the system reset or memory fault?
a) imprecise exception
b) precise exception
c) synchronous exception
d) asynchronous exception
View Answer
Answer: a
Explanation: The system reset or memory fault falls into the category of imprecise exceptions while accessing the vector table.
8. Which registers are used to determine the completion status?
a) MSR
b) flag register
c) DSISR
d) index register
View Answer
Answer: c
Explanation: The completion status can be determined by the information bits in the DSISR and FPSCR registers.
9. Which of the following does not support PowerPC architecture?
a) synchronous precise
b) asynchronous precise
c) synchronous imprecise
d) asynchronous imprecise
View Answer
Answer: c
Explanation: The synchronous imprecise is usually not supported on the PowerPC architecture and also in the MPC601, MPC603 etc.
10. Which exceptions are used in the PowerPC for floating point?
a) synchronous imprecise
b) asynchronous imprecise
c) synchronous precise

d) synchronous imprecise
View Answer
Answer: a
Explanation: The PowerPC can handle the floating point exception by making use of the synchronous imprecise mode.
11. Which exception is used in the external interrupts and decrementer-caused exceptions?
a) synchronous precise
b) asynchronous precise
c) synchronous imprecise
d) asynchronous imprecise
View Answer
Answer: b
Explanation: The asynchronous precise type exception is used to handle the external interrupts and decrementer-caused exceptions. Both these can occur at any time within the instruction flow.
12. Which exception can be masked by clearing the EE bit to zero in the MSR?
a) synchronous imprecise
b) synchronous precise
c) asynchronous imprecise
d) asynchronous precise
View Answer
Answer: d

1. Which of the following can be done to ensure that all interrupts are recognised?
a) reset pin
b) external ready pin
c) handshaking
d) acknowledgment
View Answer

Answer: c
Explanation: The exception handler performs some kind of handshaking to ensure that all the interrupts are recognised.
2. How many types of exceptions are associated with the asynchronous imprecise?
a) 1
b) 2
c) 3
d) 4
View Answer
Answer: b
Explanation: Two types of exceptions are associated with the asynchronous imprecise. These are system reset and machine checks.
3. How is the internal registers and memories are reset?
a) system reset
b) memory reset
c) peripheral reset
d) software reset
View Answer
Answer: a
Explanation: By doing the system reset, all the current processing are stopped and the internal registers and the memories are reset.
4. How is the machine check exception is taken in an asynchronous imprecise?
a) ME bit
b) EE bit
c) FE0
d) FE1
View Answer
Answer: a
Explanation: The machine check exception is taken only if the ME bit of the MSR is set. If it is cleared, the processor will enter into a check stop state.

5. Which of the following are the exceptions associated with the asynchronous imprecise?
a) decrementer interrupt
b) machine check
c) instruction dependent
d) external interrupt
View Answer
Answer: b
Explanation: The machine check and the system reset are two types of exceptions which are associated with the asynchronous imprecise.
6. Which of the following possesses an additional priority?
a) asynchronous precise
b) asynchronous imprecise
c) synchronous precise
d) synchronous imprecise
View Answer
Answer: c
Explanation: The synchronous precise exceptions provide additional priority because it is possible for an instruction to generate more than one exception.
7. Which of the following has more priority?
a) system reset
b) machine check
c) external interrupt
d) decrementer interrupt
View Answer
Answer: a
Explanation: The system reset has the first priority then comes the machine reset, next priority moves for the instruction dependent, and the next priority is an external interrupt, and last priority level goes for the decrementer interrupt.
8. Which bit controls the external interrupts and the decrementer exceptions?
a) FE1
b) FE0

c) EE
d) ME
View Answer
Answer: c
Explanation: The EE bit in the MSR controls the external interrupts and the decrementer exceptions.
9. Which bit controls the machine check exceptions?
a) ME
b) FE0
c) FE1
d) EE
View Answer
Answer: a
Explanation: The ME bit in the MSR controls the machine check interrupts.
10. Which bits control the floating point exceptions?
a) EE
b) FE0
c) FE1
d) both FE1 and FE2
View Answer
Answer: d
Explanation: The FE0 and FE1 control the floating point exceptions.
11. Which of the following is a 16 kbyte block?
a) register
b) vector table
c) buffer
d) lookaside buffer
View Answer
Answer: b

1. Which processors use fast interrupts?
a) DSP processor
b) RISC processor
c) CISC processor
d) Harvard processor
View Answer
Answer: a
Explanation: The fast interrupts are used in the DSP processors or in microcontrollers in which a small routine is executed without saving the context of the processor.
2. Which interrupts generate fast interrupt exception?
a) internal interrupt
b) external interrupt
c) software interrupt
d) hardware interrupt
View Answer
Answer: b
Explanation: The external interrupts generates the fast interrupt routine exception in which the external interrupt is synchronised with the processor clock.
3. What is the disadvantage of the fast interrupts?
a) stack frame
b) delay
c) size of routine
d) low speed
View Answer
Answer: c
Explanation: The disadvantages associated with the fast interrupt is the size of routine which can be executed and the resources allocated. In this technique, it allocates a couple of address registers for the fast interrupt routine.
4. Which of the following does not have a stack frame building?
a) hardware interrupt
b) software interrupt

c) non-maskable interrupt
d) fast interrupt
View Answer
Answer: d
Explanation: The fast interrupt does not have stack frame building and it does not possess any such delays. This can be considered as the advantage of the fast interrupts.
5. What is programmed to generate a two instruction fast interrupt?
a) software
b) application
c) timer
d) sensor
View Answer
Answer: c
Explanation: The SCI timer generates the two instruction fast interrupt. This increment the register R1.
6. Which of the following can auto increment the register R1?
a) SCI timer
b) interrupt
c) software interrupt
d) non-maskable interrupt
View Answer
Answer: a
Explanation: The SCI timer is used to generate the two instruction fast interrupt that can increment the register R1 which acts as a simple counter.
7. Which of the following forces a standard service routine?
a) READY interrupt
b) IRQA interrupt
c) NMI
d) software interrupt
View Answer

Answer: b
Explanation: The SCI timer is used to generate the two instruction fast interrupt which increments the register R1 that acts as a simple counter which times the period between the events. The events itself generates an IRQA interrupt, that forces the service routine.
8. Which of the following can be used as a reset button?
a) NMI
b) internal interrupt
c) external interrupt
d) software interrupt
View Answer
Answer: a
Explanation: The non-maskable interrupt is used to generate an interrupt to try and recover control and therefore, the NMI can be used as a reset button.
9. Which of the following is connected to a fault detection circuit?
a) internal interrupt
b) external interrupt
c) NMI
d) software interrupt
View Answer
Answer: c

1. Which of the following provides a buffer between the user and the low-level interfaces to the hardware?
a) operating system
b) kernel
c) software
d) hardware
View Answer

Answer: a
Explanation: The operating system is software which provides a buffer between the low-level interfaces to the hardware within the system and the user.
2. Which of the following enables the user to utilise the system efficiently?
a) kernel
b) operating system
c) software
d) hardware
View Answer
Answer: b
Explanation: The operating system is software that enables the users to utilise the system effectively.
3. Which of the following can make the application program hardware independent?
a) software
b) application manager
c) operating system
d) kernel
View Answer
Answer: c
Explanation: The operating system allows the software to be moved from one system to another and therefore, it can make the application program hardware independent.
4. Which of the following speed up the testing process?
a) kernel
b) software
c) application manager
d) program debugging tools
View Answer
Answer: d
Explanation: The program debugging tools can speed up the testing process which can make the processor faster.
5. Which of the following includes its own I/O routine?
a) hardware

b) kernel
c) operating system
d) application manager
View Answer
Answer: c
Explanation: An operating system is a software which includes its own I/o routine in order to drive the serial ports and the parallel ports.
6. Which forms the heart of the operating system?
a) kernel
b) applications
c) hardware
d) operating system
View Answer
Answer: a
Explanation: The kernel is the heart of the operating system. This can control the hardware and can deal with the interrupts, I/O systems, memory etc.
7. Which of the following locates a parameter block by using an address pointer?
a) OS
b) kernel
c) system
d) memory
View Answer
Answer: b
Explanation: The kernel is the heart of the operating system which can control the hardware and can deal with the interrupts, I/O systems, memory etc. It can also locate the parameter block by using an address pointer which is stored in the predetermined address register.
8. Which of the following are not dependent on the actual hardware performing the physical task?
a) applications
b) hardware
c) registers

d) parameter block
View Answer
Answer: d
Explanation: The kernel can locate the parameter block by using an address pointer which is stored in the predetermined address register. These parameter blocks are standard throughout the operating system, that is, they are not dependent on the actual hardware performing the physical task.
9. Which of the following bus can easily upgrade the system hardware?
a) control bus
b) data bus
c) VMEbus
d) bus interface unit
View Answer
Answer: c
Explanation: The software can be easily moved from one system to another which is more important for designing embedded systems, especially for those which use an industry standard bus such as VMEbus, in which the system hardware can be expanded or upgraded.
10. Which of the following is the first widely used operating system?
a) MS-DOS
b) windows XP
c) android
d) CP/M
View Answer
Answer:d
Explanation: The first widely used operating system is the CP/M which is developed for Intel 8080 and the 8”floppy disk system.
11. Which of the following is an example of a single task operating system?
a) android
b) windows
c) IOS

d) CP/M
View Answer
Answer: d
Explanation: The CP/M is a single task operating system, that is, only one task or an application can be executed at a time.
12. Which of the following becomes a limiting factor while an application program has to be complete?
a) memory
b) peripheral
c) input
d) output
View Answer
Answer: a
Explanation: The application program has to complete and the memory becomes a limiting factor, which can be solved by using program overlays.
13. Which of the following cannot carry implicit information?
a) semaphore
b) message passing
c) threads
d) process
View Answer
Answer: a

1. Which of the following works by dividing the processor's time?
a) single task operating system
b) multitask operating system
c) kernel
d) applications
View Answer

Answer: b
Explanation: The multitasking operating system works by dividing the processor’s time into different discrete time slots, that is, each application requires a defined number of time slots to complete its execution.
2. Which of the following decides which task can have the next time slot?
a) single task operating system
b) applications
c) kernel
d) software
View Answer
Answer: c
Explanation: The operating system kernel decides which task can have the next time slot. So instead of the task executing continuously until completion, the execution of the processor is interleaved with the other tasks.
3. Which of the following controls the time slicing mechanism in a multitasking operating system?
a) kernel
b) single tasking kernel
c) multitasking kernel
d) application manager
View Answer
Answer: c
Explanation: The multitasking operating systems are associated with the multitasking kernel which controls the time slicing mechanism.
4. Which of the following provides a time period for the context switch?
a) timer
b) counter
c) time slice
d) time machine
View Answer
Answer: c
Explanation: The time period required for each task for execution before it is stopped and replaced during a context switch is known as the time slice.

5. Which of the following can periodically trigger the context switch?
a) software interrupt
b) hardware interrupt
c) peripheral
d) memory
View Answer
Answer: b
Explanation: The multitasking operating systems are associated with the multitasking kernel which controls the time slicing mechanism. The time period required for each task for execution before it is stopped and replaced during a context switch is known as the time slice. These are periodically triggered by a hardware interrupt from the system timer.
6. Which interrupt provides system clock in the context switching?
a) software interrupt
b) hardware interrupt
c) peripheral
d) memory
View Answer
Answer: b
Explanation: The multitasking operating systems deals with the multitasking kernel which controls the time slicing mechanism and the time period required for each task for execution before it is stopped and replaced during a context switch is known as the time slice which are periodically triggered by a hardware interrupt from the system timer. This hardware interrupt provides the system clock in which several interrupts are executed and counted before a context switch is performed.
7. The special tale in the multitasking operating system is also known as
a) task control block
b) task access block
c) task address block
d) task allocating block
View Answer
Answer: a
Explanation: When a context switch is performed, the current program or task is interrupted, so the processor’s registers are saved in a special table which is known as task control block.

8. Which of the following stores all the task information that the system requires?
a) task access block
b) register
c) accumulator
d) task control block
View Answer
Answer: d
Explanation: The task control block stores all the task information that the system requires and this is done when the context switch is performed so that the currently running program is interrupted.
9. Which of the following contains all the task and their status?
a) register
b) ready list
c) access list
d) task list
View Answer
Answer: b
Explanation: The ‘ready’ list possesses all the information regarding a task, that is, all the task and its corresponding status which is used by the scheduler to decide which task should execute in the next time slice.
10. Which determines the sequence and the associated task’s priority?
a) scheduling algorithm
b) ready list
c) task control block
d) application register
View Answer
Answer: a
Explanation: The scheduling algorithm determines the sequence and an associated task’s priority. It also determines the present status of the task.
11. Which can control memory usage?
a) operating system
b) applications

c) hardware
d) kernel
View Answer
Answer:d
Explanation: The kernel can control the memory usage and it can also prevent the tasks from corrupting each other.
12. Which can control the memory sharing between the tasks?
a) kernel
b) application
c) software
d) OS
View Answer
Answer: a
Explanation: The kernel can control memory sharing between tasks which allow sharing common program modules.
13. Which of the following can implement the message passing and control?
a) application software
b) operating system
c) software
d) kernel
View Answer
14. How many types of messages are associated with the real-time operating system?
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: a
Explanation: There are two basic types of messages associated with the real-time operating system. These are semaphores and messages.

15. Which of the following can carry information and control task?
a) semaphore
b) messages
c) flags
d) address message
View Answer
Answer: b

1. Which task swapping method does not require the time critical operations?
a) time slice
b) pre-emption
c) cooperative multitasking
d) schedule algorithm
View Answer
Answer: a
Explanation: Time-critical operations are not essential in the time slice mechanism. Time slice mechanism describes the task switching in a particular time slot.
2. Which task swap method works in a regular periodic point?
a) pre-emption
b) time slice
c) schedule algorithm
d) cooperative multitasking
View Answer
Answer: b
Explanation: The time slicing works by switching task in regular periodic points in time, that is, any task that needs to run next will have to wait until the current time slice is completed.
3. Which of the following determines the next task in the time slice method of task swapping?
a) scheduling program
b) scheduling application

c) scheduling algorithm
d) scheduling task
View Answer
Answer: c
Explanation: The time slice mechanism can also be used as a scheduling method in which the task to run next is determined by the scheduling algorithm.
4. Which of the following can be used to distribute the time slice across all the task?
a) timer
b) counter
c) round-robin
d) task slicing
View Answer
Answer: c
Explanation: The time slice based system uses fairness scheduler or round robin to distribute the time slices across all the tasks that need to run in a particular time slot.
5. What do a time slice period plus a context switch time of the processor determines?
a) scheduling task
b) scheduling algorithm
c) context task
d) context switch time
View Answer
Answer: d
Explanation: The context switch time of the processor along with the time slice period determines the context switch time of the system which is an important factor in system response, that is, the time period can be reduced to improve the context switching of the system which will increase the number of task switches.
6. Which can increase the number of task switches?
a) time period
b) frequency
c) time rate

d) number of cycles
View Answer
Answer: a
Explanation: The time period can be reduced to improve the context switching of the system which will increase the number of task switches.
7. Which mechanism is used behind the Windows 3.1?
a) time slice
b) pre-emption
c) cooperative multitasking
d) scheduling algorithm
View Answer
Answer: c
Explanation: The cooperative multitasking mechanism is used the Windows 3.1 but it is not applicable to the real-time operating systems.
8. Which of the following provides an illusion of multitasking?
a) single task operating system
b) multitasking operating system
c) cooperative multitasking
d) pre-emption
View Answer
Answer: c
Explanation: The cooperative multitasking co-operates between them which provides the illusion of multitasking. This is done by periodically executing the tasks.
9. Which task method follows a currently running task to be stopped by a higher priority task?
a) scheduling algorithm
b) time slice
c) cooperative multitasking
d) pre-emption
View Answer

Answer: d
Explanation: The pre-emption is an alternative method of the time slice where the currently running task can be stopped or preempted or switched out by a higher priority active task.
10. Which of the following requires programming within the application?
a) time slice
b) scheduling algorithm
c) pre-emption
d) cooperative multitasking
View Answer
Answer: d
Explanation: The cooperative multitasking requires programming within the application and the system can be destroyed by a single program which hogs all the processing power. Therefore, it is not applicable in the real-time operating system.
11. What does RMS stand for?
a) rate monotonic scheduling
b) rate machine scheduling
c) rate monotonic software
d) rate machine software
View Answer
Answer: a
Explanation: The rate monotonic scheduling is a method that is used to assign priority for a pre-emptive system such that the correct execution can be guaranteed.
12. Which of the following task swapping method is a better choice in the embedded systems design?
a) RMS
b) pre-emptive
c) cooperative multitasking
d) time slice
View Answer
Answer: b

1. Which of the following allows a lower priority task to run despite the higher priority task is active and waiting to preempt?
a) message queue
b) message passing
c) semaphore
d) priority inversion
View Answer
Answer: d
Explanation: The priority inversion mechanism where the lower priority task can continue to run despite there being a higher priority task active and waiting to preempt.
2. What happens to the interrupts in an interrupt service routine?
a) disable interrupt
b) enable interrupts
c) remains unchanged
d) ready state
View Answer
Answer: a
Explanation: In the interrupt service routine, all the other interrupts are disabled till the routine completes which can cause a problem if another interrupt is received and held pending. This can result in priority inversion.
3. Which of the following is a part of RTOS kernel?
a) memory
b) input
c) ISR
d) register
View Answer
Answer: c
Explanation: The ISR can send the message for the tasks and it is a part of RTOS kernel.
4. Which of the following is an industrial interconnection bus?
a) bus interface unit
b) data bus
c) address bus

d) VMEbus
View Answer
Answer: d
Explanation: The VMEbus is an interconnection bus which is used in the industrial control and many other real-time applications.
5. Which of the following supports seven interrupt priority level?
a) kernel
b) operating system
c) VMEbus
d) data bus
View Answer
Answer: c
Explanation: The VMEbus supports seven interrupt priority level which allows the prioritisation of the resources.
6. What type of interrupt handling is seen in multiprocessor applications?
a) centralised interrupt
b) handled by one MASTER
c) distributed handling
d) shared handling
View Answer
Answer: c
Explanation: The multiprocessor applications allows distributed handling in which the direct communication with the individual masters is possible.
7. Which of the following is an asynchronous bus?
a) VMEbus
b) timer
c) data bus
d) address bus
View Answer

Answer: a
Explanation: The VMEbus is based on Eurocard sizes and is asynchronous which is similar to the MC68000.
8. Which of the following is not a priority based?
a) priority inversion
b) message passing
c) fairness system
d) message queuing
View Answer
Answer: c

1. Which of the following can be used to refer to entities within the RTOS?
a) threads
b) kernels
c) system
d) applications
View Answer
Answer: a
Explanation: The threads and processes can be used to refer to entities within the RTOS. They provide an interchangeable replacement for the task. They have a slight difference in their function. A process is a program in execution and it has its own address space whereas threads have a shared address space. The task can be defined as a set of instructions which can be loaded into the memory.
2. Which of the following defines the set of instructions loaded into the memory?
a) process
b) task
c) thread
d) system hardware
View Answer

Answer: b
Explanation: The task can be defined by the set of instructions which is loaded into the memory and it can split into two or more tasks.
3. Which of the following uses its own address space?
a) thread
b) process
c) task
d) kernel
View Answer
Answer: a
Explanation: Threads uses shared memory space and it uses the memory space of the process.
4. Which of the following does not uses a shared memory?
a) process
b) thread
c) task
d) kernel
View Answer
Answer: a
Explanation: The program in execution is known as the process. The process does not share the memory space but the threads have a shared memory address. When the CPU switches from process to another, the current information is stored in the process descriptor.
5. Which of the following can own and control the resources?
a) thread
b) task
c) system
d) peripheral
View Answer
Answer: b
Explanation: The task and process have several characteristics and one such is that the task or process can own or control resources and it has threads of execution which are the paths through the code.

6. Which can be supported if the task or process maintains a separate data area for each thread?
a) single thread system
b) mono thread system
c) multiple threads
d) dual threads
View Answer
Answer: c
Explanation: The multiple threads can be supported only if the process or task can maintain separate data areas for each thread.
7. Which of the following possesses threads of execution?
a) process
b) thread
c) kernel
d) operating system
View Answer
Answer: a
Explanation: The process has threads of execution which are the paths through the code.
8. Which of the following is inherited from the parent task?
a) task
b) process
c) thread
d) kernel
View Answer
Answer: c
Explanation: The threads are a part of the process, that is, it uses a shared memory of the process and therefore said that its resources are inherited from the parent process or task.
9. Which term is used to encompass more than a simple context switch?
a) process
b) single thread system
c) thread

d) multithread
View Answer
Answer: a
Explanation: The process includes the additional information which is used to encompass more than a simple context switch. This is similar to the task switching, that is why it is said that process and task are interchangeable.
10. Which can be considered as the lower level in the multitasking operating system?
a) process
b) task
c) threads
d) multi threads
View Answer
Answer: c

1. Which of the following kernel supports the MC68000 family?
a) pSOS+
b) pSOS+kernel
c) pNA+ network manager
d) pSOS multiprocessor kernel
View Answer
Answer: a
Explanation: The pSOS+ kernel supports many processor families like Intel 80×86, M88000, MC68000 and i960 processors. The kernel is small in size and has a 15-20 Kbytes RAM.
2. What is the worst case figure for interrupt latency for an MC68020 running at 25MHz?
a) 19 microseconds
b) 6 microseconds
c) 20 microseconds
d) 8 microseconds
View Answer

Answer: b
Explanation: The worst case figure for the interrupt latency for an MC68020 which runs at 25MHz is 6 microseconds and the context switch for the same is 19 microseconds.
3. Which of the following is the multiprocessing version of the kernel?
a) pSOS+
b) pSOS+ kernel
c) pSOS multiprocessor kernel
d) pSOS
View Answer
Answer: c
Explanation: The pSOS+ is a multitasking real-time kernel of the operating system and pSOS+m or the pSOS+ multiprocessor kernel is the multiprocessing version of the kernel. It is virtually same as the single processor version except the ability to send and receiving system objects from the processors within the system.
4. Which of the following is a compiler independent run-time environment for C applications?
a) pSOS multiprocessor kernel
b) pSOS
c) pSOS+
d) pREC+ runtime support
View Answer
Answer: d
Explanation: The pREC+ is a compiler independent runtime environment for the C program applications.
5. Which kernel provides 88 functions that can be called from the C programs?
a) pSOS multiprocessor kernel
b) pSOS
c) pSOS+
d) pREC+ runtime support
View Answer
Answer: d
Explanation: The pREC+ is compatible with the ANSI X3J11 and can provide the 88 functions that can be called from the C programs.

6. Which of the following is not a standalone product?
a) pREC+ runtime support
b) pSOS+m
c) pSOS+
d) pSOS+ kernel
View Answer
Answer: a
Explanation: The pREC+ is not a standalone product it uses pSOS+m or pSOS+ for the input/output devices and task functions and calls the PHILE+ for the file and disk I/O.
7. Which kernel allows the multiple tasks which use the same routine?
a) pREC+ runtime support
b) pSOS+m
c) pSOS+
d) pSOS+ kernel
View Answer
Answer: a
Explanation: The pREC+ runtime support kernel's routines are reentrant that allows the multiple tasks to use the same routine simultaneously.
8. Which provides the TCP/IP communication over the ethernet and FDDI?
a) pSOS+m
b) pSOS+ kernel
c) pNA+ network manager
d) pSOS+
View Answer
Answer: c

1. Which can provide efficient downloading and debugging communication between the host and target system?
a) pSOS+
b) pSOS+ kernel
c) pHILE+ file system

d) pNA+ network manager
View Answer
Answer: d
Explanation: The pNA+ network manager can provide efficient downloading and debugging communication between the host and target system.
2. Which of the following is a system level debugger which provides the low-level debugging facilities and the system debugging?
a) pROBE+ system level debugger
b) pNA+ network manager
c) pHILE+ file system
d) pNA+ network manager
View Answer
Answer: a
Explanation: The pROBE+ system level debugger which can provide the system debugging and the low level debugging.
3. How is the pROBE+ system level debugger communicate with the outside world?
a) peripheral output
b) serial port
c) LCD display
d) LED
View Answer
Answer: b
Explanation: The pROBE+ system level debugger can communicate with the outside world through the serial port or by installing pNA+, a TCP/IP link can be used instead.
4. Which of the following is a complementary product to pROBE+ system level debugger?
a) pSOS+ kernel
b) pSOS+
c) XRAY+ source level debugger
d) pSOS+m
View Answer

Answer: c
Explanation: The XRAY+ source level debugger is a complementary product to pROBE+ system level debugger as it can use the debugger information and combine with the C source and other functions on the host that can provide an integrated debugging.
5. Which of the following supports the MS-DOS file?
a) pNA+ network manager
b) pSOS+ kernel
c) pSOS+ m
d) pHILE+ file system
View Answer
Answer: d
Explanation: The pHILE+ file system supports the MS-DOS file structure and the product can provide input and output file.
6. Who developed the OS-9?
a) Microwave
b) Microwave and Motorola
c) Motorola and IBM
d) Microwave and IBM
View Answer
Answer: b
Explanation: The OS-9 is developed by Motorola and Microwave as a real-time operating system. The operating system is developed for MC6809 which is an 8-bit processor.
7. Who had developed VRTX-32?
a) Microtec Research
b) Microwave
c) Motorola
d) IBM
View Answer
Answer: a
Explanation: The VRTX-32 is developed by Microtec Research which is a high-performance real-time kernel.

8. Which provides the library interface to allow C programs to call standard I/O functions?
a) RTL
b) TNX
c) IFX
d) MPV
View Answer
Answer: a

1. Which of the following unit protects the memory?
a) bus interface unit
b) execution unit
c) memory management unit
d) peripheral unit
View Answer
Answer: c
Explanation: The resources have to be protected in an embedded system and the most important resource to be protected is the memory which is protected by the memory management unit through different programming.
2. Which unit protects the hardware?
a) MMU
b) hardware unit
c) bus interface unit
d) execution unit
View Answer
Answer: a
Explanation: The hardware part is protected by the memory management unit. The memory part is also protected by the memory management unit. The hardware such as the input-output devices are protected and is prevented from the direct access.
3. Which mechanism can control the access?
a) in-situ

b) spin-lock
c) ex-situ
d) both in-situ and ex-situ
View Answer
Answer: b
Explanation: Both the memory and the hardware part are protected by the memory management unit and the hardware such as the input-output devices are protected, These are prevented from the direct access. These accesses are made through a device driver and this device driver can control the serial port. Such a mechanism is called spin-lock mechanism which provides the control access.
4. Which of the following is very resilient to the system crashes?
a) Windows 3.1
b) MS-DOS
c) Windows NT
d) kernel
View Answer
Answer: c
Explanation: The Windows NT is very resilient to the system crashes and the system will continue while the processes can crash. This is because of the user mode and the kernel mode which is coupled with the resource protection. This resilience is a big advantage over the MS-DOS and Windows 3.1.
5. Which of the following are coupled in the Windows NT for the resource protection?
a) kernel mode and user mode
b) user mode and protected mode
c) protected mode and real mode
d) virtual mode and kernel mode
View Answer
Answer: a
Explanation: The user mode and the kernel mode are coupled with the resource protection and this resilience in Windows NT is a big advantage over the MS-DOS and the Windows 3.1.
6. Which of the following support multi-threaded software?
a) Windows NT

b) thread
c) process
d) task
View Answer
Answer: a
Explanation: The Windows NT supports multi-threaded software in which the processes can support several independent paths or threads.
7. Which provides a 4 Gbyte virtual address space?
a) Windows 3.1
b) MS-DOS
c) pSOS+
d) Windows NT
View Answer
Answer: d
Explanation: The virtual address spacing in the Windows NT is somewhat different from the MS-DOS and the Windows 3.1. The Windows NT provides 4 Gbytes virtual address space for each process and that is linearly addressed using 32-bit address values.
8. Which applications can be used with the Windows NT?
a) WIN16
b) WIN32
c) WIN4
d) WIN24
View Answer
Answer: b
Explanation: The WIN32 is also known as 32-bit or even native. It is used for the Windows NT applications which uses the same instruction set as that of the Windows NT and therefore do not need to emulate a different architecture.
9. Which of the following has the same instruction set as that of the Windows NT?
a) WIN32
b) WIN4
c) WIN24

d) WIN16
View Answer
Answer: a
Explanation: WIN32 is used for the Windows NT applications and is also known as even native which uses the same instruction set as that of the Windows NT and therefore do not need to emulate a different architecture.
10. Which can provide more memory than physical memory?
a) real memory
b) physical address
c) virtual memory
d) segmented address
View Answer
Answer: c

1. Which of the following uses a swap file to provide the virtual memory?
a) windows NT
b) kernel
c) memory
d) memory management unit
View Answer
Answer: a
Explanation: The Windows NT use a swap file for providing a virtual memory environment. This file is dynamic and varies with the amount of memory that all the software including the device driver, operating systems and so on.
2. What is the size of the swap file in Windows 3.1?
a) 25 Mbytes
b) 30 Mbytes
c) 50 Mbytes
d) 100 Mbytes
View Answer

Answer: b
Explanation: The Windows 3.1 have a swap file of size 25 Mbytes.
3. What is the nature of the swap file in the Windows NT?
a) static
b) dynamic
c) linear
d) non-linear
View Answer
Answer: b
Explanation: The swap file used in the Windows NT is dynamic and it varies with the amount of memory that all the software including the device driver, operating systems and so on.
4. What limits the amount of virtual memory in Windows 3.1?
a) size of the swap file
b) nature of swap file
c) static file
d) dynamic file
View Answer
Answer: a
Explanation: The swap file of Windows 3.1 have a size of 25 Mbytes and thus limits the amount of virtual memory that it can support.
5. Which of the following control and supervises the memory requirements of an operating system?
a) processor
b) physical memory manager
c) virtual memory manager
d) ram
View Answer
Answer: c
Explanation: The virtual memory manager can control and supervises the memory requirements of the operating system.
6. What is the size of the linear address in the virtual memory manager?
a) 2 Gbytes

b) 12 Gbytes
c) 4 Gbytes
d) 16 Gbytes
View Answer
Answer: c
Explanation: The virtual memory manager can allocate a linear address space of size 4 Gbytes to each process which is unique and cannot be accessed by the other processes.
7. How many modes are used to isolate the kernel and the other components of the operating system?
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: a
Explanation: There are two modes that are used for isolating the kernel and the other components of the operating system from any process and user applications that are running. These are kernel mode and the user mode.
8. Which are the two modes used in the isolation of the kernel and the user?
a) real mode and virtual mode
b) real mode and user mode
c) user mode and kernel mode
d) kernel mode and real mode
View Answer
Answer: c
Explanation: The two modes are kernel mode and the user mode which are used for isolating the kernel and the other components of the operating system from any process and user applications that are running.
9. Which of the following must be used to isolate the access in the user mode?
a) device driver
b) software driver
c) on-chip memory

d) peripherals
View Answer
Answer: a
Explanation: The device driver is used to control and isolate the access when it is in user mode. This is used to ensure that no conflict is caused.
10. Which mode uses 16 higher real-time class priority levels?
a) real mode
b) user mode
c) kernel mode
d) protected mode
View Answer
Answer: c

1. Which filesystem is used in the Windows 95?
a) FAT
b) HPFS
c) VFAT
d) NTFS
View Answer
Answer: c
Explanation: The VFAT is used in the Windows 95 and it also supports long file names.
2. What does HPFS stand for?
a) high performance file system
b) high periodic file system
c) high peripheral file system
d) horse power file system
View Answer

Answer: a
Explanation: The high performance file system is an alternative file system which possess 254 characters. It is used by the OS/2 and also writes caching to disk technique that stores data temporarily and write it to the disk.
3. Which filing system is used by the Windows NT?
a) FAT
b) VFAT
c) HPFS
d) NTFS
View Answer
Answer: d
Explanation: The NT filing system or NTFS is used by the Windows NT, that is its own filing system which conforms to various security operations and allows system administrators to restrict access to files.
4. Which filesystem is used by the OS/2?
a) FAT
b) VFAT
c) HPFS
d) NTFS
View Answer
Answer: c
Explanation: The high performance file system is an alternative file system which possess 254 characters. It is used by the OS/2 and also writes caching to disk technique that stores data temporarily and write it to the disk.
5. What do HAL stand for?
a) hardware abstraction layer
b) hardware address layer
c) hardware access layer
d) hardware address lead
View Answer
Answer: a
Explanation: The HAL is the hardware abstraction layer. This provides the portability across the multiprocessor and different platforms.

6. Which of the following can provide portability across different processor-based platforms?
a) File system
b) HAL
c) NTFS
d) FAT
View Answer
Answer: b
Explanation: The HAL or hardware abstraction layer is designed to provide portability across the different platform and different multiprocessor or single processor.
7. Which of the following defines the virtual hardware that the kernel uses?
a) HAL
b) NTFS
c) FAT
d) VFAT
View Answer
Answer: a
Explanation: The HAL or hardware abstraction layer defines virtual hardware which the kernel uses when it needs to access the processor or hardware resources.
8. Which of the following provides a link between the user processes and threads and the hardware?
a) I/O driver
b) File system
c) Memory
d) LPC
View Answer
Answer: a

1. What does LPC stand for?
a) local procedure call
b) local program call

c) local program code
d) local procedure code
View Answer
Answer: a
Explanation: The LPC is defined as the local procedure call which is responsible for coordinating the system calls from the WIN32 subsystem and an application.
2. Which of the following is responsible for coordinating the system call within an application and the WIN32 subsystem?
a) kernel
b) file system
c) LPC
d) network support
View Answer
Answer: c
Explanation: The local procedure call is responsible for coordinating the system calls from the WIN32 subsystem and an application. Depending upon the type of the system call, the application will be routed directly with the LPC without going through the WIN32 subsystem.
3. Which of the following is responsible for ensuring correct operation of all processes which are running within the system?
a) kernel
b) file system
c) lpc
d) user mode
View Answer
Answer: a
Explanation: The kernel is responsible for ensuring the correct operation of all process which are running within the system. It also provides the synchronisation and the scheduling that the system needs.
4. How many level priority scheme does the scheduling used in the kernel?
a) 8
b) 16
c) 32

d) 64
View Answer
Answer: c
Explanation: The scheduling support in the kernel support 32 level priority scheme and it can be used to schedule threads rather than processes.
5. Which procedure in the kernel allows the thread to wait until a specific resource is available?
a) synchronisation
b) scheduling
c) scheduling and synchronisation
d) lpc
View Answer
Answer: a
Explanation: The synchronisation procedure will allow the thread to wait until a specific resource such as semaphore, object etc are available.
6. Which of the following can preempt the current thread and reschedule the high priority thread in the kernel?
a) interrupt
b) lpc
c) file system
d) memory
View Answer
Answer: a
Explanation: The interrupts and the similar events such as exceptions can pass through the kernel which can preempt the current thread and the can reschedule the high priority thread to process.
7. How many file system does the Windows NT support?
a) 4
b) 5
c) 3
d) 2
View Answer

Answer: c
Explanation: The Windows NT support three file system and these coexist with each other even though there are some restrictions.
8. What does FAT stand for?
a) file address table
b) file access table
c) file arbitrary table
d) file allocation table
View Answer
Answer: d

1. Who started Linux first as a personal project?
a) Linus Torvalds
b) Ken Thompson
c) Dennis Ritchie
d) John Dell
View Answer
Answer: a
Explanation: The Linux was taken as a personal project by Linus Torvalds at the University of Helsinki in Finland that is similar to UNIX as an operating system.
2. Which of the following is similar to UNIX OS?
a) Windows NT
b) MS-DOS
c) Linux
d) Windows 3.1
View Answer
Answer: c
Explanation: The Linux is similar to UNIX operating system but it is entirely different for the Windows NT, MS-DOS and the Windows 3.1

3. Who had first described UNIX in an article?
a) Ken Thompson
b) Dennis Ritchie and Ken Thompson
c) Dennis Ritchie
d) Linus Torvalds
View Answer
Answer: b
Explanation: The UNIX was first described by Dennis Ritchie and Ken Thompson of Bell Research Labs in 1974 through an article.
4. What does MULTICS stand for?
a) multiplexed information and computing service
b) multiplexed information and code service
c) multiplexed inter-access code service
d) multiplexed inter-code sensor
View Answer
Answer: a
Explanation: MULTICS is a multiplexed information and computing service which generate software that would allow a large number of users for accessing the computer simultaneously.
5. Which of the following is the first version of the UNIX operating system?
a) PDP-2
b) Linux
c) MS-DOS
d) PDP-7
View Answer
Answer: d
Explanation: The PDP-7 processor is the first version of the UNIX which has a new filing system and new utilities.
6. Which of the following is a UNIX clone?
a) XENIX
b) Windows 3.1
c) Windows NT

d) Linux
View Answer
Answer: a
Explanation: The XENIX is a UNIX clone developed by the Motorola in the year 2979 and is ported to many processors.
7. Which of the following is an alternate source of UNIX?
a) MS-DOS
b) Windows 3.1
c) Windows NT
d) Linux
View Answer
Answer: a
Explanation: With the many disadvantages of the UNIX operating system, Linux was used as an alternative source. The UNIX operating system was more expensive operating system and most of the hardware was specific to the manufacturer, which restricted the use of UNIX and developed for an alternative one, the Linux.
8. Which of the following are grouped into directories and subdirectories?
a) register
b) memory
c) files
d) routines
View Answer
Answer: c
Explanation: The files are grouped into directories and subdirectories. This file system contains all the data files, commands, programs and special files which allow the access to the physical computer system. The file system of the Linux operating system is similar to the UNIX operating system.
9. Which character is known as a root directory?
a) ^
b) &
c) &&
d) /

Answer: d
Explanation: The character / is used at the beginning of the file name or the path name which is used as the starting point and is known as the root directory or root.
10. How many types of Linux files are typically used?
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: c

1. Which filesystem of Linux has mass storage devices?
a) physical file system
b) temporary file system
c) ram
d) register
View Answer
Answer: a
Explanation: The physical file system has mass storage devices such as hard disks and floppy which are allocated to parts of the logical file system.
2. Which file type of Linux has no restriction on size and can have any kind of data?
a) special
b) regular
c) directories
d) named pipes
View Answer
Answer: b
Explanation: There are four types of Linux files. These are regular, special, directories and named pipes in which the regular file type can have any kind of data and does not have restrictions in size, the special file type represent certain terminals such

as physical I/O device, the directories can hold lists of files, and the named pipes are similar to regular files but restricted in size.

3. Which file type of Linux is similar to the regular file type?

a) named pipe
b) directories
c) regular file
d) special file

View Answer

Answer: a

Explanation: Among the Linux files, the regular file type is similar to the named pipe but these are restricted in size. On the other hand, the regular file does not have restrictions.

4. Which file type of the Linux hold lists of files rather than the actual data?

a) regular
b) special
c) directories
d) named pipes

View Answer

Answer: c

Explanation: The directories can hold lists of files other than the actual data, but the other file type does not have this characteristic.

5. Which filesystem of the Linux can be implemented on a system with two hard disks?

a) logical file system
b) physical file system
c) special file type system
d) regular file type system

View Answer

Answer: a

Explanation: The physical file system is allocated to the parts of the logical file system. The logical file system can be implemented on a system with two hard disks by the allocation of the bin directory under the hard disk 1 and the file subsystem under the hard disk 2.

6. Which directory is allocated on the hard disk 1 of the physical storage in a Linux operating system?
a) term
b) dev
c) etc
d) bin
View Answer
Answer: d
Explanation: The bin directory is on the hard disk 1 of the physical storage whereas the term, dev, etc is on the hard disk 1 of the physical logical file system.
7. Which process defines the allocation of the mass storage to the logical file system?
a) mounting
b) de-allocation
c) demounting
d) unmounting
View Answer
Answer: a
Explanation: The allocation of the mass storage to the logical file system is known as the mounting and its reverse operation, deallocation of the mass storage is known as unmounting.
8. Which commands can be used to access the removable media?
a) system calls
b) loop instruction
c) mount and unmount command
d) procedure commands
View Answer
Answer: c
Explanation: The commands such as mount and unmount commands are used to access the removable media like the floppy disks, through the logical file system.
9. Which target directory is used in the file system of the Linux operating system?
a) /mnt
b) /etc

c) /term
d) /bin
View Answer
Answer: a

1. Identify the standard software components that can be reused?
a) application manager
b) operating system
c) application software
d) memory
View Answer
Answer: b
Explanation: There are certain software components that can be reused in an embedded system design. These are the operating systems, real-time databases and some other forms of middleware.
2. What does WCTE stand for?
a) wait case execution time
b) wait case encoder time
c) worst case execution time
d) worst code execution time
View Answer
Answer: c
Explanation: The WCTE is the worst case execution time which is an upper bound on the execution times of task. It can be computed for certain programs like while loops, programs without recursion, iteration count etc.
3. For which of the following WCET can be computed?
a) C program
b) assembly language
c) VHDL

d) program without recursion
View Answer
Answer: d
Explanation: The WCET computing is a difficult task for assembly language and for computing WCTE for any high-level language without the knowledge of the generated assembly code is impossible.
4. The WCET of which component can be computed if the task is mapped to hardware?
a) hardware
b) task
c) both task and hardware
d) application manager
View Answer
Answer: a
Explanation: The worst case execution time of the hardware can be computed if the task is mapped to the hardware which in turn requires the synthesis of the hardware.
5. Which estimation approach is used by Jha and Dutt for hardware?
a) accurate cost and performance value
b) estimated cost and performance value
c) performance value
d) accurate cost
View Answer
Answer: b
Explanation: There are different estimation techniques used. One such is the estimated cost and performance value which is proposed by Jha and Dutt for hardware. The accurate cost and performance value is proposed by Jain et al for software.
6. Which estimate approach is more precise?
a) estimated cost and performance value
b) accurate cost and performance value
c) performance value and execution time
d) estimated cost
View Answer

Answer: b
Explanation: The accurate cost and performance value is possible if interfaces to software synthesis tools and hardware synthesis tools exist and is more precise than any other methods.
7. Which estimate approach takes more time to consume?
a) accurate value
b) estimated value
c) accurate cost and performance value
d) estimated cost and performance value
View Answer
Answer: c
Explanation: The accurate cost and the performance value method is time-consuming but the other estimating approaches are less time consuming.
8. Which estimation technique can be used if interfaces to software synthesis tools and hardware synthesis tools exist?
a) performance value
b) estimated cost
c) estimated cost and performance value
d) accurate cost and performance value
View Answer
Answer: d
Explanation: The accurate cost and performance value is possible if interfaces to software synthesis tools and hardware synthesis tools exist.
9. Which of the following is the base for scheduling algorithm?
a) WCET
b) time
c) execution time
d) address accessing time
View Answer
Answer: a

1. Which classification is based on the extension to standard operating systems?
a) software and hardware deadline
b) aperiodic deadline
c) periodic deadline
d) static and dynamic deadline
View Answer
Answer: a
Explanation: The real-time scheduling can be classified into various criteria. The fundamental classification is the software and hardware deadline which is based on the extension to standard operating systems.
2. Which of the following defines the task which must be executed at every defined unit of time?
a) aperiodic task
b) periodic task
c) job
d) process
View Answer
Answer: b
Explanation: The periodic task is the one which must be executed in a defined unit of time say ‘p’ where p is called the period.
3. Which of the task are not periodic?
a) periodic task
b) unpredictable task
c) aperiodic task
d) job
View Answer
Answer: c
Explanation: The aperiodic task is the one in which the task is not periodic but the periodic task is the one in which are the task are periodic. Each execution of a periodic task is known as the job.
4. Which of the following is an aperiodic task requesting the processor at unpredictable times?
a) job
b) aperiodic task
c) sporadic

d) periodic task
View Answer
Answer: c
Explanation: The aperiodic tasks request the processor at unpredictable times if and only if there is a minimum separation between the times at which they request the processor which is called sporadic.
5. Which of the scheduling algorithm are based on the assumption that tasks are executed until they are done?
a) periodic task
b) aperiodic task
c) non-preemptive scheduling
d) preemptive scheduling
View Answer
Answer: c
Explanation: The nonpreemptive scheduling is based on the assumptions that the tasks are executed until the task is done whereas the preemptive scheduling is used if the task has long execution times or for a short response time.
6. Which of the following schedulers take decisions at run-time?
a) preemptive scheduler
b) non preemptive scheduler
c) dynamic scheduler
d) static scheduler
View Answer
Answer: c
Explanation: The dynamic schedulers take decisions at run-time and they are quite flexible but generate overhead at run-time whereas static scheduler is the ones in which the scheduler take their designs at the design time.
7. Which scheduler takes their designs at design time?
a) preemptive scheduler
b) non preemptive scheduler
c) dynamic scheduler
d) static scheduler
View Answer

Answer: d
Explanation: The static scheduler take their designs at the design time and it also generates tables of start times which are forwarded to a simple dispatcher but the dynamic scheduler takes a decision at the run-time.
8. Which scheduler generates tables and forward to the dispatcher?
a) static scheduler
b) dynamic scheduler
c) aperiodic scheduler
d) preemptive scheduler
View Answer
Answer: a
Explanation: The static scheduler generates tables of start times which are forwarded to a simple dispatcher and it can be controlled by a timer which makes the dispatcher analyze the table.
9. Which of the following systems are entirely controlled by the timer?
a) voltage triggered
b) time triggered
c) aperiodic task scheduler
d) periodic task scheduler
View Answer
Answer: b
Explanation: The systems which are entirely controlled by a timer are known as entirely time-triggered systems. A temporal control structure is associated with the entirely time-triggered system which is encoded in a TDL, task descriptor list.
10. What does TDL stand for?
a) task descriptor list
b) task design list
c) temporal descriptor list
d) temporal design list
View Answer
Answer: a
Explanation: TDL is a task descriptor list which contains the cyclic schedule for all activities of the node and the temporal control structure is encoded by the task descriptor table.

11. Which scheduling algorithm can be used in mixed software/hardware systems?
a) simple algorithm
b) complex algorithm
c) uniprocessor algorithm
d) multiprocessor algorithm
View Answer
Answer: b
Explanation: The complex algorithm is used in mixed software/hardware systems. It can be used to handle multiple processors.
12. Which algorithm can distinguish homogeneous multiprocessor system and heterogeneous multiprocessor system?
a) complex algorithm
b) simple algorithm
c) scheduler algorithm
d) preemptive algorithm
View Answer
Answer: a
Explanation: The simple algorithm can be used in handling single processors and the complex algorithm is used in mixed both in software and the hardware systems. It can also be used to distinguish homogeneous multiprocessor system and heterogeneous multiprocessor systems. The complex algorithm can be used to handle multiple processors whereas.
13. Which of the following scheduling test can be used to show that no scheduling exist?
a) sufficient test
b) necessary test
c) complex test
d) simple test
View Answer
Answer: b
Explanation: The necessary and sufficient conditions are used in the schedulability test. For necessary condition, the test is based only on the necessary conditions and it also can be used to show that no schedule exists. The sufficient condition indicates that no schedule exists even if there exists one.
14. Which scheduling test is used to indicate that no scheduling exist even if there exist one?
a) complex test

b) simple test
c) sufficient test
d) necessary test
View Answer
Answer: c
Explanation: The sufficient condition indicates that no schedule exists even if there exist one and the necessary condition indicates that no schedule exists even if a schedule exists.
15. Which algorithm can be used to schedule tasks at run-time?
a) online scheduler
b) offline scheduler
c) multiprocessor scheduler
d) uniprocessor scheduler
View Answer
Answer: a

1. Which algorithm is based on Jackson's rule?
a) EDD
b) LL
c) EDF
d) LST
View Answer
Answer: a
Explanation: The EDD or earliest due date is based on Jackson's rule. The Jackson's rule states that for a given a set of n independent tasks, any algorithm that executes the tasks in the order of nondecreasing deadlines is optimal with respect to reducing the maximum lateness. EDF is the earliest deadline first, LL is the least laxity and the LST is the least slack time first.
2. What does EDD stand for?
a) earliest device date
b) earliest due date
c) earliest device deadline

d) earliest deadline device
View Answer
Answer: b
Explanation: The earliest due date requires all tasks to be sorted by their deadlines and it is based on Jackson's rule. If the deadlines are known, EDD algorithm can be used.
3. Which of the following can be implemented as static scheduling algorithm?
a) EDF
b) LL
c) EDD
d) LST
View Answer
Answer: c
Explanation: The EDD can be implemented as static scheduling algorithm if the deadlines are known in advance and it follows Jackson's rule.
4. What does EDF stand for?
a) earliest deadline fix
b) earliest due fix
c) earliest due first
d) earliest deadline first
View Answer
Answer: d
Explanation: The EDF stands for earliest deadline first. This algorithm is optimal with respect to minimizing the maximum lateness and is implemented as dynamic scheduling algorithm for a set of n independent tasks with arbitrary arrival times, any algorithm that at any instant executes the task with the earliest absolute deadline among all the ready tasks is optimal with respect to minimizing the maximum lateness.
5. Which algorithm is dynamic scheduling algorithm?
a) LL
b) LST
c) EDF

d) EDD
View Answer
Answer: c
Explanation: The EDF or earliest deadline first can be implemented as a dynamic scheduling algorithm.
6. In which scheduling, the task priorities are a monotonically decreasing function of laxity?
a) LL
b) EDD
c) EFD
d) LST
View Answer
Answer: a
Explanation: In the least laxity algorithm, the laxity can be changed dynamically which shows that the task priorities are a monotonically decreasing function of laxity.
7. Which scheduling algorithm is an optimal scheduling policy for mono-processor system?
a) preemptive algorithm
b) LST
c) EDD
d) LL
View Answer
Answer: d
Explanation: The least laxity algorithm is a dynamic scheduling algorithm and hence it can be implemented as an optimal scheduling policy for the mono-processor system. The LL scheduling algorithm is also preemptive scheduling.
8. Which scheduling algorithm cannot be used with a standard OS providing fixed priorities?
a) LL
b) LST
c) EDD
d) EFD
View Answer

Answer: a
Explanation: The least laxity algorithm cannot be used with a standard OS providing fixed priorities because of its dynamic property.
9. Who proposed the LDF algorithm?
a) Bayes
b) Nyquist
c) Lawler
d) Stankovic
View Answer
Answer: c
Explanation: The latest deadline first or LDF is proposed by Lawler which performs a topological sort. It is based on the total order compatible with the partial order with respect to the task graph.
10. What does LDF stand for?
a) last deadline first
b) least deadline first
c) list deadline first
d) latest deadline first
View Answer
Answer: d
Explanation: The LDF or latest deadline first is a scheduling algorithm which is proposed by Lawler.
11. Which algorithm is non-preemptive and can be used with a mono processor?
a) LDF
b) pre-emptive
c) aperiodic
d) LL
View Answer
Answer: a
Explanation: The latest deadline first or LDF is a non-preemptive scheduling algorithm and can be used with a mono processor whereas LL or least laxity is a preemptive scheduling algorithm.

12. Which algorithm requires the periodic checks of the laxity?
a) LST
b) LL
c) EDD
d) EFD
View Answer
Answer: b
Explanation: The LL scheduling algorithm requires the knowledge of the execution times and the periodic check of the laxity.
13. Who developed the heuristic algorithm?
a) Stankovic and Ramamritham
b) Stankovic and Lawler
c) Lawler
d) Stankovic
View Answer
Answer: a
Explanation: The heuristic algorithm is developed by Stankovic and Ramamritham in 1991.
14. Which algorithm can be used if the preemptive is not allowed?
a) heuristic algorithm
b) LL
c) EDD
d) LST
View Answer
Answer: a
Explanation: The heuristic algorithm was proposed by Stankovic and Ramamritham in 1991 can be used if the preemption is not allowed.
15. Deadline interval – execution time =
a) laxity
b) execution time
c) deadline interval

d) period
View Answer
Answer: a

1. The execution of the task is known as
a) process
b) job
c) task
d) thread
View Answer
Answer: b
Explanation: The execution of the task is known as the job. The time for both the execution of the task and the corresponding job is same.
2. Which scheduling algorithm is can be used for an independent periodic process?
a) EDD
b) LL
c) LST
d) RMS
View Answer
Answer: d
Explanation: The RMS os rate monotonic scheduling is periodic scheduling algorithm but EDD, LL, and LST are aperiodic scheduling algorithm.
3. What is the relationship between the priority of task and their period in RMS?
a) decreases
b) increases
c) remains unchanged
d) linear
View Answer

Answer: a
Explanation: The priority of the task decreases monotonically with respect to their period in the rate monotonic scheduling, that is, the task with the long period will get a low priority but task with the short period will get a high priority.
4. Which of the following uses a preemptive periodic scheduling algorithm?
a) Pre-emptive scheduling
b) RMS
c) LL
d) LST
View Answer
Answer: b
Explanation: The rate monotonic scheduling is a periodic scheduler algorithm which follows a preemptive algorithm. LL is also preemptive scheduling but it is aperiodic scheduling algorithm.
5. Which of the following is based on static priorities?
a) Periodic EDF
b) RMS
c) LL
d) Aperiodic EDF
View Answer
Answer: b
Explanation: The rate monotonic scheduling is a periodic scheduler algorithm which follows a preemptive algorithm and have static priorities. EDF and LL have dynamic priorities.
6. How many assumptions have to meet for a rate monotonic scheduling?
a) 3
b) 4
c) 5
d) 6
View Answer
Answer: d
Explanation: The rate monotonic scheduling has to meet six assumptions. These are: All the tasks should be periodic, all the

tasks must be independent, the deadline should be equal to the period for all tasks, the execution time must be constant, the time required for the context switching must be negligible, it should hold the accumulation utilization equation.

7. Which of the following can be applied to periodic scheduling?

a) EDF
b) LL
c) LST
d) EDD

View Answer

Answer: a

Explanation: The earliest deadline first can be applied both to the periodic and aperiodic scheduling algorithm. But LL, LST, and EDD are aperiodic scheduling. It is not applicable to the periodic scheduling.

8. Which of the following periodic scheduling is dynamic?

a) RMS
b) EDF
c) LST
d) LL

View Answer

Answer: b

Explanation: The EDF or the earliest deadline first is a periodic scheduling algorithm which is dynamic but RMS or rate monotonic scheduling is the periodic algorithm which is static. The LL and LST are aperiodic scheduling algorithm.

9. Which of the following do the sporadic events are connected?

a) Interrupts
b) NMI
c) Software interrupt
d) Timer

View Answer

Answer: a

Explanation: The sporadic events are connected to the interrupts thereby execute them immediately as possible since the interrupt priority is the highest in the system.

10. Which of the following can execute quickly, if the interrupt priority is higher in the system?
a) EDD
b) Sporadic event
c) LL
d) Aperiodic scheduling
View Answer
Answer: b
Explanation: The sporadic events are connected to the interrupts and execute them immediately because the interrupt priority is the highest priority level in the system.
11. Which of the following are used to execute at regular intervals and check for ready sporadic tasks?
a) sporadic task server
b) sporadic task client
c) sporadic event application
d) sporadic register
View Answer
Answer: a
Explanation: The special sporadic task servers are used that execute at regular intervals and check for ready sporadic tasks which improve the predictability of the whole system.
12. How is a sporadic task can turn into a periodic task?
a) scheduling algorithm
b) sporadic task event
c) sporadic register
d) sporadic task server
View Answer
Answer: d
Explanation: The special sporadic task servers execute at regular intervals and check for ready sporadic tasks and by this, sporadic tasks are essentially turned into periodic tasks which can improve the predictability of the whole system.
13. Which of the following is more difficult than the scheduling independent task?
a) scheduling algorithm
b) scheduling independent task

c) scheduling dependent task
d) aperiodic scheduling algorithm
View Answer
Answer: c
Explanation: The scheduling dependent task is more difficult than the independent scheduling task. The problem of deciding whether or not a schedule exists for a given set of dependent tasks and a given deadline is NP-complete.
14. Which scheduling is the basis for a number of formal proofs of schedulability?
a) LL
b) RMS
c) LST
d) EDD
View Answer
Answer: b
Explanation: The rate monotonic scheduling which is an independent scheduling algorithm form the basis for a number of formal proofs of schedulability.
15. Which of the following is independent scheduling?
a) LL
b) LST
c) EDD
d) RMS
View Answer
Answer: d

1. Which allows the parallel development of the hardware and software in the simulation?
a) high-level language simulation
b) low-level language simulation
c) cpu simulator

d) onboard simulator
View Answer
Answer: a
Explanation: The high-level language simulation allows parallel development of the software and the hardware and when two parts are integrated, that will work. It can simulate I/O using the keyboard as the inputs or task which passes input data for other modules.
2. Which of the following are used to test the software?
a) data entity
b) data entry
c) data table
d) data book
View Answer
Answer: c
Explanation: In the high-level language simulation, many techniques are used to simulate the system and one such is the data table which contains the data sequences which are used to test the software.
3. Which allows the UNIX software to be ported using a simple recompilation?
a) pSOS+
b) UNIX compatible library
c) pSOS+m
d) pOS+kernel
View Answer
Answer: b
Explanation: The most of the operating system support or provide the UNIX-compatible library which supports the UNIX software to be ported using a simple recompilation.
4. Which of the following can simulate the processor, memory, and peripherals?
a) input simulator
b) peripheral simulator
c) memory simulator

d) cpu simulator
View Answer
Answer: d
Explanation: The CPU simulator can simulate the memory, processor, and the peripherals and allow the low-level assembler code and the small HLL programs to be tested without the actual hardware.
5. How many categories are there for the low-level simulation?
a) 2
b) 3
c) 4
d) 5
View Answer
Answer: a
Explanation: There are two categories for the low-level simulation. The first category simulates the memory system, programming model and can offer simple debugging tools whereas the second category simulation provides timing information based on the number of clocks.
6. Which of the following can simulate the LCD controllers and parallel ports?
a) memory simulator
b) sds
c) input simulator
d) output tools
View Answer
Answer: b
Explanation: There are certain tools which provide powerful tools for simulation and one such is the SDS which can simulate the processor, memory systems, integrated processor, onboard peripherals such as LCD controllers and parallel ports.
7. Which of the following provides a low-level method of debugging software?
a) high-level simulator
b) low-level simulator
c) onboard debugger

d) cpu simulator
View Answer
Answer: c
Explanation: The onboard debugger provides a very low-level method of simulating or debugging the software. It usually handles EPROMs which are plugged into the board or a set of application codes by providing a serial connection to communicate with the PC or workstation.
8. Which of the following has the ability to download code using a serial port?
a) cpu simulator
b) high-level language simulator
c) onboard debugger
d) low-level language simulator
View Answer
Answer: c
Explanation: The onboard debugger has the ability to download code from a floppy disk or by using a serial port.
9. What does the processor fetch from the EPROM if the board is powered?
a) reset vector
b) ready vector
c) start vector
d) acknowledge vector
View Answer
Answer: a
Explanation: The processor fetches its reset vector from the table which is stored in the EPROM when the board is powered and then starts the initialize the board.
10. Which of the following device can transfer the vector table from the EPROM?
a) ROM
b) RAM
c) CPU
d) peripheral
View Answer

Answer: b
Explanation: When the board gets powered up, the reset vector from the table stored in the EPROM makes the initialisation of the board and is transferred to the RAM from the EPROM through the hardware where the EPROM memory address is temporarily altered.
11. Which of the following is used to determine the number of memory access in an onboard debugger?
a) timer
b) counter
c) input
d) memory
View Answer
Answer: b
Explanation: The counter is used to determine a preset number of memory accesses, which is assumed that the table has been transferred by the debugger and the EPROM address can be safely be changed.
12. Which of the following has the ability to use the high-level language functions, instructions instead of the normal address?
a) task level debugging
b) low level debugging
c) onboard debugging
d) symbolic debugging
View Answer
Answer: d
Explanation: The symbolic debugging has the ability to use high-level language functions, instructions and the variables instead of the normal addresses and their contents.
13. Which of the following debugger works at the operating system level?
a) task level debugging
b) low level debugging
c) onboard debugging
d) symbolic debugging
View Answer
Answer: a

1. Which of the following has a single set of compiler and the debugger tools?
a) Xray
b) onboard debugger
c) emulation
d) high-level simulator
View Answer
Answer: a
Explanation: The Xray debugging technique is a product from the Microtec which is having a complete set of compiler and debugger tools which will work with the simulator, debugger, emulator and the onboard debugger.
2. Who developed the Xray product?
a) IBM
b) Intel
c) Microtec
d) Motorola
View Answer
Answer: c
Explanation: The Xray which is a product from the Microtec is having a complete set of compiler and debugger tools.
3. Which part of the Xray can interface with a simulator?
a) emulator
b) debugger
c) simulator
d) onboard debugger
View Answer
Answer: b
Explanation: The Xray consists of the consistent debugger which can interface the emulator, simulator, task level debugger or onboard debugger.
4. Which can provide the consistent interface to the Xray?
a) emulator
b) simulator

c) memory simulator
d) debugger system
View Answer
Answer: d
Explanation: The Xray consists of the debugger which interfaces with the emulator, simulator, onboard debugger that provides the consistent interface to the Xray product. This can improve the overall productivity of the product since it does not require any relearning.
5. Which of the following can access the information directly in the Xray?
a) emulator
b) debugger
c) simulator
d) hardware
View Answer
Answer: c
Explanation: The Xray obtain its debugging information from a variety of sources and how it access these sources. The simulator can access direct information but the emulator can access the information via a serial line or via the ethernet or directly across a shared memory interface.
6. Which of the following access the information through the ethernet in a Xray?
a) simulator
b) debugger
c) onboard debugger
d) emulator
View Answer
Answer: d
Explanation: The Xray obtain its debugging information from a variety of sources. The emulator can access the information via a serial line or via the ethernet or directly across a shared memory interface and the simulator can access the direct information.
7. Which tools help the Xray allows the software to be developed on the host system?
a) compiler tool
b) simulator tool

c) debugger tool
d) emulator tool
View Answer
Answer: a
Explanation: The compiler tools allow the software to be developed on the host system and this system does not have to use the same processor as the target.
8. Which of the following is ideal for debugging codes at an early stage?
a) compiler
b) debugger
c) simulator
d) emulator
View Answer
Answer: c
Explanation: There are a variety of ways for executing the codes. The simulator provides an ideal way for debugging the codes at an early stage, that is before the hardware is available and it can allow the software to proceed in parallel with the hardware.
9. How can we extend the power of Xray?
a) Xray interface
b) Xray memory
c) Xray input
d) Xray peripheral
View Answer
Answer: a
Explanation: The power of the Xray product can be extended by the Xray interface method from the operating system debugger.
10. Which of the following uses the Xray interface method to provide the debugging interface?
a) pSOS+m
b) pSOS
c) pSOS+

d) NAP
View Answer
Answer: c
Explanation: The pSOS+ uses the Xray interface method to provide the debugging interfaces which can extend the power of the Xray.
11. How is the processor enter into a BDM state?
a) BDM signal
b) Start signal
c) BDM acknowledge signal
d) Start signal of the processor
View Answer
Answer: a

1. What does ICE stand for?
a) in-circuit emulation
b) in-code EPROM
c) in-circuit EPOM
d) in-code emulation
View Answer
Answer: a
Explanation: The ICE or in-circuit emulation is one the traditional method used to emulate the processor in the embedded system so that the software can be downloaded and can be debugged in situ in the end application.
2. Which of the following is a traditional method for emulating the processor?
a) SDS
b) ICE
c) CPU simulator
d) Low-level language simulator
View Answer

Answer: b
Explanation: The SDS is one of the simulation tool used in the embedded systems. CPU simulator and the low-level simulator are the other kinds of the simulator used in the embedded system design.
3. Which of the following does not have the ability to get hundred individual signal cables into the probe in the emulation technique?
a) OnCE
b) BDM
c) ICE
d) JTAG
View Answer
Answer: c
Explanation: The in-circuit emulation does not have the ability to get a hundred individual signal cables into the probe. This problem comes under the physical limitation of the probe, that is as the density of the processor increases the available sockets which provide good electrical contacts is becoming harder which causes a restriction to the probe.
4. What does JTAG stand for?
a) joint tag address group
b) joint test address group
c) joint test access group
d) joint test action group
View Answer
Answer: d
Explanation: The JTAG is a joint test action group which is an electronics industry association which developed the interfacing port that is standardised for testing the devices.
5. Which of the following allows access to all the hardware within the system?
a) debugger
b) JTAG
c) onboard debugger
d) simulator
View Answer

Answer: b
Explanation: The JTAG can access all the hardware within the system. They provide a way of taking over the pins of a device and allows the different bit patterns to be imposed on the pins which allow other circuits to be tested with the imposed pins.
6. Which of the following works by using a serial port?
a) Simulator
b) JTAG
c) BDM
d) OnCE
View Answer
Answer: b
Explanation: The JTAG works by using a serial port and clocking data into a shift register and the output of the shift register drives the pins under the control of the port.
7. What is meant by OnCE?
a) on-chip emulation
b) off-chip emulation
c) one-chip emulation
d) once-chip emulation
View Answer
Answer: a
Explanation: The OnCE is an on-chip emulation which is a debugging facility used in the digital signal processor chips.
8. Which debugging facility is used in the Motorola's DSP 56x0x family?
a) JTAG
b) ICE
c) OnCE
d) BDM
View Answer
Answer: c
Explanation: The on-chip emulation provides a debugging facility in the DSP chips. The OnCE is developed for Motorola's DSP 56x0x family.

9. Which facility provides the provision of the debug ports in the ICE technique?
a) simulator
b) emulator
c) debug support
d) jtag
View Answer
Answer: c
Explanation: The debugging support to the processor enables the processor to be a single stepped and breakpoint under remote control from a host or the workstation. This facility can provide the provision of the debug ports.
10. How the additional registers are accessed in the OnCE?
a) parallel port
b) serial port
c) jtag
d) address register
View Answer
Answer: b
Explanation: The on-chip emulation can access additional registers by using a special serial port within the device that provides control over the processor and access to its internal registers.
11. Which of the following emulators can provide its own in circuit emulation facility?
a) Simulator
b) Debugger
c) SDS
d) OnCE
View Answer
Answer: d
Explanation: Every system can provide its own in circuit emulation facilities by hooking the port to an interface port in a workstation or in the PC while connecting the OnCE port to an external connector.
12. What does BDM stand for?
a) background debug mode
b) basic debug mode

c) basic debug microcode
d) background decode mode
View Answer
Answer: a
Explanation: The BDM or background debug mode is similar to the on-chip emulator with a slight difference. BDM is provided on the Motorola MC683xx series of processors and for the 8-bit microcontroller like MC68HC12 etc.
13. Which emulator is used in MC68HC12?
a) JTAG
b) BDM
c) On-CE
d) SDS
View Answer
Answer: b
Explanation: The BDM or the background debug mode is provided on the Motorola MC683xx series of processors and for several 8-bit microcontrollers. One such microcontroller is the MC68HC12.
14. Which of the following takes the processor, when the processor enters the BDM mode?
a) address code
b) high-level microcode
c) low-level microcode
d) data code
View Answer
Answer: c
Explanation: When the processor enters into the BDM mode, low-level microcode takes the processor which allows the breakpoint to be set, registers to be accessed and so on.
15. Which of the following has the additional circuitry which supports the background debug mode?
a) memory
b) input
c) peripheral

d) processor
View Answer
Answer: d

1. Which of these is an area for temporary memory storage?
a) buffer
b) register
c) table
d) flag
View Answer
Answer: a
Explanation: The buffer is an area that is used to store data temporarily which can be used to compensate the timing problems.
2. Which of the following can be used as a collection point of data?
a) register
b) buffer
c) flag register
d) accumulator
View Answer
Answer: b
Explanation: The buffer can be used as a collection point for data, that is all the important information can be collected and organised before processing.
3. Which device can compensate for the timing problems between the software?
a) index
b) register
c) buffer
d) memory
View Answer

Answer: c
Explanation: The buffer is used to store data temporarily which can be used to compensate the timing problems between the software and it can also be used as a collection point for data, that is all the important information can be collected and organised before processing.
4. What do a buffer consist of?
a) memory and register
b) memory and peripheral
c) memory and flag register
d) memory and pointer
View Answer
Answer: d
Explanation: The buffer consists of a pointer and memory which can be used to locate the next piece of data to be removed or accessed from the buffer.
5. Which of the following is a condition for buffer overrun?
a) cannot accept data
b) cannot receive data
c) cannot provide data
d) can provide data
View Answer
Answer: a
Explanation: The buffer involves two conditions. These are the buffer overrun condition and the buffer underrun condition. If the buffer cannot accept any more data, it is said to be buffer overrun.
6. What is the state of the buffer if it asked for data and cannot provide it?
a) overrun
b) underrun
c) remains unchanged
d) beyond overrun
View Answer

Answer: b
Explanation: The buffer is said to be overrun if the buffer cannot accept any more data and said to be underrun if it asked for data but not able to provide it.
7. Which of the following can remove data from the buffer?
a) memory
b) ram
c) pointer
d) slack
View Answer
Answer: c
Explanation: The data can be removed from the buffer using a pointer. The pointer locates the next value and can move the data from the buffer and is moved to the next location by incrementing its value by the number of words or bytes.
8. How many bits does a 32-bit processor can access?
a) 32-bit char
b) 32-bit word
c) 32-bit double
d) 32-bit double word
View Answer
Answer: b
Explanation: The 32-bit processor can access 32-bit word and hence the pointer is incremented by one.
9. What occurs first if data is stored in the buffer?
a) speed increases
b) linear shoot
c) overshoot
d) delay
View Answer
Answer: d
Explanation: When the data is stored in the buffer, at first there will be a delay and the subsequent data is received from the buffer. This delay is known as buffer latency.

10. Which of the following defines the earliest information that is passed through the buffer?
a) buffer latency
b) memory
c) pointer
d) peripheral
View Answer
Answer: a
Explanation: The buffer latency determines the earliest information that passes through the buffer and any response to that information will be delayed by the buffer latency irrespective of how fast the processor is.
11. Which of the following possesses a problem for data streams on the real-time operating system?
a) pointer
b) memory
c) latency
d) processor
View Answer
Answer: c
Explanation: The latency will be a problem for the real-time operating system such as the digital audio system which must have a consistent and regular stream of data.
12. Which of the following determines the time to take a simple sample?
a) buffer
b) latency
c) pointer
d) memory
View Answer
Answer: b
Explanation: The sampling is performed on a regular basis in which the filtering takes less time than the interval between the sample and this does not need a buffering and it will have very low latency. Each sample is received, processed and stored and the latency is the time take a single sample.
13. How is a stack created?
a) slack and pointer

b) stack and memory
c) memory and a pointer
d) memory and a register
View Answer
Answer: d
Explanation: The slack is created in the same way as the buffer does, that is by using a memory and a pointer. The control associated with the buffer or memory is a register which acts as an address pointer.
14. Which of the following acts as an address pointer?
a) memory
b) pointer
c) stack
d) register
View Answer
Answer: d
Explanation: The control associated with the buffer or memory is a register which acts as an address pointer.
15. Which of the following possesses an issue while concerning the memory size of the buffer?
a) digital signal processor
b) microprocessor
c) memory
d) pointer
View Answer
Answer: a

1. Which of the buffers has a single piece of linear contiguous memory?
a) circular buffer
b) linear buffer
c) directional buffer
d) double buffer
View Answer

Answer: b
Explanation: The linear buffer is contiguous memory which is a single piece memory that is controlled by the pointers whose address increments linearly.
2. Which buffer will lose data when it is full?
a) linear buffer
b) circular buffer
c) directional buffer
d) double buffer
View Answer
Answer: a
Explanation: The linear buffer has a single piece of contiguous memory which is controlled by the pointers whose address increments linearly and it will lose data when it is full and fail to provide data when it is empty.
3. Which of the following buffers loses the incoming data when it is full?
a) circular buffer
b) double buffer
c) linear buffer
d) directional buffer
View Answer
Answer: c
Explanation: The linear buffer will lose the incoming data when full such that the data it contains become older, which is known as the overrun condition.
4. Which state of the linear buffer will provide old data, when it is empty?
a) overrun
b) critical timing
c) peak overshoot
d) underrun
View Answer
Answer: d
Explanation: In the linear buffer, when it is empty it will provide the old data, usually the last entry so that the processor will continue to process the incorrect data potentially, and this condition is known as underrun.

5. Which state of the linear buffer loses its incoming data when full?
a) underrun
b) overrun
c) critical time
d) pointer
View Answer
Answer: b
Explanation: In the overrun condition, the linear buffer will lose the incoming data when the buffer is filled and the data it contains become older.
6. Which technique can solve the errors in the linear buffer?
a) low water mark
b) high water mark
c) low and high water mark
d) pointer
View Answer
Answer: c
Explanation: The errors in the linear buffering include the loss of data especially during the regular sampling which can be avoided by the pointers that are checked against certain values and this result is used for fetching more data. These points are known as the low water mark and the high water mark.
7. Which of the following is similar to the high and low water marks at the coast?
a) minimum and maximum water level
b) low and high water mark
c) small and big water mark
d) medium and high water mark
View Answer
Answer: b
Explanation: There are some errors in the linear buffering which includes the loss of data especially in the regular sampling. This can be avoided by the pointers that are checked against certain values and the result is used to fetch more data. These points are known as the low water mark and the high water mark. It is named so because it is similar to the high and low water marks seen at the coast which indicates the maximum and minimum levels that the tidal water will fall and rise.

8. Which of the following determines the number of entries in the buffer?
a) low water mark
b) high water mark
c) low and high water mark
d) small and big water mark
View Answer
Answer: a
Explanation: The number of entries below the low water mark determines the number of entries the buffer has and the amount of time which is available to fill the buffer before empties and the condition is known as underrun.
9. Which of the following determines the number of empty entries?
a) low water tank
b) high water tank
c) small water tank
d) big water tank
View Answer
Answer: b
Explanation: The high water tank measures the number of empty entries, that is the number of empty entries above the high water tank determines the length of time which is available to stop the filling of the buffer and it can prevent the data loss through overrunning.
10. In which case, the buffer is used by two software task?
a) single buffer
b) linear buffer
c) double buffer
d) directional buffer
View Answer
Answer: a
Explanation: In the single buffer, the buffer is used by two software tasks to insert or extract information. The problem with this buffer is that the water level is above or below, and the free space that is used to fill the buffer does not lie in the correct location.

11. Which buffer is important for the signal data?
a) double buffer
b) single buffer
c) linear buffer
d) directional buffer
View Answer
Answer: d
Explanation: The directional buffer is used for the signal data or for the data which is sampled periodically. The data must be kept in the same order in order to preserve it in chronological order.
12. Which of the following uses two buffers?
a) linear buffer
b) single buffer
c) double buffer
d) directional buffer
View Answer
Answer: c
Explanation: The double buffer uses buffers as its name suggest, one buffer is for filling and the other buffer is for extraction.
13. Which of the following uses a single low water tank and a next data pointer?
a) single buffer
b) double buffer
c) directional buffer
d) linear buffer
View Answer
Answer: a

1. Which of the following allows the multiple tasks to process data simultaneously?
a) single buffer
b) double buffer
c) buffer exchange

d) directional buffer
View Answer
Answer: c
Explanation: The buffer exchange allows the multiple tasks to process simultaneously without having to have control structures to supervise access and it is also used to simplify the control code.
2. Which buffering mechanism is common to the SPOX operating system?
a) buffer exchange
b) single buffer
c) linear buffer
d) directional buffer
View Answer
Answer: a
Explanation: The buffer exchange can support the SPOX operating system which is used for the digital signal processors and it is easy to implement.
3. Which buffers exchange the empty buffers for full ones?
a) single buffer
b) buffer exchange
c) directional buffer
d) double buffer
View Answer
Answer: b
Explanation: The buffer exchange can be used for exchanging the empty buffers with the full ones. It will have more than two buffers.
4. Which process takes place when the buffer is empty?
a) read
b) write
c) read and write
d) memory access
View Answer

Answer: a
Explanation: The buffer exchange will contain the data in case of the writing process but the buffer will be emptied in the case of the read cycle.
5. Which process takes place when the buffer contains data?
a) read
b) read and write
c) acknowledge
d) write
View Answer
Answer: d
Explanation: The buffer will be emptied in the case of the readin process and it will contain the data in case of the writing process.
6. Which of the following does not need to have a semaphore?
a) double buffer
b) single buffer
c) buffer exchange
d) directional buffer
View Answer
Answer: c
Explanation: There are many advantages over the buffer exchange. One such is that it will not have a semaphore to control any shared memory or buffers.
7. Which buffer can assimilate a large amount of data before processing?
a) single buffer
b) double buffer
c) multiple buffers
d) directional buffer
View Answer
Answer: c
Explanation: The requesting task can use multiple buffers which can assimilate large amounts of data before processing. This can be considered one of the advantages of the buffer exchange.

8. Which can reduce the latency?
a) partial filling
b) complete filling
c) no filling
d) multiple buffers
View Answer
Answer: a
Explanation: The latency is introduced because of the size of the buffer. The partial filling of data can be used to reduce the latency but it requires some additional control signal.
9. Which of the following can indicate when the buffer is full or ready for collection?
a) intra-task communication
b) inter-task communication
c) memory task communication
d) peripheral task communication
View Answer
Answer: b
Explanation: The level of the inter-task communication can indicate the buffer status, that is whether it is full or ready for collection.
10. What solution can be done for the inefficiency in the memory usage of small data?
a) same size buffer
b) single buffer
c) variable size buffer
d) directional buffer
View Answer
Answer: c
Explanation: The buffer exchange becomes inefficient while concerning the memory usage for small and the simple data. In order to solve this problem, variable size buffers can be used but this requires a more complex operation to handle the length of the valid data.
11. Which processor has a different segment buffer?
a) 8051

b) 8086
c) ARM
d) MC68HC11
View Answer
Answer: b
Explanation: The 8086 has a segmented architecture where the buffers are having a different segment. In such processors, the device drive is running in the supervisor mode, requesting task in the user mode and so on.
12. Which of the following can combine buffers in a regular and methodical way using pointers?
a) buffer exchange
b) directional buffer
c) linked lists
d) double buffer
View Answer
Answer: c
Explanation: The linked lists are the way of combining buffers in a methodical way and regular method by using the pointers to point the next entry in the list. This can be maintained by adding an entry to the which contains the address of the next buffer.
13. Which entry will have a special value in the linked list?
a) first entry
b) last entry
c) second entry
d) second last entry
View Answer
Answer: b
Explanation: The last entry will have a special value that indicates that the entry is the last one but the first entry uses the pointer entry to locate the position.
14. Which entry can use the pointer in the linked list?
a) first entry
b) last entry
c) second entry

d) third entry
View Answer
Answer: a

1. How a buffer memory allocate its memory through the linker?
a) statically
b) dynamically
c) linearly
d) non-linearly
View Answer
Answer: a
Explanation: The buffer memory can be allocated mainly in two ways, statically and dynamically. Statically, the memory is allocated through the linker and dynamically it can allocate memory during runtime by calling an operating system.
2. How did a buffer memory allocate in the runtime?
a) linearly
b) non-linearly
c) statically
d) dynamically
View Answer
Answer: d
Explanation: The buffer memory allocation is done in two ways, statically and dynamically. Dynamically, it can allocate memory during runtime by calling an operating system.
3. Which allocation requires the memory to be defined before building the application?
a) dynamic allocation
b) static allocation
c) linear allocation
d) straight allocation
View Answer

Answer: b
Explanation: The static allocation requires the memory to be defined before building the application and allocates the memory through the special directives at the assembler level.
4. What factor depends on the allocation of buffer memory?
a) nature
b) size
c) variable type and definition
d) variable size and type
View Answer
Answer: c
Explanation: The amount of allocated buffer memory depends on the variable type and the definition, the strings and the character arrays are the most commonly used types.
5. Which are the system calls which are used by the UNIX operating system?
a) malloc()
b) unmalloc()
c) malloc() and unmalloc()
d) proc() and return
View Answer
Answer: c
Explanation: The malloc() and the unmalloc() are the system calls which is used by the UNIX operating system which allocates the memory dynamically and returns it.
6. Which is the counterpart of the malloc()?
a) unmalloc()
b) proc()
c) struc()
d) return()
View Answer
Answer: a
Explanation: The malloc() and unmalloc() are the system calls in which the unmalloc() is the counterpart of the malloc().

7. How is the UNIX operating system allocates its memory?
a) statically
b) linearly
c) non linearly
d) dynamically
View Answer
Answer: d
Explanation: The malloc() and the unmalloc() are the system calls which is used by the UNIX operating system which allocates the memory dynamically and returns it.
8. Which term is used to describe a bug within the memory system?
a) memory leakage
b) buffer memory
c) system call
d) register leakage
View Answer
Answer: a
Explanation: The memory leakage is used to describe the bug within the memory system.
9. What are the common errors that are seen in memory leakage?
a) memory size
b) memory type
c) stack frame error
d) stack register
View Answer
Answer: c
Explanation: The stack frame errors are the common errors which are seen in the memory leakage and it is caused by the stack overflowing of its allocated memory space and the system call function failure.
10. How the stack frame errors are caused?
a) stack overflow
b) underrun
c) overrun

d) timing
View Answer
Answer: a
Explanation: There are certain common errors called the stack frame errors which are responsible for the memory leakage and it is due to the stack overflowing of its allocated memory space and the system call function failure.
11. Which of the following clean up the stack?
a) interrupt handler
b) processor
c) exception handler
d) memory handler
View Answer
Answer: c
Explanation: The exception handler cleans up the stack memory before returning to the previous executing software thread or the generic handler.
12. Which of the following stores the context of the exception?
a) stack
b) register
c) ROM
d) RAM
View Answer
Answer: a
Explanation: The exception handler is the one which clean up the stack memory before returning to the previous executing software thread and the ROM stores the context of exception in the stack automatically or as a part of the exception routine.
13. Which of the following contains the return information of the stack?
a) table
b) vector
c) frame
d) block

Answer: c

1. Which of the following allows the reuse of the software and the hardware components?
a) platform based design
b) memory design
c) peripheral design
d) input design
View Answer
Answer: a
Explanation: The platform design allows the reuse of the software and the hardware components in order to cope with the increasing complexity in the design of embedded systems.
2. Which of the following is the design in which both the hardware and software are considered during the design?
a) platform based design
b) memory based design
c) software/hardware codesign
d) peripheral design
View Answer
Answer: c
Explanation: The software/hardware codesign is the one which having both hardware and software design concerns. This will help in the right combination of the hardware and the software for the efficient product.
3. What does API stand for?
a) address programming interface
b) application programming interface
c) accessing peripheral through interface
d) address programming interface
View Answer
Answer: b
Explanation: The platform-based design helps in the reuse of both the hardware and the software components. The application programming interface helps in extending the platform towards software applications.
4. Which activity is concerned with identifying the task at the final embedded systems?
a) high-level transformation

b) compilation
c) scheduling
d) task-level concurrency management
View Answer
Answer: d
Explanation: There are many design activities associated with the platforms in the embedded system and one such is the task-level concurrency management which helps in identifying the task that needed to be present in the final embedded systems.
5. In which design activity, the loops are interchangeable?
a) compilation
b) scheduling
c) high-level transformation
d) hardware/software partitioning
View Answer
Answer: c
Explanation: The high-level transformation is responsible for the high optimizing transformations, that is, the loops can be interchanged so that the accesses to array components become more local.
6. Which design activity helps in the transformation of the floating point arithmetic to fixed point arithmetic?
a) high-level transformation
b) scheduling
c) compilation
d) task-level concurrency management
View Answer
Answer: a
Explanation: The high-level transformation are responsible for the high optimizing transformations, that is, for the loop interchanging and the transformation of the floating point arithmetic to the fixed point arithmetic can be done by the high-level transformation.
7. Which design activity is in charge of mapping operations to hardware?
a) scheduling
b) high-level transformation
c) hardware/software partitioning

d) compilation
View Answer
Answer: c
Explanation: The hardware/software partitioning is the activity which is in charge of mapping operations to the software or to the hardware.
8. Which of the following is approximated during hardware/software partitioning, during task-level concurrency management?
a) scheduling
b) compilation
c) task-level concurrency management
d) high-level transformation
View Answer
Answer: a
Explanation: The scheduling is performed in several contexts. It should be approximated with the other design activities like the compilation, hardware/software partitioning, and task-level concurrency management. The scheduling should be precise for the final code.
9. Which of the following is a process of analyzing the set of possible designs?
a) design space exploration
b) scheduling
c) compilation
d) hardware/software partitioning
View Answer
Answer: a
Explanation: The design space exploration is the process of analyzing the set of designs and the design which meet the specification is selected.
10. Which of the following is a meet-in-the-middle approach?
a) peripheral based design
b) platform based design
c) memory based design

d) processor design
View Answer
Answer: b

1. What does FRIDGE stand for?
a) fixed-point programming design environment
b) floating-point programming design environment
c) fixed-point programming decoding
d) floating-point programming decoding
View Answer
Answer: a
Explanation: Certain tools are available which are developed for the optimization programmes and one such tool is the FRIDGE or fixed-point programming design environment, commercially made by Synopsys System Studio.
2. Which of the following tool can replace the floating point arithmetic to fixed point arithmetic?
a) SDS
b) FAT
c) VFAT
d) FRIDGE
View Answer
Answer: d
Explanation: There are certain tools available which are developed for the optimization programmes and one such tool is the FRIDGE or fixed-point programming design environment, commercially made available by Synopsys System Studio. This tool can is used in the transformation program, that is the conversion of floating point arithmetic to the fixed point arithmetic. This is widely used in signal processing.
3. Which programming algorithm is used in the starting process of the FRIDGE?
a) C++
b) JAVA
c) C

d) BASIC
View Answer
Answer: c
Explanation: The FRIDGE tool uses C programming algorithm in the initial stage and is converted to a fixed-C algorithm which extends C by two extends.
4. In which loop transformation, a single loop is split into two?
a) loop tiling
b) loop fusion
c) loop permutation
d) loop unrolling
View Answer
Answer: b
Explanation: Many loop transformation are done for the optimization of the program and one such loop transformation is the loop fusion in which a single loop is split and the loop fission includes the merging of the two separate loops.
5. Which loop transformations have several instances of the loop body?
a) loop fusion
b) loop unrolling
c) loop fission
d) loop tiling
View Answer
Answer: b
Explanation: The loop unrolling is a standard transformation which creates several instances of the loop body and the number of copies of the loop is known as the unrolling factor.
6. The number of copies of a loop is called as
a) rolling factor
b) loop factor
c) unrolling factor
d) loop size
View Answer

Answer: c
Explanation: The number of copies of the loop is known as the unrolling factor and it is a standard transformation that produces instances of the loop body.
7. Which of the following can reduce the loop overhead and thus increase the speed?
a) loop unrolling
b) loop tiling
c) loop permutation
d) loop fusion
View Answer
Answer: a
Explanation: The loop unrolling can reduce the loop overhead, that is the fewer branches per execution of the loop body, which in turn increases the speed but is only restricted to loops with a constant number of iteration. The unrolling can increase the code size.
8. Which loop transformation can increase the code size?
a) loop permutation
b) loop fusion
c) loop fission
d) loop unrolling
View Answer
Answer: d
Explanation: The loop unrolling can decrease the loop overhead, the fewer branches per execution of the loop body and this can increase the speed but is only restricted to loops with a constant number of iteration and thus the loop unrolling can increase the code size.
9. Which memories are faster in nature?
a) RAM
b) ROM
c) Scratch pad memories
d) EEPROM
View Answer

Answer: c
Explanation: As the memory size decreases, it is faster in operation, that is the smaller memories are faster than the larger memories. The small memories are caches and the scratch pad memories.
10. Which loop transformation reduces the energy consumption of the memory systems?
a) loop permutation
b) loop tiling
c) loop fission
d) loop fusion
View Answer
Answer: b

1. What does COOL stand for?
a) coprocessor tool
b) codesign tool
c) code tool
d) code control
View Answer
Answer: b
Explanation: The COOL is the codesign tool which is one of the optimisation technique for partitioning the software and the hardware.
2. How many inputs part does COOL have?
a) 2
b) 4
c) 5
d) 3
View Answer
Answer: d
Explanation: The codesign tool consists of three input parts. These are target technology, design constraints and the behaviour and each input follows different functions. The target technology comprises the information about the different hardware

platform components available within the system, design constraints are the second part of the input which contains the design constraints, and the behaviour part is the third input which describes the required overall behaviour.

3. Which part of the COOL input comprises information about the available hardware platform components?

a) target technology
b) design constraints
c) both behaviour and design constraints
d) behaviour

View Answer

Answer: a

Explanation: The codesign tool consists of three input parts which are described as target technology, design constraints and the behavior. Each input does different functions. The target technology comprises information about the different hardware platform components available within the system.

4. What does the second part of the COOL input comprise?

a) behaviour and target technology
b) design constraints
c) behaviour
d) target technology

View Answer

Answer: b

Explanation: The second part of the COOL input comprises of the design constraints such as the latency, maximum memory size, required throughput or maximum area for application-specific hardware.

5. What does the third part of the COOL input comprise?

a) design constraints and target technology
b) design constraints
c) behaviour
d) target technology

View Answer

Answer: c

Explanation: The codesign tool consists of three input parts and the third part of the COOL input describes the overall behaviour of the system. The hierarchical task graphs are used for this.

6. How many edges does the COOL use?
a) 1
b) 2
c) 3
d) 4
View Answer
Answer: b
Explanation: The codesign tool has 2 edges. These are timing edges and the communication edges. The timing edge provides the timing constraints whereas the communication edge contains the information about the amount of information to be exchanged.
7. Which edge provides the timing constraints?
a) timing edge
b) communication edge
c) timing edge and communication edge
d) special edge
View Answer
Answer: a
Explanation: The codesign tool has 2 edges. They are timing edges and the communication edges. The timing edge provides the timing constraints.
8. Which edge of the COOL contains information about the amount of information to be exchanged?
a) regular edge
b) timing edge
c) communication edge
d) special edge
View Answer
Answer: c
Explanation: The codesign tool has 2 edges and these are timing edges and the communication edges. The communication edge contains information about the amount of information to be exchanged.
9. What does Index set KH denotes?
a) processor

b) hardware components
c) task graph nodes
d) task graph node type
View Answer
Answer: b
Explanation: There is a certain index set which is used in the IP or the integer programming model. The KH denotes the hardware component types.
10. What does Index set L denotes?
a) processor
b) task graph node
c) task graph node type
d) hardware components
View Answer
Answer: c

1. Which of the following helps in reducing the energy consumption of the embedded system?
a) compilers
b) simulator
c) debugger
d) emulator
View Answer
Answer: a
Explanation: The compilers can reduce the energy consumption of the embedded system and the compilers performing the energy optimizations are available.
2. Which of the following help to meet and prove real-time constraints?
a) simulator
b) debugger
c) emulator

d) compiler
View Answer
Answer: d
Explanation: There are several reasons for designing the optimization and compilers and one such is that it could help to meet and prove the real-time constraints.
3. Which of the following is an important ingredient of all power optimization?
a) energy model
b) power model
c) watt model
d) power compiler
View Answer
Answer: b
Explanation: Saving energy can be done at any stage of the embedded system development. The high-level optimization techniques can reduce power consumption and similarly compiler optimization also can reduce the power consumption and the most important thing in power optimization are the power model.
4. Who proposed the first power model?
a) Jacome
b) Russell
c) Tiwari
d) Russell and Jacome
View Answer
Answer: c
Explanation: Tiwari proposed the first power model in the year 1974. The model includes the so-called bases and the inter-instruction instructions. Base costs of the instruction correspond to the energy consumed per instruction execution when an infinite sequence of that instruction is executed. Inter instruction costs model the additional energy consumed by the processor if instructions change.
5. Who proposed the third power model?
a) Tiwari
b) Russell
c) Jacome

d) Russell and Jacome
View Answer
Answer: d
Explanation: The third model was proposed by Russell and Jacome in the year 1998.
6. Which compiler is based on the precise measurements of two fixed configurations?
a) first power model
b) second power model
c) third power model
d) fourth power model
View Answer
Answer: c
Explanation: The third model was proposed by Russell and Jacome in the year 1998 and is based on the precise measurements of the two fixed configurations.
7. What does SPM stand for?
a) scratch pad memories
b) sensor parity machine
c) scratch pad machine
d) sensor parity memories
View Answer
Answer: a
Explanation: The smaller memories provide faster access and consume less energy per access and SPM or scratch pad memories is a kind of small memory which access fastly and consume less energy per access and it can be exploited by the compiler.
8. Which model is based on precise measurements using real hardware?
a) encc energy-aware compiler
b) first power model
c) third power model
d) second power model
View Answer

Answer: a
Explanation: The encc-energy aware compiler uses the energy model by Steinke et al. it is based on the precise measurements of the real hardware. The power consumption of the memory, as well as the processor, is included in this model.
9. What is the solution to the knapsack problem?
a) many-to-many mapping
b) one-to-many mapping
c) many-to-one mapping
d) one-to-one mapping
View Answer
Answer: d
Explanation: The knapsack problem is associated with the size constraints, that is the size of the scratch pad memories. This problem can be solved by one-to-one mapping which was presented in an integer programming model by Steinke et al.
10. How can one compute the power consumption of the cache?
a) Lee power model
b) First power model
c) Third power model
d) CACTI
View Answer
Answer: d

1. Which of the following function can interpret data in the C language?
a) printf
b) scanf
c) proc
d) file
View Answer
Answer: b
Explanation: The scanf and printf are the well-known functions in the C language which is used to interpret data and print data respectively.

2. What is the first stage of the compilation process?
a) pre-processing
b) post-processing
c) compilation
d) linking
View Answer
Answer: a
Explanation: The pre-processing involves the first stage of the compilation process in which the include files are added. This file defines the standard functions, constants etc and the output is fed to the compiler.
3. Which of the following produces an assembler file in the compilation process?
a) pre-processor
b) assembler
c) compiler
d) post-processing
View Answer
Answer: c
Explanation: The output of the pre-processor is given to the compiler in which it produces an assembler file from the instruction codes of the processor.
4. Which file is converted to an object file?
a) hex file
b) decoded file
c) coded file
d) assembly file
View Answer
Answer: d
Explanation: The output of the pre-processor is given to the compiler which produces an assembler file from the instruction codes of the processor and this possesses libraries. The assembly file is then converted into the object file and this contains the hexadecimal coding.
5. Which of the following contains the hexadecimal coding?
a) object file

b) assembly file
c) coded file
d) decoded file
View Answer
Answer: a
Explanation: The output of the pre-processor is given to the compiler which produces an assembler file from the instruction codes of the processor and this possesses libraries and then these assembly file is converted into the object file and this possesses the coding of hexadecimal.
6. Which of the following processes the source code before it goes to the compiler?
a) compiler
b) simulator
c) pre-processor
d) emulator
View Answer
Answer: c
Explanation: The pre-processor is responsible for processing the source code before it goes to the compiler and this in turn allows the programmer to define variable types, constants, and much other information.
7. Which of the following allows the programmer to define constants?
a) pre-processor
b) compiler
c) emulator
d) debugger
View Answer
Answer: a
Explanation: The pre-processor processes the source code before it goes to the compiler and this allows the programmer to define variable types, constants, and much other information.
8. Which statement replaces all occurrences of the identifier with string?
a) # define identifier string
b) # include
c) # define MACRO()

d) # ifdef
View Answer
Answer: a
Explanation: # define statement can replace all occurrences of the identifier with string. Similarly, it is able to define the constants, which also make the code easier to understand.
9. Which of the following has the include file?
a) emulator
b) debugger
c) pre-processor
d) simulator
View Answer
Answer: c
Explanation: The pre-processor produces the source code before it goes to the compiler and this allows the programmer to define variable types, constants, and much other information. This pre-processor also has to include files and combines them into the program source.
10. Which statement is used to condense the code to improve the eligibility?
a) # define MACRO()
b) # include
c) if
d) else-if
View Answer
Answer: a

1. Which of the following are header files?
a) #include
b) file
c) struct()
d) proc()
View Answer

Answer: a
Explanation: The #include is a header file which defines the standard constants, variable types, and many other functions. This can also include some standard libraries.
2. Which is the standard C compiler used for the UNIX systems?
a) simulator
b) compiler
c) cc
d) sc
View Answer
Answer: c
Explanation: The cc is the standard C compiler used in the UNIX system. Its command lines can be pre-processed, compiled, assembled and linked to create an executable file.
3. Which compiling option is used to compile programs to form part of a library?
a) -c
b) -p
c) -f
d) -g
View Answer
Answer: a
Explanation: There are several options for the compilers. The option -c compiles the linking stage and then leaves the object file. This option is used to compile programs to form a part of the library.
4. Which compiling option can be used for finding which part of the program is consuming most of the processing time?
a) -f
b) -g
c) -p
d) -c
View Answer
Answer: c
Explanation: The -p instructs the compiler to produce codes which count the number of times each routine is called and this is useful for finding the processing time of the programs.

5. Which compiling option can generate symbolic debug information for debuggers?
a) -c
b) -p
c) -f
d) -g
View Answer
Answer: d
Explanation: The -g generates the symbolic debug information for the debuggers. Without this, the debugger cannot print the variable values, it can only work at the assembler level. The symbolic information is passed through the compilation process and stored in the executable file.
6. Which of the following is also known as loader?
a) locater
b) linker
c) assembler
d) compiler
View Answer
Answer: b
Explanation: The linker is also known as a loader. It can take the object file and searches the library files to find the routine it calls.
7. Which of the following gives the final control to the programmer?
a) linker
b) compiler
c) locater
d) simulator
View Answer
Answer: a
Explanation: The linker can give the final control to the programmer concerning how unresolved references are reconciled, where the sections are located in the memory, which routines are used, and so on.
8. Which command takes the object file and searches library files to find the routine calls?
a) simulator

b) emulator
c) debugger
d) linker
View Answer
Answer: d
Explanation: The linker is also known as a loader. It can take the object file and searches the library files to find the routine it calls. The linker can give the final control to the programmer concerning how unresolved references are reconciled, where the sections are located in the memory, which routines are used, and so on.
9. Which assembler option is used to turn off long or short address optimization?
a) -n
b) -V
c) -m
d) -o
View Answer
Answer: a
Explanation: The option -o puts the assembler into the file obj file, -V can write the assembler's version number on the standard error output, -m runs the macro preprocessor on the source file and -n turns off the long or short address optimization.
10. Which assembler option runs the m4 macro preprocessor on the source file?
a) -n
b) -m
c) -V
d) -o
View Answer
Answer: b

1. Which of the following language can describe the hardware?
a) C
b) C++
c) JAVA

d) VHDL
View Answer
Answer: d
Explanation: The VHDL is the hardware description language which describes the hardware whereas the C, C++ and JAVA are software languages.
2. What do VHDL stand for?
a) Verilog hardware description language
b) VHSIC hardware description language
c) very hardware description language
d) VMEbus description language
View Answer
Answer: b
Explanation: VHDL is the VHSIC(very high speed integrated circuit) hardware description language which was developed by three companies, IBM, Intermetrics and Texas Instruments and the first version of the VHDL is established in the year 1984 and later on the VHDL is standardised by the IEEE.
3. What does VHSIC stand for?
a) very high speed integrated chip
b) very high sensor integrated chip
c) Verilog system integrated chip
d) Verilog speed integrated chip
View Answer
Answer: a
Explanation: The VHSIC stands for very high speed integrated chip and VHDL was designed in the context of the VHSIC, developed by the department of defence in the US.
4. Each unit to be modelled in a VHDL design is known as
a) behavioural model
b) design architecture
c) design entity

d) structural model
View Answer
Answer: c
Explanation: Each unit to be modelled in a VHDL design is known as the design entity or the VHDL entity. There are two types of ingredients are used. These are the entity declaration and the architecture declaration.
5. Which of the following are capable of displaying output signal waveforms resulting from stimuli applied to the inputs?
a) VHDL simulator
b) VHDL emulator
c) VHDL debugger
d) VHDL locater
View Answer
Answer: a
Explanation: The VHDL simulator is capable of displaying the output signal waveforms which results from the stimuli or trigger applied to the input.
6. Which of the following describes the connections between the entity port and the local component?
a) port map
b) one-to-one map
c) many-to-one map
d) one-to-many maps
View Answer
Answer: a
Explanation: The port map describes the connection between the entity port and the local component. The component is declared by component declaration and the entity ports are mapped with the port mapping.
7. Who proposed the CSA theory?
a) Russell
b) Jacome
c) Hayes
d) Ritchie
View Answer

Answer: c
Explanation: The CSA theory is proposed by Hayes and this theory is based on the systematic way of building up value sets.
8. Which of the following is a systematic way of building up value sets?
a) CSA theory
b) Bayes theorem
c) Russell's power mode;
d) first power model
View Answer
Answer: a
Explanation: The CSA theory is proposed by Hayes. The theory is based on the systematic way of building up value sets, that is the electronics design system uses a variety of value sets, like 2, 3 etc. The goal of developing discrete value sets is to avoid the problems of solving network equations.
9. Which of the following is an abstraction of the signal impedance?
a) level
b) strength
c) size
d) nature
View Answer
Answer: b
Explanation: The systems contain electrical signals of different strengths and it needs to compute the strength and the logic level resulting from a connection of two or more sources of electrical signals. The strength is the abstraction of the signal impedance.
10. Which of the following is an abstraction of the signal voltage?
a) level
b) strength
c) nature
d) size
View Answer
Answer: a

1. How many kinds of wait statements are available in the VHDL design?
a) 3
b) 4
c) 5
d) 6
View Answer
Answer: b
Explanation: There are four kinds of wait statements. These are wait on, wait for, wait until and wait.
2. Which wait statement does follow a condition?
a) wait for
b) wait until
c) wait
d) wait on
View Answer
Answer: b
Explanation: The wait until follows a condition. The condition may be an arithmetic or logical one and the wait for statement follows time duration, it might be in microseconds or nanoseconds or any other time unit. Similarly, the wait on statement follows a signal list and the wait statement suspends indefinitely.
3. Which wait statement does follow duration?
a) wait for
b) wait
c) wait until
d) wait on
View Answer
Answer: a
Explanation: The wait for statement follows time duration, it might be in microseconds or nanoseconds or any other time unit.
4. Which of the following is a C++ class library?
a) C++
b) C
c) JAVA

d) SystemC
View Answer
Answer: d
Explanation: System C is a C++ class library which helps in solving the behavioural, resolution, simulation time problems.
5. Which model of SystemC uses floating point numbers to denote time?
a) SystemC 1.0
b) SystemC 2.0
c) SystemC 3.0
d) SystemC 4.0
View Answer
Answer: a
Explanation: The SystemC includes several models of the time units. SystemC 1.0 uses floating point numbers which denote time.
6. Which model of SystemC uses the integer number to define time?
a) SystemC 1.0
b) SystemC 2.0
c) SystemC 3.0
d) SystemC 4.0
View Answer
Answer: b
Explanation: The SystemC includes several models of the time. System 2.0 is an integer model to define time and this model also supports physical units such as microseconds, nanoseconds, picoseconds etc.
7. Which model of the SystemC helps in the communication purpose?
a) SystemC 2.0
b) SystemC 3.0
c) SystemC 1.0
d) SystemC 4.0
View Answer

Answer: a
Explanation: The SystemC 2.0 provides the channel port and interface ports for the communication purpose.
8. Which C++ class is similar to the hardware description language like VHDL?
a) SystemC
b) Verilog
c) C
d) JAVA
View Answer
Answer: a
Explanation: The SystemC is a C++ class which is similar to the hardware description languages like VHDL and Verilog. The execution and simulation time in the SystemC is almost similar to the VHDL.
9. What does ESL stand for?
a) EEPROM system level
b) Electronic-system level
c) Electrical system level
d) Electron system level
View Answer
Answer: b
Explanation: The ESL is electronic-system level and the SystemC is associated with the ESL and TLM. The SystemC is also applied to the architectural exploration, performance modelling, software development and so on.
10. What to TLM stand for?
a) transfer level modelling
b) triode level modelling
c) transaction level modelling
d) transistor level modelling
View Answer
Answer: c

1. Which of the following is standardised as IEEE 1364?
a) C
b) C++
c) FORTRAN
d) Verilog
View Answer
Answer: d
Explanation: The Verilog is a hardware description language which was developed for modelling hardware and electronic devices. This was later standardised by IEEE standard 1364.
2. Who developed the Verilog?
a) Moorby
b) Thomas
c) Russell and Ritchie
d) Moorby and Thomson
View Answer
Answer: d
Explanation: The Verilog is a hardware description language which was developed by Moorby and Thomson in 1991 and it was standardised as IEEE standard 1364. The Verilog is modelled for the electronics devices.
3. Which versions of the Verilog is known as System Verilog?
a) Verilog version 3.0
b) Verilog version 1.0
c) Verilog version 1.5
d) Verilog version 4.0
View Answer
Answer: a
Explanation: The Verilog versions 3.0 and 3.1 is called as the System Verilog. These include several extensions to the Verilog version 2.0.
4. Which of the following is a Verilog version 1.0?
a) IEEE standard 1394-1995
b) IEEE standard 1364-1995

c) IEEE standard 1394-2001
d) IEEE standard 1364-2001
View Answer
Answer: b
Explanation: The IEEE standard 1364-1995 is the first version of the Verilog and IEEE standard 1394-2001 is the Verilog version 2.0.
5. Which of the following provides multiple-valued logic with eight signal strength?
a) Verilog
b) VHDL
c) C
d) C++
View Answer
Answer: a
Explanation: The Verilog supports the multiple-valued logic with eight different signal strength but Verilog is less flexible compared to the VHDL, that is, it allows the hardware entities to be instantiated in loops which help to build up a structural description.
6. Which of the following is a superset of Verilog?
a) Verilog
b) VHDL
c) System Verilog
d) System VHDL
View Answer
Answer: c
Explanation: The System Verilog is a superset of the Verilog. But later on, System Verilog and Verilog has merged into a new IEEE standard 1800-2009.
7. Which hardware description language is more flexible?
a) VHDL
b) Verilog
c) C

d) C++
View Answer
Answer: a
Explanation: The Verilog is less flexible compared to the VHDL, that is, it allows the hardware entities to be instantiated in loops which help to build up a structural description. But Verilog, on the other hand, focuses more on the built-in features.
8. Which of the following provide more features for transistor-level descriptions?
a) C++
b) C
c) VHDL
d) Verilog
View Answer
Answer: d
Explanation: The Verilog offers more features than the VHDL but VHDL is more flexible compared to the Verilog. The Verilog can provide transistor-level descriptions but the VHDL cannot provide this description.
9. Which hardware description language is popular in the US?
a) System Verilog
b) System log
c) Verilog
d) VHDL
View Answer
Answer: c
Explanation: Verilog and VHDL are almost similar in their characteristics and have a similar number of users. The VHDL is more popular in Europe whereas Verilog is more popular in the US.
10. Which hardware description language is more popular in Europe?
a) VHDL
b) System log
c) Verilog
d) C
View Answer

Answer: a

1. Which of the following is an analogue extension of the VHDL?
a) VHDL-AMS
b) System VHDL
c) Verilog
d) System Verilog
View Answer
Answer: a
Explanation: The VHDL-AMS is the extension of the VHDL and this includes the analogue and mixed behaviour of the signals.
2. Which of the following support the modelling partial differentiation equation?
a) gate level
b) algorithmic level
c) system level
d) switch level
View Answer
Answer: c
Explanation: There are a variety of levels for designing the embedded systems and each level has its own language. The system level is one such kind which has many peculiarities with respect to the other levels. The system model denotes the entire embedded system and includes the mechanical as well as the information processing aspects. This also supports the modelling of the partial differential equations, which is a key requirement in the modelling.
3. Which level simulates the algorithms that are used within the embedded systems?
a) gate level
b) circuit level
c) switch level
d) algorithmic level
View Answer
Answer: d
Explanation: The algorithmic level simulates the algorithm which is used within in the embedded system.

4. Which level model components like ALU, memories registers, muxes and decoders?
a) switch level
b) register-transfer level
c) gate level
d) circuit level
View Answer
Answer: b
Explanation: The register-transfer level modelling models all the components like the arithmetic and logical unit(ALU), memories, registers, muxes, decoders etc and this modelling is always cycled truly.
5. Which of the following is the most frequently used circuit-level model?
a) SPICE
b) VHDL
c) Verilog
d) System Verilog
View Answer
Answer: a
Explanation: The SPICE is simulation program with integrated circuit emphasis, which is a frequently used circuit-level in the early days. It is used to find the behavior and the integrity of the circuit.
6. Which model includes geometric information?
a) switch-level model
b) layout model
c) gate level model
d) register-transfer level
View Answer
Answer: b
Explanation: The layout reflects the actual circuit model. It includes the geometric information and cannot be simulated directly since it does not provide the information regarding the behavior.
7. Which model cannot simulate directly?
a) circuit level model
b) switch-level model

c) gate level model
d) layout model
View Answer
Answer: d
Explanation: The layout model reflects the actual circuit model and this includes the geometric information and this model cannot be simulated directly because it does not provide the information regarding the behavior.
8. Which of the following models the components like resistors, capacitors etc?
a) register-transfer level
b) layout model
c) circuit level model
d) switch-level model
View Answer
Answer: c
Explanation: The circuit-level model simulation is used for the circuit theory and its components such as the resistors, inductors, capacitors, voltage sources, current sources. This simulation also involves the partial differential equations.
9. Which model uses transistors as their basic components?
a) switch model
b) gate level
c) circuit level
d) layout model
View Answer
Answer: a
Explanation: The switch model can be used in the simulation of the transistors since the transistor is the very basic component in a switch. It is capable of reflecting bidirectional transferring of the information.
10. Which model is used to denote the boolean functions?
a) switch level
b) gate level model
c) circuit level

d) layout model
View Answer
Answer: b
Explanation: The gate level model is used to denote the boolean functions and the simulation only consider the behaviour of the gate.
11. Which model is used for the power estimation?
a) gate-level model
b) layout model
c) circuit model
d) switch model
View Answer
Answer: a
Explanation: The gate level model is used to denote the boolean functions and the simulation only consider the behaviour of the gate. This model is also useful in the power estimation since it provides accurate information about the signal transition probabilities.
12. In which model, the effect of instruction is simulated and their timing is not considered?
a) gate-level model
b) circuit model
c) coarse-grained model
d) layout model
View Answer
Answer: c
Explanation: The coarse-grained model is a kind of the instruction set level modelling in which only the effect of instruction is simulated and the timing is not considered. The information which is provided in the manual is sufficient for this type of modelling.
13. Which models communicate between the components?
a) transaction level modelling
b) fine-grained modelling
c) coarse-grained modelling

d) circuit level model
View Answer
Answer: a
Explanation: The transaction level modelling is a type of instruction set level model. This modelling helps in the modelling of components which is used for the communication purpose. It also models the transaction, such as read and writes cycles.
14. Which of the following has a cycle-true set of simulation?
a) switch-level model
b) layout model
c) circuit-level
d) fine-grained model
View Answer
Answer: d

1. Which of the following is a set of specially selected input patterns?
a) test pattern
b) debugger pattern
c) bit pattern
d) byte pattern
View Answer
Answer: a
Explanation: While testing any devices or embedded systems, we apply some selected inputs which is known as the test pattern and observe the output. This output is compared with the expected output. The test patterns are normally applied to the already manufactured systems.
2. Which is applied to a manufactured system?
a) bit pattern
b) parity pattern
c) test pattern
d) byte pattern
View Answer

Answer: c
Explanation: For testing any devices or embedded systems, we use some sort of selected inputs which is known as the test pattern and observe the output and is compared with the expected output. These test patterns are normally applied to the manufactured systems.
3. Which of the following is based on fault models?
a) alpha-numeric pattern
b) test pattern
c) bit pattern
d) parity pattern
View Answer
Answer: b
Explanation: The test pattern generation is normally based on the fault models and this model is also known as the stuck-at model. The test pattern is based on a certain assumption, that is why it is called the stuck-at model.
4. Which is also called stuck-at model?
a) byte pattern
b) parity pattern
c) bit pattern
d) test pattern
View Answer
Answer: d
Explanation: The test pattern generation is basically based on the fault models and this type of model is also known as the stuck-at model. These test patterns are based on a certain assumption, hence it is known as the stuck-at model.
5. How is the quality of the test pattern evaluated?
a) fault coverage
b) test pattern
c) size of the test pattern
d) number of errors
View Answer
Answer: a
Explanation: The quality of the test pattern can be evaluated on the basis of the fault coverage. It is the percentage of potential

faults that can be found for a given test pattern set, that is fault coverage equals the number of detectable faults for a given test pattern set divided by the number of faults possible due to the fault model.
6. What is DfT?
a) discrete Fourier transform
b) discrete for transaction
c) design for testability
d) design Fourier transform
View Answer
Answer: c
Explanation: The design of testability or DfT is the process of designing for the better testability.
7. Which of the following is also known as boundary scan?
a) test pattern
b) JTAG
c) FSM
d) CRC
View Answer
Answer: b
Explanation: The JTAG is a technique for connecting scan chains of several chips and is also known as boundary scan.
8. What does BILBO stand for?
a) built-in logic block observer
b) bounded input bounded output
c) built-in loading block observer
d) built-in local block observer
View Answer
Answer: a
Explanation: The BILBO or the built-in logic block observer is proposed as a circuit combining, test response compaction, test pattern generation, and serial input/output capabilities.
9. What is CRC?
a) code reducing check
b) counter reducing check

c) counting redundancy check
d) cyclic redundancy check
View Answer
Answer: d
Explanation: The CRC or the cyclic redundancy check is the error detecting code which is commonly used in the storage device and the digital networks.
10. What is FSM?
a) Fourier state machine
b) finite state machine
c) fast state machine
d) free state machine
View Answer
Answer: b
Explanation: The FSM is the finite state machine. It will be having a finite number of states and is used to design both the sequential logic circuit and the computer programs. It can be used for testing the scan design in the testing techniques.
11. Which of the following have flip-flops which are connected to form shift registers?
a) scan design
b) test pattern
c) bit pattern
d) CRC
View Answer
Answer: a

1. Which is a top-down method of analyzing risks?
a) FTA
b) FMEA
c) Hazards

d) Damages
View Answer
Answer: a
Explanation: The FTA is Fault tree analysis which is a top-down method of analyzing risks. It starts with damage and comes up with the reasons for the damage. The analysis is done graphically by using gates.
2. What is FTA?
a) free tree analysis
b) fault tree analysis
c) fault top analysis
d) free top analysis
View Answer
Answer: b
Explanation: The FTA is also known as the Fault tree analysis which is a top-down method of analyzing risks. The analysis starts with damage and comes up with the reasons for the damage. The analysis can be checked graphically by using gates.
3. Which gate is used in the geometrical representation, if a single event causes hazards?
a) AND
b) NOT
c) NAND
d) OR
View Answer
Answer: d
Explanation: The fault tree analysis is done graphically by using gates mainly AND gates and OR gates. The OR gate is used to represent the single event which is hazardous. Similarly, AND gates are used in the graphical representation if several events cause hazards.
4. Which analysis uses the graphical representation of hazards?
a) Power model
b) FTA
c) FMEA

d) First power model
View Answer
Answer: b
Explanation: The FTA is done graphically by using gates mainly AND gates and OR gates. The OR gate is used to represent the single event which is hazardous.
5. Which gate is used in the graphical representation, if several events cause hazard?
a) OR
b) NOT
c) AND
d) NAND
View Answer
Answer: c
Explanation: The fault tree analysis is done graphically by using gates. The main gates used are AND gates and OR gates. The AND gates are used in the graphical representation if several events cause hazards.
6. What is FMEA?
a) fast mode and effect analysis
b) front mode and effect analysis
c) false mode and effect analysis
d) failure mode and effect analysis
View Answer
Answer: d
Explanation: The FMEA is the failure mode and the effect analysis, in which the analysis starts at the components and tries to estimate their reliability.
7. Which of the following can compute the exact number of clock cycles required to run an application?
a) layout model
b) coarse-grained model
c) fine-grained model
d) register-transaction model
View Answer

Answer: c
Explanation: The fine-grained model has the cycle-true instruction set simulation. In this modelling, it is possible to compute the exact number of clock cycles which is required to run an application.
8. Which model is capable of reflecting the bidirectional transfer of information?
a) switch-level model
b) gate level
c) layout model
d) circuit-level model
View Answer
Answer: a

1. What is meant by FOL?
a) free order logic
b) fast order logic
c) false order logic
d) first order logic
View Answer
Answer: d
Explanation: Many formal verification techniques are used and these are classified on the basis of the logics employed. The techniques are propositional logic, first order logic, and higher order logic. The FOL is the abbreviated form of the first order logic which includes the quantification.
2. What is HOL?
a) higher order logic
b) higher order last
c) highly organised logic
d) higher order less
View Answer
Answer: a
Explanation: The formal verification techniques are classified on the basis of the logics employed. The techniques are

propositional logic, first order logic, and higher order logic. The HOL is the abbreviation of the higher order logic in which the proofs are automated and manually done with some proof support.

3. What is BDD?

a) boolean decision diagram
b) binary decision diagrams
c) binary decision device
d) binary device diagram

View Answer

Answer: b

Explanation: The binary decision diagram is a kind of data structure which is used to represent the Boolean function.

4. Which formal verification technique consists of a Boolean formula?

a) HOL
b) FOL
c) Propositional logic
d) Both HOL and FOL

View Answer

Answer: c

Explanation: The propositional logic technique is having the boolean formulas and the boolean function. The tools used in propositional logic is the tautology checker or the equivalence checker which in turn uses the binary decision diagrams which are also known as BDD.

5. Which of the following is also known as equivalence checker?

a) BDD
b) FOL
c) Tautology checker
d) HOL

View Answer

Answer: c

Explanation: The propositional logic technique consists of the boolean formulas and the boolean function. The tools used in this type of logic is the tautology checker or the equivalence checker which in turn uses the BDD or the binary decision diagrams.

6. Which of the following is possible to locate errors in the specification of the future bus protocol?
a) EMC
b) HOL
c) BDD
d) FOL
View Answer
Answer: c
Explanation: The model checking was developed using the binary decision diagram and the BDD and it was possible to locate errors in the specification of the future bus protocol.
7. Which of the following is a popular system for model checking?
a) HOL
b) FOL
c) BDD
d) EMC
View Answer
Answer: d
Explanation: The EMC-system is developed by Clark and it describes the CTL formulas, which is the computational tree logics.
8. What is CTL?
a) computational tree logic
b) code tree logic
c) cpu tree logic
d) computer tree logic
View Answer
Answer: a