24225

3 Hours / 70 Marks   Seat No. ☐☐☐☐☐☐☐☐

Instructions :   (1)   All Questions are *compulsory.*

(2)   Illustrate your answers with neat sketches wherever necessary.

(3)   Figures to the right indicate full marks.

(4)   Assume suitable data, if necessary.

Marks

1.   **Attempt any FIVE of the following :**   **10**

(a)   Define term (1) Skew (2) Metastability

(b)   Give the syntax for construct "when".

(c)   State any two types of VHDL modeling.

(d)   Write two applications of test bench.

(e)   Define Mealy machine & write its equation.

(f)   Define sensitivity list. Where it is used ?

(g)   Draw CMOS inverter & label it.

2.   **Attempt any THREE of the following :**   **12**

(a)   Draw the architecture of CPLD and state any two CPLD devices.

(b)   Write VHDL code for D-Flip-flop.

(c)   Justify transmission gates are used instead of MOS switches.

(d)   Explain the process of optimization of arithmetic expressions. Give example.

3. **Attempt any THREE of the following :**   12

     (a)   Draw $Y = \overline{A \cdot B}$ using CMOS logic.

     (b)   Write VHDL code for 3 : 8 decoder.

     (c)   List the different types of logical operator in VHDL.

     (d)   State the advantages & disadvantage of VHDL.

4. **Attempt any THREE of the following :**   12

     (a)   Explain AS/C flow design.

     (b)   Compare BJT & CMOS with any four parameters.

     (c)   Describe simulation cycle in VHDL.

     (d)   Describe any two process used in fabrication of CMOS devices.

     (e)   State the uses of signals & variables in VHDL programming.

5. **Attempt any TWO of the following :**   12

     (a)   Design Moore or Mealy machine for detecting sequence 101.

     (b)   Draw & describe the steps used in twin tub process in CMOS fabrication.

     (c)   Write VHDL code for Half adder using :

         (1)   Structural Model

         (2)   Behavioural Model

6. **Attempt any TWO of the following :**   12

     (a)   Describe HDL design flow for synthesis.

     (b)   (1)   Compare Synchronous & asynchronous logic (any four parameters)

         (2)   Define : (i) Noise Margin (ii) Fanout

     (c)   Write VHDL code for AND, EX-OR logic gate & label the entity, architecture, library in it.

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