17659

21819

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory.*

(2) Answer each next main Question on a new page.

(3) Figures to the right indicate full marks.

Marks

1. Attempt any FIVE : **5 × 4 = 20**

(a) Draw AND gate and NOR gate using NMOS.

(b) Define : (i) Metastability

(ii) Noise Margin

(c) Compare Moore and Mealy machine.

(d) What is VHDL ? Write two advantages of VHDL.

(e) Explain : (i) Sensitivity list.

(ii) Wait statement.

(f) Explain the wafer processing with C-Z method.

(g) Design Mealy sequence detector circuit for detecting sequence of "001".

2. Attempt any FOUR : **4 × 4 = 16**

(a) Compare synchronous & asynchronous sequential circuits.

(b) Draw the architecture of sparatan-3 FPGA series. Explain any two blocks.

(c) Explain : (i) Flattening

(ii) Structuring

(d) Write VHDL program for 3 : 8 decoder.

(e) List and explain data types used in VHDL.

(f) Draw and explain CMOS AND gate.

3. Attempt any FOUR : **16**

(a) List and explain features of CPLD.

(b) State and explain delta delay.

(c) Write VHDL code for Full ADDER.

(d) Explain N-well process with diagram.

(e) Explain Resistance Fabrication.

(f) Design parity checker using Moore logic or Mealy logic.

4. Attempt any FOUR : **4 × 4 = 16**

(a) Compare FPGA and CPLD.

(b) Explain cycle based and event based simulators.

(c) Describe verification using Test Bench.

(d) Write VHDL code for 2 : 1 MUX using if… else statements.

(e) Explain Twin-Tab process in CMOS fabrication with diagram.

(f) Explain HDL design flow for synthesis.

5. Attempt any FOUR : **4 × 4 = 16**

(a) Explain : (i) Sensitivity list

(ii) Zero modeling

(b) Draw the architecture of Xilinx 9500 family CPLD. Explain any two blocks.

(c) What is instantiation in VHDL ? Write one example.

(d) List and explain different types of operators in VHDL.

(e) State and explain efficient coding styles.

(f) Write the VHDL code for 4-bit adder without instantiation.

6. Attempt any FOUR : **4 × 4 = 16**

(a) Explain the following process :

(i) Oxidation process

(ii) Diffusion process

(b) Draw ASIC design flow.

(c) Compare software & hardware description language.

(d) Write VHDL program for 4 : 1 MUX using case statement.

(e) Explain Entity and Architecture with suitable example.

(f) Design the following function using CMOS :

$Y = (A \cdot B) + C$