SUMMER – 2019 EXAMINATION
MODEL ANSWER

Subject: Digital Techniques **Subject Code: 17333**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q.N.	Answer	Marking Scheme
1.	**(A) (i) Ans.**	**Attempt any SIX of the following:** **Define digital system and give its two applications.** **Definition of digital system:** The system which processes or works on the digital signal is known as digital system **Applications:** 1. Flip flops 2. Counters 3. Register 4. Digital calculators 5. Computers	**12** **2M** ***Definition 1M*** ***Any two applications $^{1/2}$M each***
	(ii) Ans.	**State any four Boolean Laws.** **Boolean laws:** A + 1 = 1 A + 0 = A A . 1 = A A . 0 = 0 A + A = A A . A = A	**2M** ***Any four laws ½ M each***

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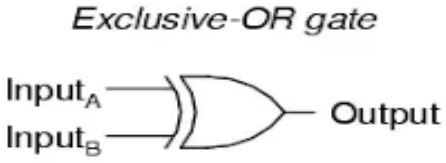
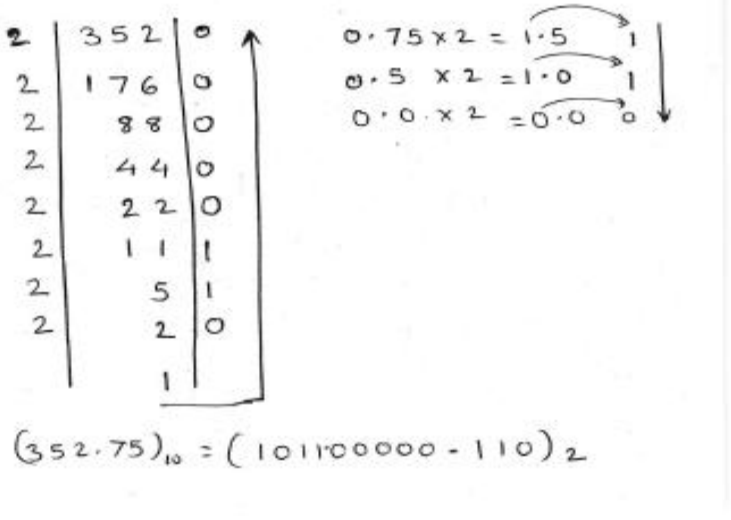
		A+B = B+A A.B = B.A (A + B) + C = A + (B + C) (A B) C = A (B C) A (B + C) = A B + A C A + (B C) = (A + B) (A + C)	
	(iii) Ans.	**Draw logical symbol and truth table of X-OR gate.**  A B Output 0 0 0 0 1 1 1 0 1 1 1 0	**2M** ***Symbol 1M*** ***Truth table 1M***
	(iv) Ans.	**Convert (352.75)10 = (?)2** 	**2M** ***2M***
	(v) Ans.	**List Universal gates. Why they are called as universal gate?**	**2M**

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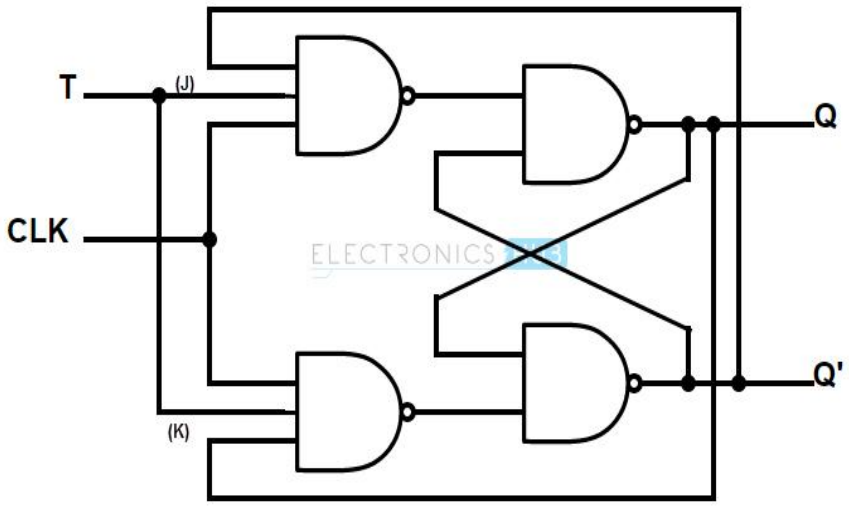
		Universal gates: i) NAND gate ii) NOR gate The NAND and NOR gates are called Universal gates because it is possible to implement any Boolean expression with the help of only NAND or only NOT gates.	***List 1/2M each*** ***Universal gate 1M***
	(vi) Ans.	**Name the IC for digital comparator and ALU.** Digital comparator: IC 7485 ALU: IC 74181	**2M** ***Each 1M***
	(vii) Ans.	**Draw T flip-flop using NAND gate.**  	**2M** ***Diagram 2M***
	(viii) Ans.	**State advantages of digital system.** **Advantages of digital circuits:** 1. Digital Electronic circuits are relatively easy to design. 2. It has higher accuracy, programmability. 3. Transmitted signals are not degraded over long distances. 4. Digital Signals can be stored easily. 5. Digital Electronics is comparatively more immune to "error" and "noise". But in case of high speed designs a small noise can induce error in signal. 6. More Digital Circuits can be fabricated on integrated chips; this helps us obtain complex systems in smaller size.	**2M** ***Any two advantages 1M each***

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1.	**(B)**	**Attempt any TWO of the following:**	**8**
	(i)	**Subtract using 2's complement method:**	**4M**
		(1) $(11101)_2 - (10010)_2$	
		(2) $(1010)_2 - (0110)_2$	
	Ans.	**(1) $(11101)_2 - (10010)_2$**	
		$(10010)_2$ 1's complement = 0 1 1 0 1 + 1 2's complement = 0 1 1 1 0	***2M***
		1 1 1 0 1 + 0 1 1 1 0 Discard → 1 0 1 0 1 1 Carry Final carry is generated, hence answer is positive and in true form.	
		(2) $(1010)_2 - (0110)_2$ $(0110)_2$ 1's complement = 1 0 0 1 + 1 2's complement = 1 0 1 0	***2M***
		1 0 1 0 + 1 0 1 0 1 Discard → 1 0 1 0 0 Carry Final carry is generated, hence answer is positive and in true form.	
	(ii)	**State and prove Demorgan's theorem.**	**4M**
	Ans.	It state that the, complement of a sum is equal to product of its complements	
		$\overline{A+B} = \overline{A}.\overline{B}$ NOR = Bubbled AND	***Theorem 1M each***

A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A}.\overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

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Theorem2: It states that, the complement of a product is equal to sum of the complements.

$\overline{A.B} = \overline{A} + \overline{B}$

NAND = Bubbled OR

A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

Prove 1M each

(iii) **Convert the following:** **4M**

(1) $(1011010110)_2 = (?)_{10}$
(2) $(576)_{10} = (?)_2$
(3) $(237)_8 = (?)_{10}$
(4) $(327.89)_{10} = (?)_{BCD}$

Ans. **(1) $(1011010110)_2 = (?)_{10}$**

$= 1\times2^9 + 0\times2^8 + 1\times2^7 + 1\times2^6 + 0\times2^5 + 1\times2^4 + 0\times2^3 + 1\times2^2 + 1\times2^1 + 0\times2^0$

$= 512 + 0 + 128 + 64 + 0 + 16 + 0 + 4 + 2 + 0$

$= 726$

$(1011010110)_2 = (726)_{10}$

Each 1M

(2) $(576)_{10} = (?)_2$

2	576	0
2	288	0
2	144	0
2	72	0
2	36	0
2	18	0
2	9	1
2	4	0
2	2	0
	1	

$(576)_{10} = (1001000000)_2$

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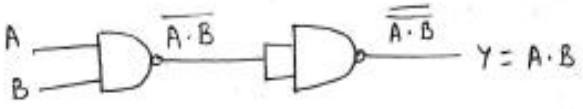
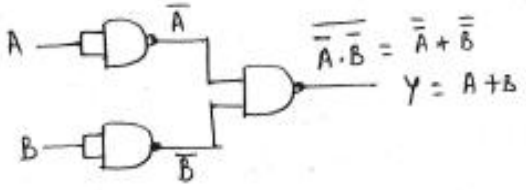
		(3) $(237)_8 = (?)_{10}$ $= 2 \times 8^2 + 3 \times 8^1 + 7 \times 8^0$ $= 2 \times 64 + 3 \times 8 + 7 \times 1$ $= 159$ $(237)_8 = (159)_{10}$ **(4) $(327.89)_{10} = (?)_{BCD}$** 3 2 7 . 8 9 ↓ ↓ ↓ 0011 0010 0111 . 1000 1001 $(327.89)_{10} = (001100100111.10001001)_{BCD}$	
2.	**(a) Ans.**	**Attempt any FOUR of the following:** **Derive AND gate and OR gate using NAND gate only.** AND gate using NAND gate only 2 marks  OR gate using NAND gate only 2 marks.  	**16** **4M** ***AND Gate 2M*** ***OR Gate 2M***

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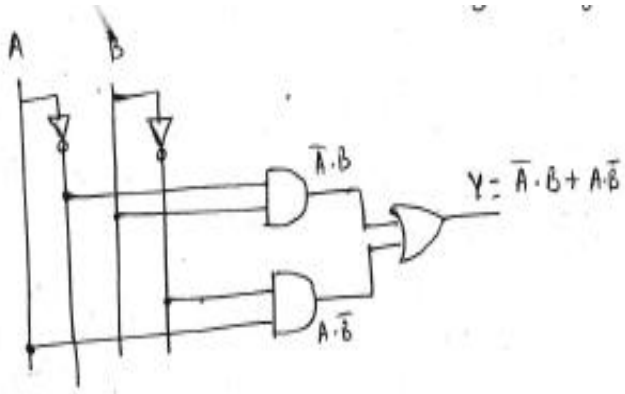
	(b)	**For the following logic expressions given below. $Y = \bar{A} . B + A . \bar{B}$ Do:** **(i) Obtain truth table** **(ii) Name the operation performed from the truth table** **(iii) Realize this operation using basic gates** **(iv) Realize this operation using only NOR gates.**	**4M**
	Ans.	**(i) Obtain truth table:** Truth table A B $\bar{A}$ $\bar{B}$ $\bar{A}.B$ $A\bar{B}$ $\bar{A}.B+A\bar{B}$ 0 0 1 1 0 0 0 0 1 1 0 1 0 1 1 0 0 1 0 1 1 1 1 0 0 0 0 0 **(ii) Name the operation performed from the truth table:** From truth table, the operation performed is EX-OR. **(iii) Realize this operation using basic gates**  **(iv) Realize this operation using only NOR gates.**	***Each sub question 1M***

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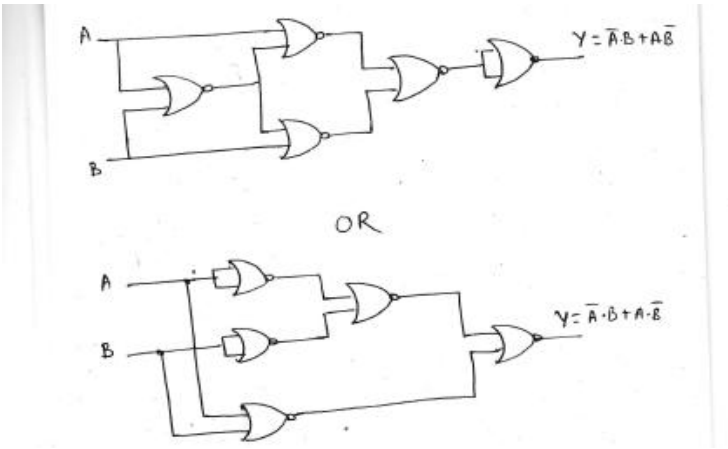


(c) Ans. **Design half subtractor circuit using K-Map.** — **4M**

Half subtractor: Half subtractor is a combinatonal circuit with two inputs and two outputs (difference and borrow)

Truth Table — *Truth table 1M*

Inputs		Outputs	
A	B	Difference A – B	Borrow B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

K-map for difference — *K-map 1M*

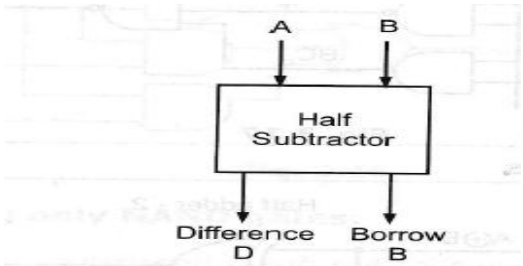
A \ B	$\bar{B}$	B
$\bar{A}$	0	(1)
A	(1)	0

Difference = $\bar{A}B + A\bar{B}$ = $A \oplus B$

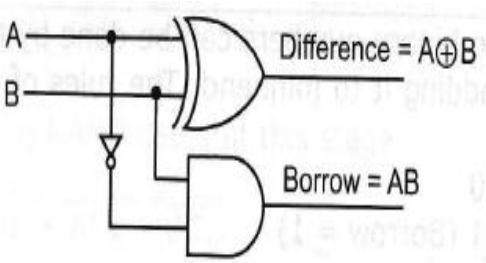
K-map for borrow

A \ B	$\bar{B}$	B
$\bar{A}$	0	(1)
A	0	0

Borrow = $\bar{A}B$ — *Equations 1M*

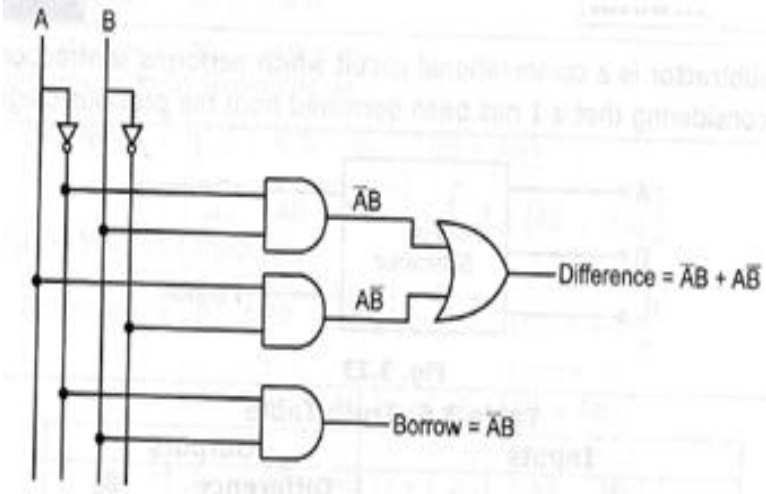


Logic implementation of half subtractor:



Logic implementation of half subtractor 1M

Logic implementation using basic gates:



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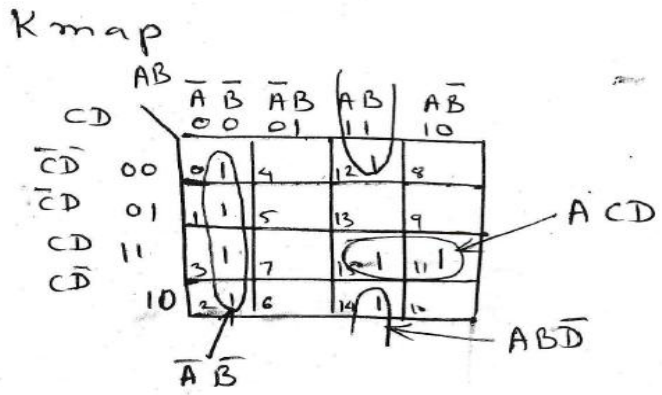
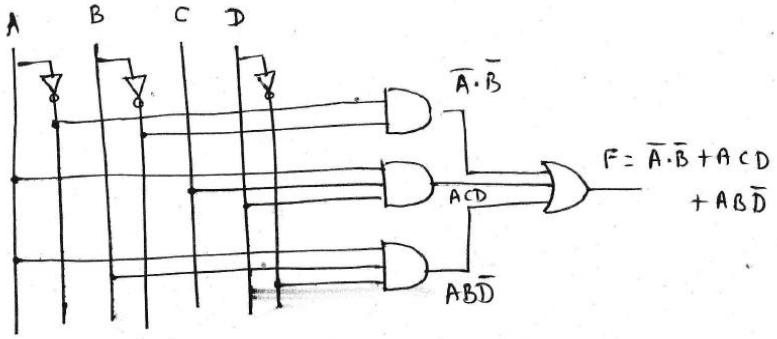
	(d) **Ans.**	**Minimize the following function using K-Maps:** **F = Σ m(0, 1, 2, 3, 11, 12, 14, 15)** **Realise the expression using basic gates.**  $F = \bar{A}\cdot\bar{B} + ACD + AB\bar{D}$  	**4M** ***K map 1M*** ***Grouping 1M*** ***Expression 1M*** ***Realisation 1M***
	(e) **Ans.**	**Draw the block diagram of ALU IC 74181 and explain function of all pins.**	**4M**

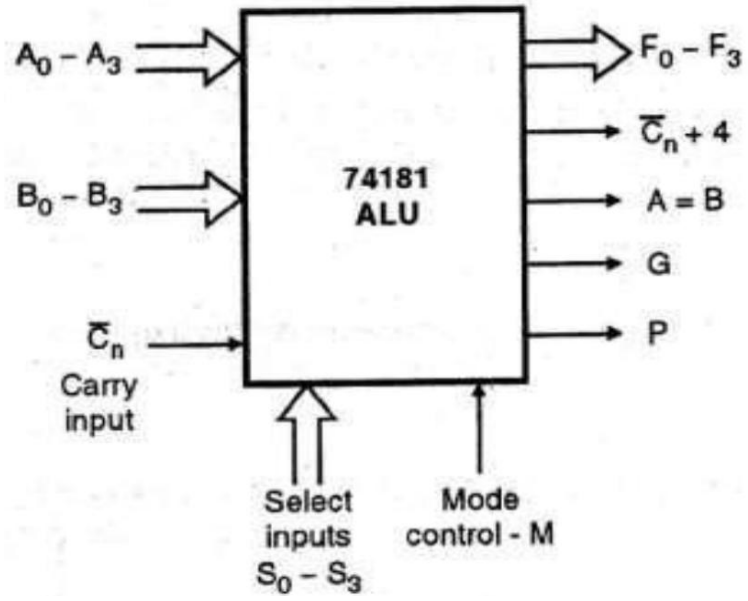


Fig: Block diagram of 74181 ALU

Block diagram 2M

The functions of various input, output and control lines are given below:
A and *B*: 4-bit binary data inputs.
$\bar{C}_n$: Carry input (active-low)
F: 4-bit binary data output.
$\bar{C}_{n+4}$: Carry output (active-low)
For subtraction operation, it indicates the sign of the output. Logic 0 indicates positive result and logic 1 indicates negative result expressed in 2's complement form.
A = *B*: Logic 1 on this line indicates *A* = *B*
G: Carry generate output
P: Carry propagate output
G and *P* outputs are used when a number of 74181 circuits are used in cascade along with 74182 Look-ahead Carry-generator circuit to make the arithmetic operations faster.
Select input (*S*): Used to select any operation
Model Control (*M*): *M* = 0 Arithmetic operations
M = 1 Logic operations

Pin function 2M

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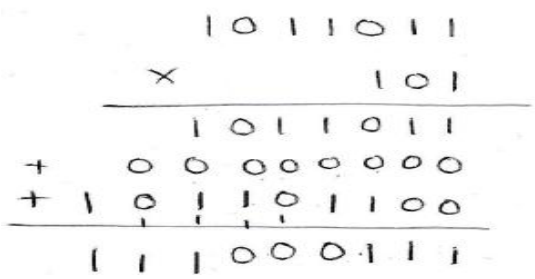
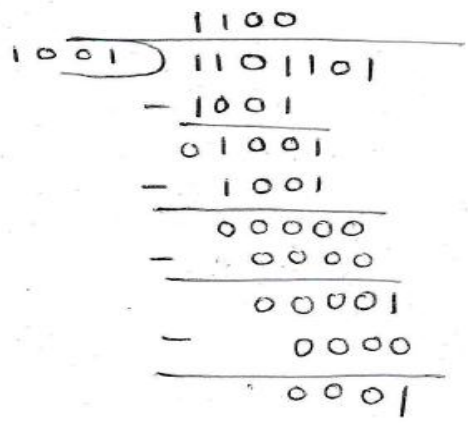
	(f) **Ans.**	**Perform following binary operations:** **(i) 1011011 X 101** **(ii) 1101101 + 1001** **(i) 1011011 X 101**  **(ii) 1101101 + 1001** 	**4M** ***2M*** ***2M***
3.	**(a)** **Ans.**	**Attempt any FOUR of the following:** **Design 1 : 32 demultiplexer using 1 : 4 demultiplexer.**	**16** **4M**

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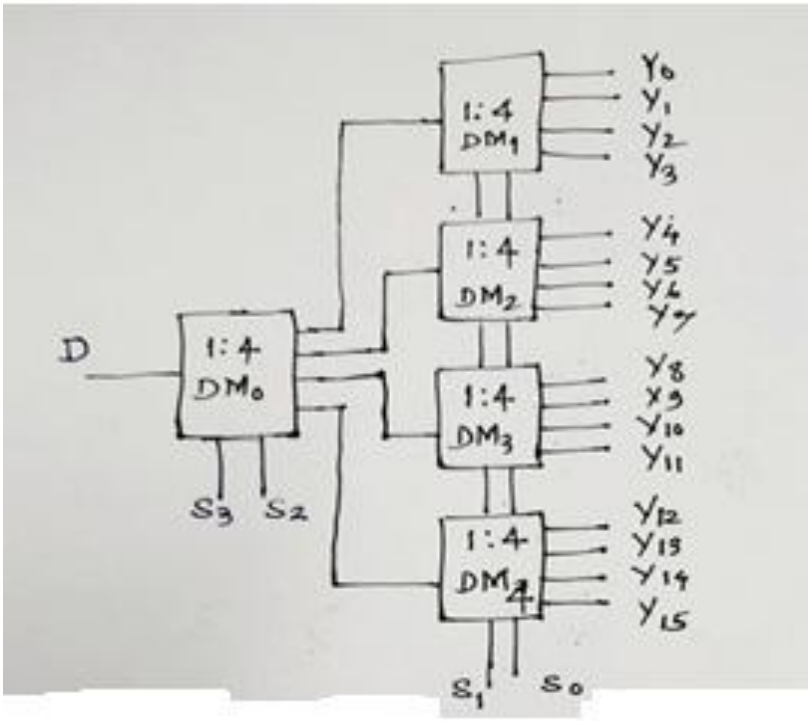
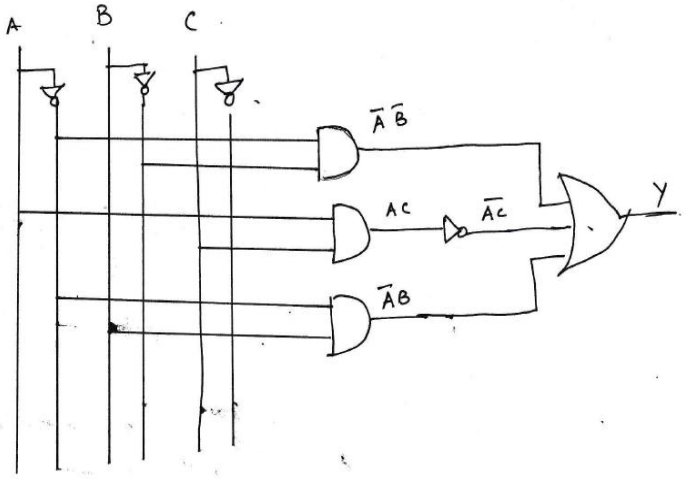
			***Correct diagram 4M***
	(b) **Ans.**	**Implement following logical expression using basic gates. Y = $\bar{A}\bar{B} + \overline{AC} + \bar{A}B$.** 	**4M** ***Correct diagram 4M***

(c) Ans.

Convert F(A, B, C) = Σm(1, 4, 5, 6, 7) in standard POS form. **4M**

The missing term in Standard SO P are 0,2,3

So when converted to Standard POS the form will be

4M for correct conversion

F(A, B, C) = πM(0, 2,3)

(d) Ans.

Differentiate between synchronous and asynchronous counter. **4M**

Sr. No.	Synchronous counter	Asynchronous counter
1	In case of synchronous counter, all the flip-flops are clocked simultaneously.	In case of asynchronous counter, all the flip-flops are not clocked simultaneously.
2	In case of synchronous counter , there is no interconnection between output of one flip-flop and clock of next flip-flop,	In the case of asynchronous counter, the output of first flip-flop drives the clock for second flip-flop, the output of second drives the third and so on.
3	The settling time of synchronous counter is equal to highest settling time of all flip-flops.	The settling time of asynchronous counter is cumulative sum of individual flip-flops.
4	Synchronous counter is known as parallel counter.	Asynchronous counter is known as serial counter
5	Synchronous counter design and implementation becomes tedious and complex as the number of states increases.	Its design and implementation is very simple.
6	Synchronous counter is faster in speed as compare to asynchronous counter.	Asynchronous counter is slow in speed as compare of synchronous counter.

Any four points 1M each

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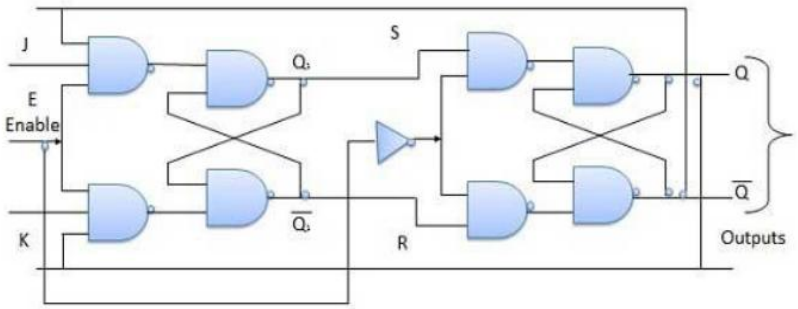
	(e) Ans.	**Explain master slave JK flip-flop with neat diagram.**  **Working of a master slave flip flop –** 1. When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip-flop is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master flip-flop to the slave and output is obtained. 2. Firstly the master flip flop is positive level triggered and the slave flip flop is negative level triggered, so the master responds before the slave. 3. If J=0 and K=1, the high Q' output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slave copies the master. 4. If J=1 and K=0, the high Q output of the master goes to the J input of the slave and the Negative transition of the clock sets the slave, copying the master. 5. If J=1 and K=1, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock. 6. If J=0 and K=0, the flip flop is disabled and Q remains unchanged.	**4M** ***2M for diagram*** ***2M for explaination***
	(f) Ans.	**State any four specifications of DAC.** **1. Resolution:** Resolution is defined as the ratio of change in analog output voltage resulting from a change of 1 LSB at the digital input V_{FS} is defined as the full scale analog output voltage i.e. the analog output voltage when all the digital input with all digits 1.	**4M**

		$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$ **2. Accuracy:** Accuracy indicates how close the analog output voltage is to its theoretical value. It indicates the deviation of actual output from the theoretical value. Accuracy depends on the accuracy of the resistors used in the ladder, and the precision of the reference voltage used. Accuracy is always specified in terms of percentage of the full scale output that means maximum output voltage **3. Linearity:** • The relation between the digital input and analog output should be linear. • However practically it is not so due to the error in the values of resistors used for the resistive networks. **4. Temperature sensitivity:** • The analog output voltage of D to A converter should not change due to changes in temperature. • But practically the output is a function of temperature. It is so because the resistance values and OPAMP parameters change with changes in temperature. **5. Settling time:** • The time required to settle the analog output within the final value, after the change in digital input is called as settling time. • The settling time should be as short as possible. **6. Long term drift** • Long term drift are mainly due to resistor and semiconductor aging and can affect all the characteristics. • Characteristics mainly affected are linearity, speed etc. **7. Supply rejection** • Supply rejection indicates the ability of DAC to maintain scale, linearity and other important characteristics when the supply voltage is varied. • Supply rejection is usually specified as percentage of full scale	***Any four specifications 1M each***

change at or near full scale voltage at 25°C

8. Speed:

- It is defined as the time needed to perform a conversion from digital to analog. It is also defined as the number of conversions that can be performed per second

4. **Attempt any FOUR of the following:** **16**

(a) Ans. **Differentiate between RAM & ROM.** **4M**

Comparison	RAM	ROM
Data	The data is not permanent and it can be altered any number of times.	The data is permanent it can be altered but only a limited number of times that too at slow speed.
Speed	It is high-speed memory.	It is much slower than the RAM
CPU Interaction	The CPU can access the data stored on it.	The CPU cannot access the data stored on it. In order to do so, the data is first copied to the RAM.
Size and capacity	Large size with higher capacity.	Small size with less capacity.
Usage	Primary memory (DRAM DIMM modules), CPU Cache	Firmware like BIOS or UEFI, RFID tags, microcontrollers, medical devices, and at places where a small and permanent memory solution.

Any four points 1M each

(b) Ans. **Draw circuit diagram of R-2R type D to A convertor. Describe its working.** **4M**

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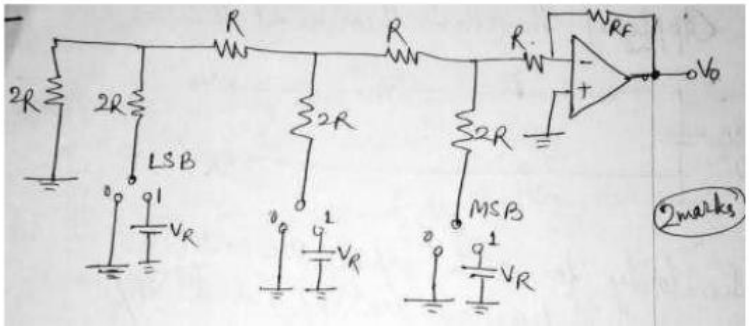
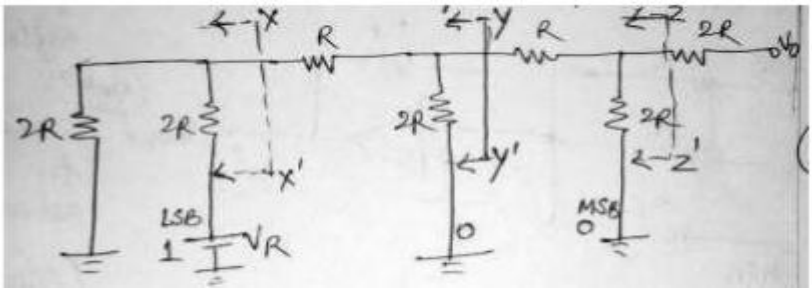


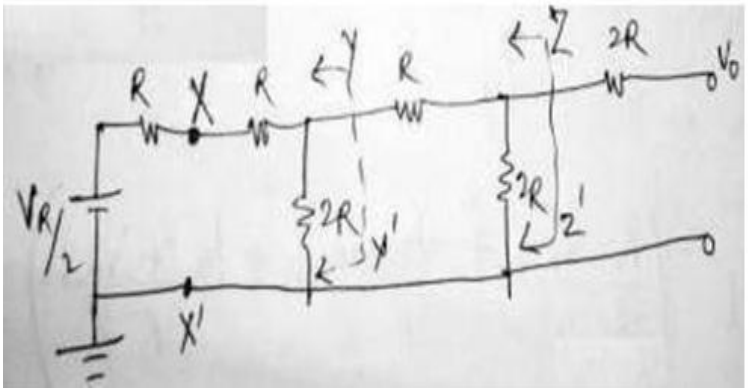
For example if the digital input is 001

3M for diagram

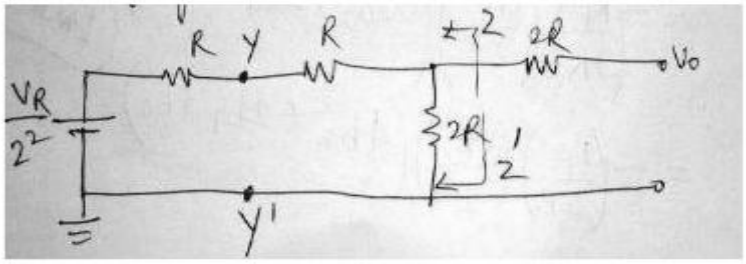


Applying Theremins theorem at XX

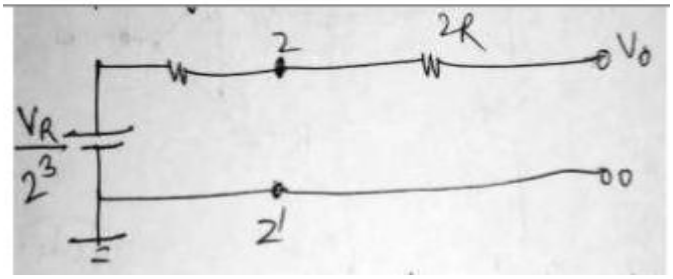
1M for final equation



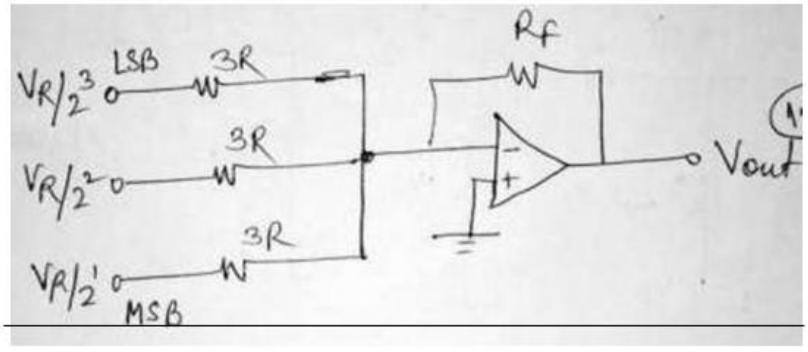
Applying Thevenins theorem at YY



Applying Thevenins theorem at YY



Similarly for digital input 010 and 100 the equivalent voltages are $VR/2^2$ and $V\ R/2^1$ respectively. The equivalent resistance is 3Rin each case. So the simplified
Circuitof3bit R-2R ladder DAC is

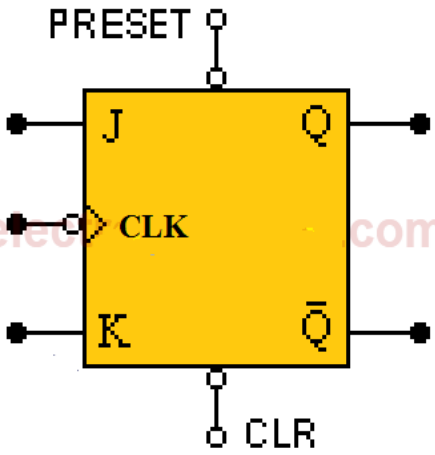


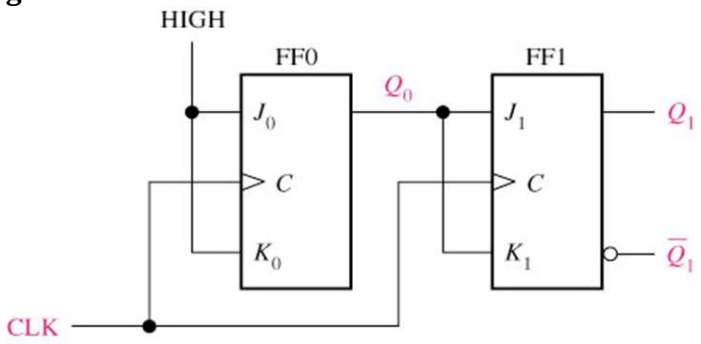
The analog output voltage for a given digital input is given by

$V_{out} = -((R_F/3R)\ V_R \times b_0/2^3 + R_F/3R\ V_R \times b_1/2^2 + R_F/3R\ V_R \times b_2/2^1)$

$= -(R_F/3R)(V_R/2^3)(2^2b_2 + 2^1b_1 + 2^0b_0)$

$= -(R_F/3R)(V_R/2^3)(4b_2 + 2b_1 + b_0)$

	(c) **Ans.**	**Describe the function of present and clear terminals in JK flip-flop. Write truth table of it.** **The PRESET and CLEAR inputs of a JK Flip-Flop** There are two very important additional inputs in the JK Flip-Flop. • The PRESET input used to directly put a "1" in the Q output on the JK Flip-Flop. • The CLEAR input used to directly put a "0" in the Q output on the JK Flip-Flop.  The PRESET and CLEAR inputs of the JK Flip-Flop are asynchronous, which means that they will have an immediate effect on the Q and Q' outputs regardless of the state of the clock and / or the J and K inputs. The Flip-Flop may or may not have a small bubble in the PRESET or CLEAR inputs which indicate that they are active low. **JK Flip Flop Truth Table**	**4M** ***2M for function of preset and clear***

		<table><tr><th></th><th colspan="5">Input</th><th colspan="2">Output</th></tr><tr><th></th><th>Preset</th><th>Clear</th><th>CLK</th><th>J</th><th>K</th><th>Q</th><th>$\overline{Q}$</th></tr><tr><td>Invalid</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>1*</td><td>1*</td></tr><tr><td>Preset</td><td>0</td><td>1</td><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td></tr><tr><td>Clear</td><td>1</td><td>0</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td></tr></table> In order for the J and K inputs and the clock to be functional, the CLEAR and PRESET inputs must be at a "High" logic level	***2M for truth table***
	(d) **Ans.**	**Explain 2-bit synchronous counter with truth table and timing diagram.**  **Synchronous Up Counter:** In the circuit diagram, the basic Synchronous counter design is shown which is Synchronous up counter. A 2 -bit Synchronous up counter start to count from 0 (00 in binary) and increment or count upwards to 03 (11 in binary) and then start new counting cycle by getting reset. The external clock is directly provided to all J-K Flip-flops at the same time in a parallel way. If we see the circuit, the first flip-flop, FF0 which is the least significant bit in this 2-bit synchronous counter, is connected to a Logic 1 external input via J and K pin. Due to this connection, HIGH logic across the Logic 1 signal, change the state of first flip-flop on every clock pulse. Next stage, the second flip-flop FF1, input pin of J and K is connected across the output of the first Flip-flop. The truth table is as shown	**4M** ***1M for diagram*** ***1M for explaination***

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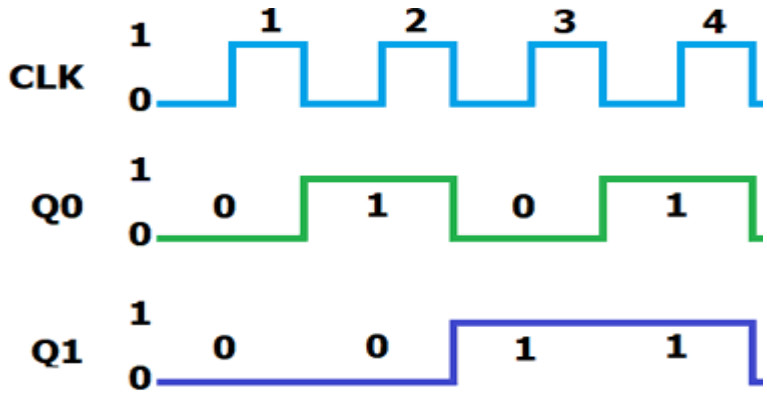
		<table><tr><th>Clock</th><th>Q1</th><th>Q0</th><th>Decimal Count</th></tr><tr><td>1st</td><td>0</td><td>0</td><td>0</td></tr><tr><td>2nd</td><td>0</td><td>1</td><td>1</td></tr><tr><td>3rd</td><td>1</td><td>0</td><td>2</td></tr><tr><td>4th</td><td>1</td><td>1</td><td>3</td></tr></table> The timing diagram is as given below 	***1M for truth table*** ***1M for timing diagram***
	(e) **Ans.**	**Draw block diagram of PISO shift register and describe its operations.** As name suggests the input data will enter in parallel that means at a time to all flip flop. And output will get serially. We now can develop an idea for the parallel entry of data into the register. Here the data bits are entered into the flip flops simultaneously, rather than a bit-by-bit basis. Let take an example suppose we have to save a 4-bit number (1011). Then all input are feed the inputs of different 4 number of flip flop. With single clock pulse all data are enter to all 4 flip flops. In bellow see the block diagram of 4 bit of parallel in serial out shift register.	**4M** ***Description 2M***

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		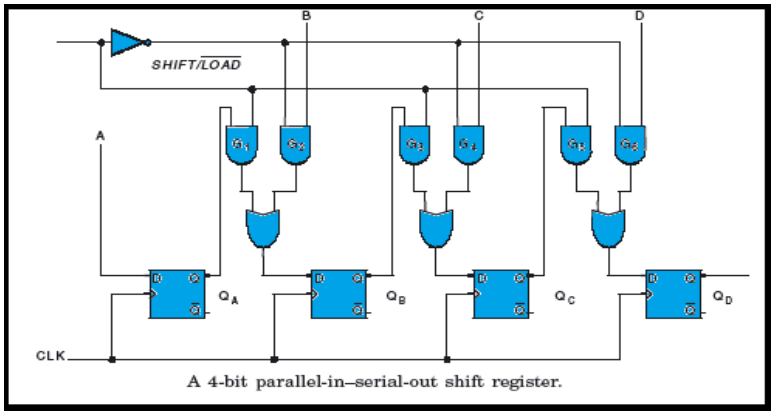 A 4-bit parallel-in–serial-out shift register. Now from above 4 bit parallel in serial out shift register we can see, A, B, C, and D are the four parallel data input lines and *SHIFT* / *LOAD* (*SH* / *LD*) is a control input that allows the four bits of data at A, B, C, and D inputs to enter into the register in parallel or shift the data in serial. When *SHIFT* / *LOAD* is HIGH, AND gates G1, G3, and G5 are enabled, allowing the data bits to shift right from one stage to the next. When *SHIFT* / *LOAD* is LOW, AND gates G2, G4, and G6 are enabled, allowing the data bits at the parallel inputs. When a clock pulse is applied, the flip-flops with D = 1 will be set and the flip-flops with D = 0 will be reset, thereby storing all the four bits simultaneously. The OR gates allow either the normal shifting operation or the parallel data-entry operation, depending on which of the AND gates are enabled by the level on the *SHIFT* / *LOAD* input.	***2M for diagram***
	(f) **Ans.**	**Reduce following expression using K-map and implement it using NOR gates:** **$Y = \pi M(1, 3, 5, 7, 8, 10, 14)$**	**4M**

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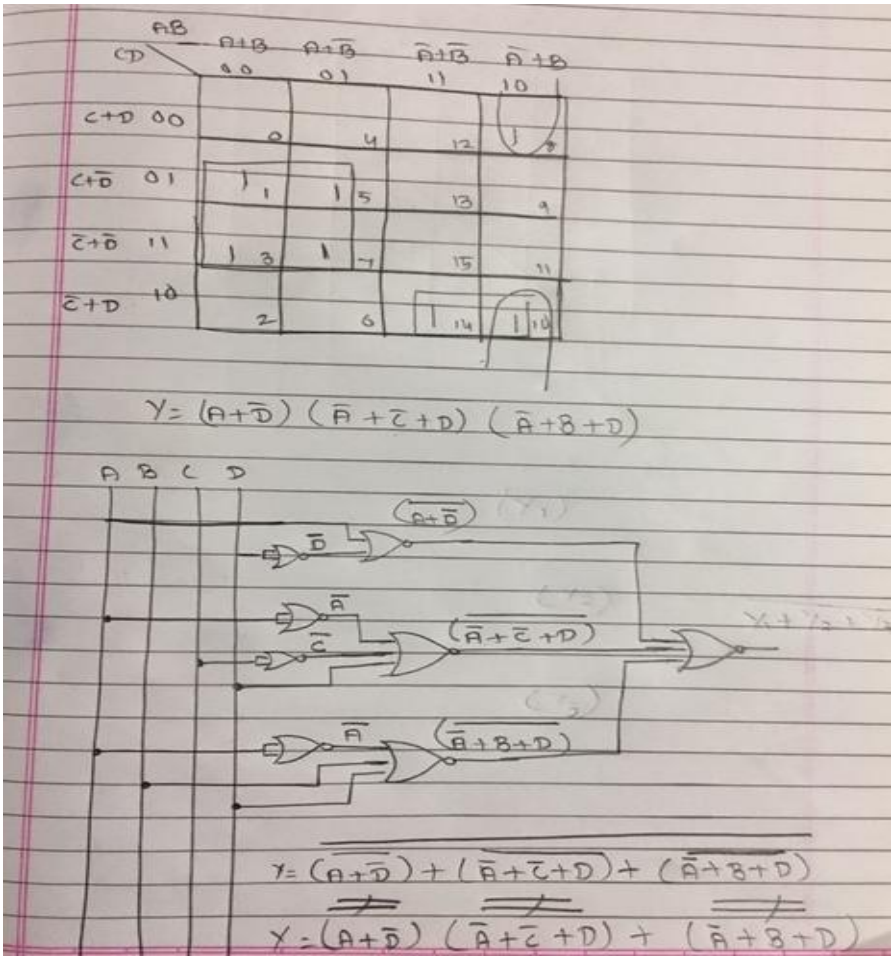
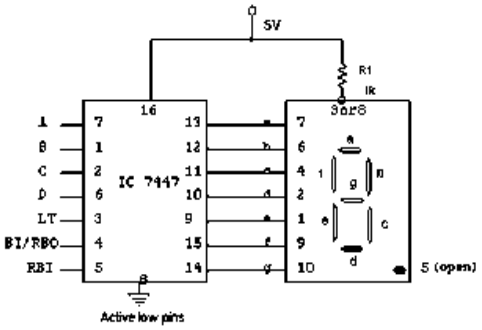
			***1M for k map*** ***1M for Logical expression*** ***2M for the logic diagram using NOR gate***
5.	**(a) Ans.**	**Attempt any FOUR of the following:** **State different applications of flip-flops.** **Applications of flip-flops:** 1. Bounce elimination switch, 2. Latch, 3. Registers, 4. Counters, 5. Memory.	**16** **4M** ***Any four application 1M each***
	(b) Ans.	**Draw block diagram of BCD to seven segment decoder using IC 7447 with its truth table.**	**4M**



TRUTH TABLE:

BCD Inputs				Output Logic Levels from IC 7447 to 7-segments							Decimal number display
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	1	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	1	1	0	0	9

Block diagram 2M

Truth table 2M

(c) Ans. **Compare weighted resistor DAC & R-2R DAC.** **4M**

Sr. No.	Parameters	Weighted Resistor DAC	R-2R Ladder DAC
1	Simplicity	Simple	Slightly complicated
2	Range of resistor values	Wide range is required	Resistors of only two values
3	Number of resistors per bit	One	Two
4	Ease of expansion	Not easy to expand for more number of bits	Easy to expand

1M for each point

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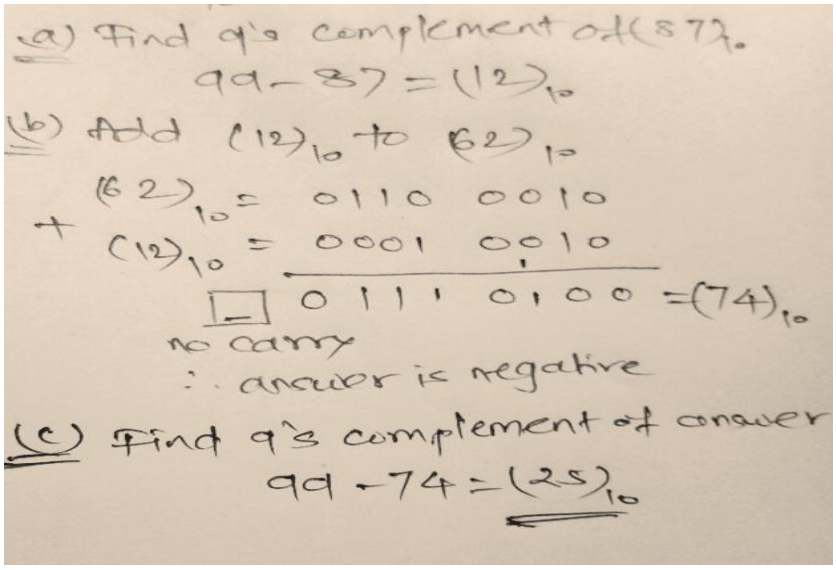
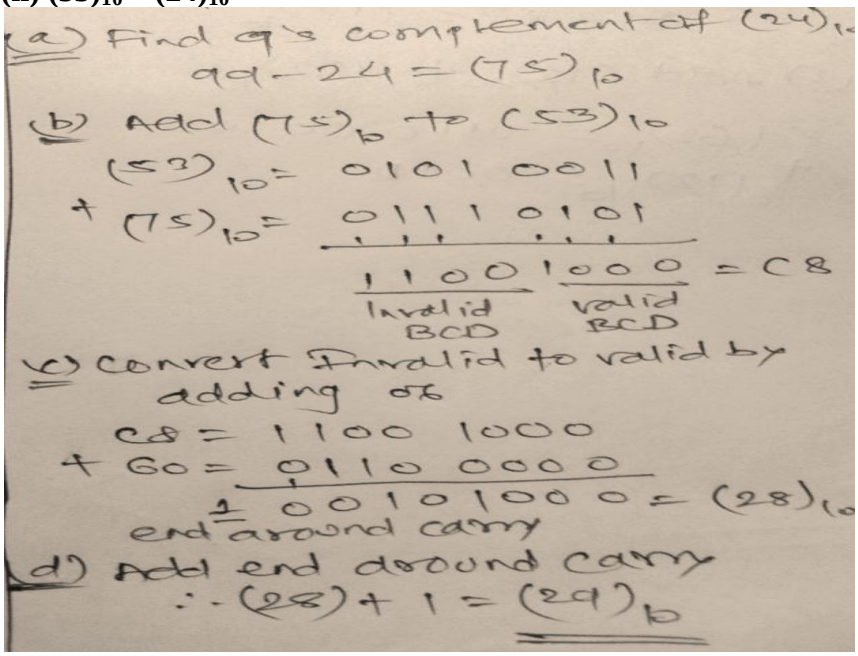
	(d)	**Perform the following using 9's complement:** **(i) $(62)_{10} - (87)_{10}$** **(ii) $(53)_{10} - (24)_{10}$**	**4M**
	Ans.	**(i) $(62)_{10} - (87)_{10}$**  (a) Find 9's complement of $(87)_{10}$ $99 - 87 = (12)_{10}$ (b) Add $(12)_{10}$ to $(62)_{10}$ $(62)_{10} = 0110\ 0010$ $+ (12)_{10} = 0001\ 0010$ $0111\ 0100 = (74)_{10}$ no carry ∴ answer is negative (c) Find 9's complement of answer $99 - 74 = (25)_{10}$ **(ii) $(53)_{10} - (24)_{10}$**  (a) Find 9's complement of $(24)_{10}$ $99 - 24 = (75)_{10}$ (b) Add $(75)_b$ to $(53)_{10}$ $(53)_{10} = 0101\ 0011$ $+ (75)_{10} = 0111\ 0101$ $1100\ 1000 = C8$ Invalid BCD, valid BCD (c) Convert invalid to valid by adding 06 $C8 = 1100\ 1000$ $+ 60 = 0110\ 0000$ $1\ 0010\ 1000 = (28)_{10}$ end around carry (d) Add end around carry ∴ $(28) + 1 = (29)_b$	***Each 2M***

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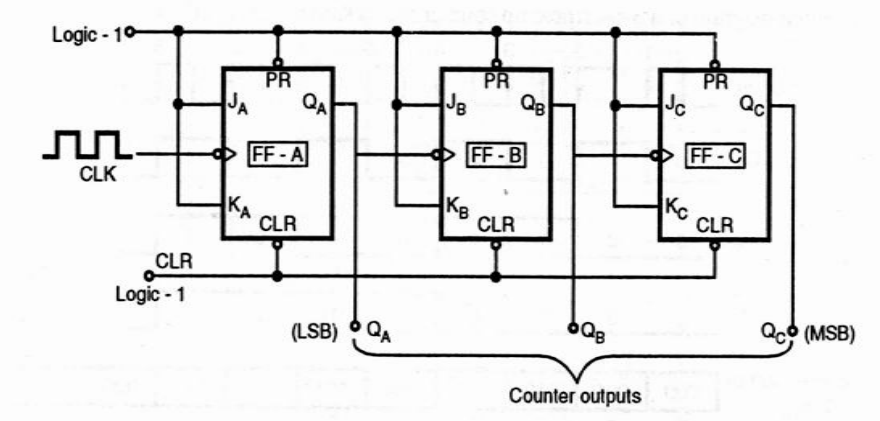
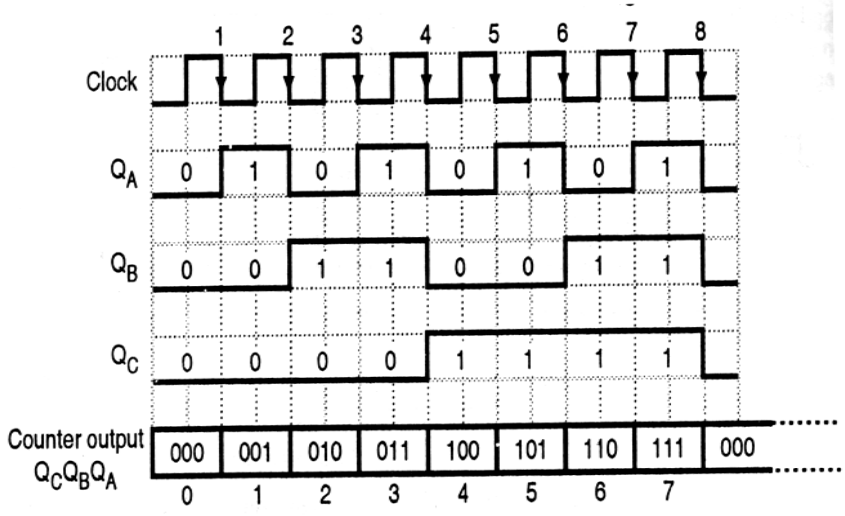
	(e)	**Design 3-bit asynchronous up counter and describe its operations.**	**4M**
	Ans.	The number of states in 3-bit counter is 8 that require 3 flip-flops and QA, QB and QC are the output of the flip-flops. The output QA of the least significant F/F changes for every clock pulse. This can achieved by using the T-type F/F with TA=1. The output QB makes a transition from 0-1 or 1-0 whenever QA changes from 1 to 0. Therefore if QA is connected to the clock input of next T-type F/F FF1 with TB=1, QB goes from 1-0. Similarly QC makes a transition whenever QB goes from 1-0 and this is achieved by connecting QB to the clock input of the most significant FF2 and TC=1.	***Operation 1M***
			***Diagram 2M***
			***Waveform 1M***

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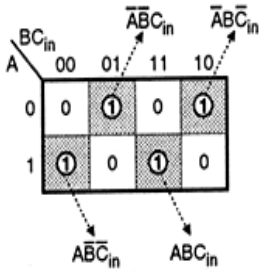
	(f)	**Prove the following using algebraic theorems:** **(i) AB + $\bar{A}$ B + $\bar{A}$ $\bar{B}$ = $\bar{A}$ + B** **(ii) A + $\bar{A}$ B + A$\bar{B}$ = A+ B**	**4M**
	Ans.	**(i) AB + $\bar{A}$ B + $\bar{A}$ $\bar{B}$ = $\bar{A}$ + B** $AB + \bar{A}B + \bar{A}\bar{B} = \bar{A} + B$ LHS $AB + \bar{A}B + \bar{A}\bar{B}$ $= B(A + \bar{A}) + \bar{A}\bar{B}$ $= B + \bar{A}\bar{B}$ $= \bar{A} + B$ **(ii) A + $\bar{A}$ B + A$\bar{B}$ = A+ B** $A + \bar{A}B + A\bar{B} = A + B$ LHS $A + \bar{A}B + A\bar{B}$ $= A + B + A\bar{B}$ $= A(1 + \bar{B}) + B$ $= A + B$	***Correct prove 2M each***
6.	**(a)**	**Attempt any TWO of the following:** **(i) Design full adder circuit using K-map. Implement using logic gates.**	**16** **6M**
	Ans.	**Full Adder:** In Half adder there is no provision to add the carry generated by lower bits while adding present inputs that is when multibit addition is performed. Hence a third input is added and this circuit is used to add A_n, B_n and C_{n-1} where A_n, B_n are present state inputs and C_{n-1} is the last state output that is previous carry. This circuit is known as Full Adder.	

An	Bn	Cn-1	Sum Sn	Carry Cn
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1

Truth table 2M

1	0	0	1	0	
1	0	1	0	1	
1	1	0	0	1	
1	1	1	1	1	

For the sum output



(a) : K-map for sum output

Expression for sum output

$$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + AB\bar{C}_{in} + \bar{A}\bar{B}\bar{C}_{in}$$

$$S = C_{in}(\underbrace{\bar{A}\bar{B} + AB}) + \bar{C}_{in}(\underbrace{\bar{A}B + A\bar{B}})$$

EX-NOR EX-OR

$$\therefore S = C_{in}(\overline{\bar{A}B + A\bar{B}}) + \bar{C}_{in}(\bar{A}B + A\bar{B})$$

Let $X = \bar{A}B + A\bar{B}$

$$\therefore S = C_{in}\bar{X} + \bar{C}_{in}X = C_{in} \oplus X$$

$$\therefore S = C_{in} \oplus (\bar{A}B + A\bar{B})$$

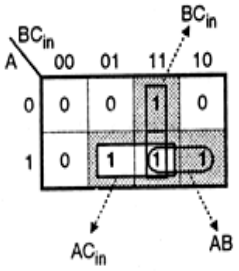
But $\bar{A}B + A\bar{B} = A \oplus B$

$$\therefore S = C_{in} \oplus A \oplus B$$

Expression for carry output

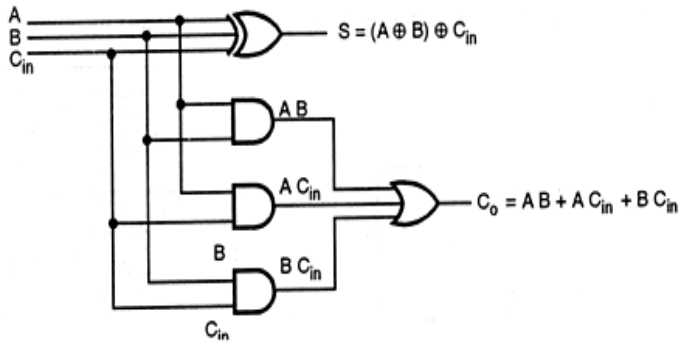
$$C_o = AB + AC_{in} + BC_{in}$$

For carry output



K-map for carry output

Logic diagram for full adder :



K-map for Sum 1M

K-map for Carry 1M

Logical diagram 2M

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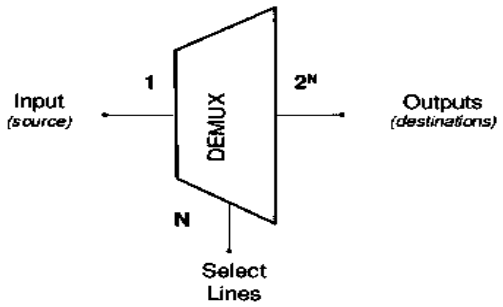
	(a) Ans.	**(ii) Define and draw logical symbol of a demultiplexer.** It has only one input, "n" outputs and "m" select inputs. A demuliplexer performs the reverse operation of a multiplexer i.e. it receives one input and distributes it over several outputs. At a time only one output line is selected lines and the input is transmitted to the selected output line. The enable input will enable the demultiplexer. The relation between the n output lines and m select lines as follows: $n = 2^m$  	**2M** ***Definition 1M*** ***Diagram 1M***
	(b) Ans.	**(i) Differentiate between combinational and sequential logic circuits (2 points).** **Sr. No** / **Combinational circuits** / **Sequential circuits** 1 / In combinational circuits, the output variables depends on the combinational of input variables. / In sequential circuits, the output variables depends upon the present inputs as well as on the past output. 2 / Memory unit is not required in these circuits. / Memory unit is required in these circuits to store the previous output. 3 / These circuits are faster in speed because the delay between the input and output is due to the propogation delay. / Sequential circuits are slower than the combinational circuits. 4 / These are easy to design. / These are complex in designing. 5 / Ex: Parallel Adder. / Ex: Serial Adder.	**2M** ***Any 2 points 1M each***
	(b) Ans.	**(ii) State the applications of shift register.**	**2M**

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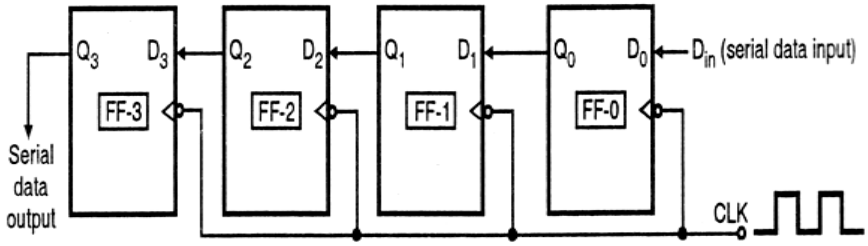
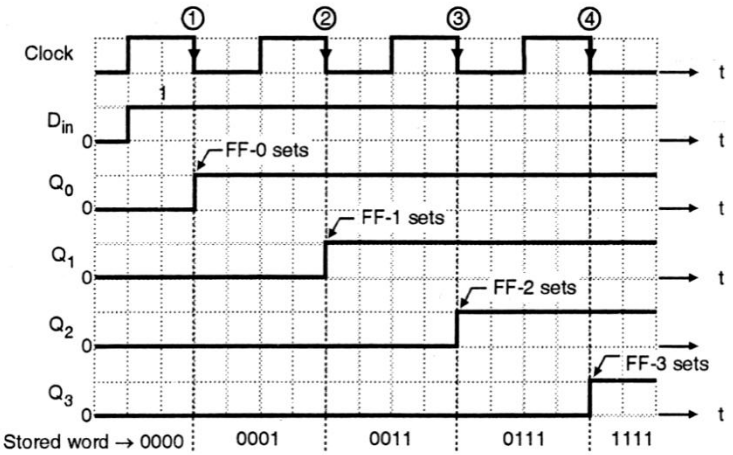
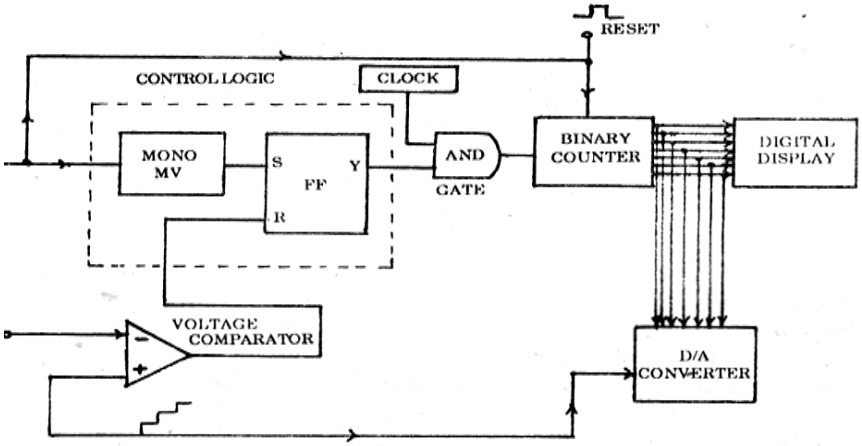
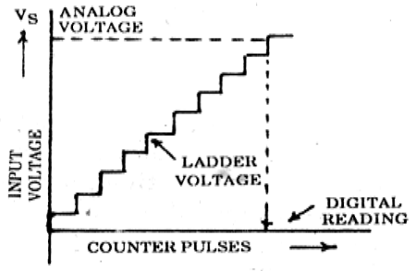
		Applications of shift register: 1. Serial to Parallel Converter 2. Parallel to Serial Converter. 3. Sequence Detector. 4. Counter.	***Any two applications 1M each***
	(b) **Ans.**	**(iii) Draw the block diagram of 4-bit SISO shift register and explain its working with timing diagram.** **Shift Left:** **Working:** Initially all the flip flops are cleared so the output is 0000. When data (assumed data is 1) is applied serially to it is applied at the Din. The arrival of first clock pulse sets the right most flip flop making the output as 0001. With the next clock edge the Q1 flip flop sets and the register contents become 0011. Similarly at the third clock edge results in 0111 and at the fourth clock edge it becomes 1111.   	**4M** ***Working 1M*** ***Diagram 2M*** ***Timing diagram 1M***

	(c) Ans.	**(i) Draw neat diagram of RAMP ADC and explain its working.** This method of A/D conversion uses a binary counter, to count a continuous train of pulses. The pulses are produced from a clock. They pass through a gate, which is normally closed. It opens only when a start signal is applied to initiate a linear ramp. The gate remains open till the linear ramp voltage reaches a value equal to the input voltage to be measured. The counter thus records a number of clock pulses which is proportional to the input voltage. This method is also called counter method. The fig. shows a schematic diagram of a staircase ramp or counter type A/D converter. This method uses a clock source, a counter and a D/A converter.  **(a) Block diagram of a Ramp type ADC**  An analog input is applied to one input of an OP AMP which is used as a voltage comparator. A start or convert pulse is applied to the set input of the flip-flop through a monostable multivibrator (i.e. control logic) and also to the reset input of the binary counter. This pulse	**4M** ***Diagram 2M***

		resets the binary counter and makes it ready for counting. As the counter resets, output of the D/A converter reduces to zero and thus with positive analog input to the voltage comparator, the output of the comparator goes low, which makes R = 0. The start pulse also triggers the monostable multivibrator, which introduces the desired delay in the action of the other circuits. Thus the output of the monostable multivibrator goes high. This makes S = 1, while R was already made 0. The RS flip-flop sets and the Y output goes high. The AND gate is enabled & the counter starts the counting the clock pulses. The output of the counter is fed to n D/A converter which produces an analog output in response to the digital signal as its input. This binary output starts increasing continuously with time. The output of the D/A converter also starts increasing in steps. The analog output is a staircase signal as shown in fig. This D/A output is fed to the reference voltage for the comparator. The staircase signal (i.e. digital output) is compared by the comparator with the analog voltage. So long as the input signal, Vs is greater than the digital output the gate remains enabled and clock pulses are counted by the counter, thus continuously raising the digital output. But as soon as the staircase digital output exceeds the given analog input, the output of the comparator changes from a low to a high level. This makes R = 1, while S is at 0. Thus, the flip-flop resets and Y output goes low. Hence the AND gate is disabled and no clock pulses can now reach the counter. This stops the counting and the binary output of the counter represents the final digital output.	***Explanation 2M***
	(c) Ans.	**(ii) What are advantages and disadvantages of DAC?** For Weighted Resister DAC: **Advantages:** 1. Simple circuit. 2. Easy calculations **Dis-Advantages:** 1. The accuracy and stability of this type of DAC depends upon the accuracy of the resistors used. 2. This type of DAC requires a wide range of resistor values. If the no. of digits n per binary word is 8 then the smallest resistor is 2^0 x R = RΩ, while the largest resistance is 2^7 R = 128R Ω. Thus the	**4M** ***Advantages 2M*** ***Disadvantages 2M***

		largest resistor is 128 times the smaller resistor. This proportion will be still worse for n =12. 3. The difficulty to achieve & maintain accurate ratios over such a wide range of resistor values restricts the use of weighted resistor DAC for the values of n < 8 hence the resolution is poor. 4. The finite resistance of the switches will disturb the currents particularly in the MSB position where the current setting resistors are small in value.	