Subject Name: Electronic Devices \& Circuits
Model Answer Subject Code:

## Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in themodel answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may tryto assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given morelmportance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in thefigure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constantvalues may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

| $\mathrm{Q} .$ <br> No. | Sub <br> Q. <br> N. | Answers | Marking Scheme |
| :---: | :---: | :---: | :---: |
| 1 | A | Attempt any SIX: | 12- Total Marks |
|  | (a) | Name two types of BJT \&draw their symbols. | 2M |
|  | Ans: | Two types of BJT: <br> - NPN <br> - PNP <br> n-p-n transistor <br> p-n-p transistor | 1M for types <br> 1M for symbols |
|  | (b) | Define Q-point | 2M |
|  | Ans: | Q-point: <br> For proper operation of transistor, in any application, we set fixed levels of certain voltages and currents in a transistor. These values of currents and voltages define the | 2M for correct definition |

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|  | To find S : $S=\frac{(1+\beta)}{(1-\beta) \frac{\partial I_{B}}{\partial I_{C}}}$ <br> $\frac{\partial I_{B}}{\partial I_{C}}$ is obtained by diff. $I_{B}$ WRT $I_{S}$ $\begin{aligned} & I_{B}=\frac{V_{C C}-I_{C} R_{C}-V_{B E}}{R_{C}+R_{B}} \\ & \frac{\partial I_{B}}{\partial I_{C}}=\frac{-R_{C}}{R_{C}+R_{B}} \\ & S=\frac{(1+\beta)}{(1-\beta) \frac{-R_{C}}{R_{C}+R_{B}}} \\ & =\frac{(1+\beta)}{(1+\beta) \frac{R_{C}}{R_{C}+R_{B}}} \\ & S=\frac{(1+\beta)\left(R_{C}+R_{B}\right)}{R_{C}+R_{B}+\beta R_{C}} \\ & S=\frac{(1+\beta)\left(R_{C}+R_{B}\right)}{R_{B}+(\beta+1) R_{C}} \end{aligned}$ |  |
| :---: | :---: | :---: |
| (c) | State the need of regulation. Explain the concept of load \& line regulation. | 4M |
| Ans: | Need of Regulation: <br> The major disadvantage of a power supply is that the output voltage changes with the variations in the input voltage or the DC output voltage of the rectifier also increase similarly. In many electronic applications, it is desired that the output voltage, should remain constant regardless of the variations in the input voltage or load. In order to get ensure this ;a voltage stabilizing device called voltage regulator is used. <br> Load Regulation: <br> The load regulation indicates the change in output voltage that will occur per unit change in load current. <br> Mathematically | 2M for need of regulation |

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| Q. <br> No <br> N | Sub <br> Q. <br> N. | Answers | Marking <br> Scheme |
| :--- | :--- | :--- | :--- |
| 2 |  | Attempt any FOUR: | 16- Total <br> Marks |
|  | (a) | State the need of biasing and describe the concept of DC load line |  |
| Ans | Need of Biasing for Transistor: <br> The transistor should be biased in the active region if it is to be used for amplification <br> and in saturation and cut off if it is used as a switch. <br> 2. The Q point should be adjusted approximately at the center of the load line for <br> voltage amplifier application. <br> 3. The value of stability factor (S) should be as small as possible. | 2M for need <br> of biasing |  |

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| $\begin{array}{\|l} \hline \text { Q. } \\ \text { No. } \end{array}$ | $\begin{aligned} & \text { Sub } \\ & \text { Q. } \\ & \mathrm{N} . \end{aligned}$ | Answers | Marking Scheme |
| :---: | :---: | :---: | :---: |
| 3 |  | Attempt any FOUR: | 16- Total Marks |
|  | (a) | In CE configuration if $\beta=90$, leakage current $I_{c E o}=40 \mu \mathrm{~A}$, base current is 0.4 mA , determine $I_{c}$ and $I_{E}$ | 4M |
|  | Ans: | Given: $\begin{aligned} & \beta=90 \\ & \mathrm{I}_{\mathrm{CEO}}=40 \mu \mathrm{~A} \\ & \mathrm{I}_{\mathrm{B}}=0.4 \mathrm{~mA} \end{aligned}$ <br> Required: | Each <br> formula : <br> 2M |

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| Ans: | Working: <br> When the supply voltage $\left(V_{c c}\right)$ is switched ON , the capacitor charges through resistor $(R)$, till the capacitor voltage reaches the voltage level ( $V_{P}$ ) which is called as peak point voltage. At this voltage the UJT turns ON. As a result of this, the capacitor (C) discharges rapidly through resistor (R1). When that capacitor voltage drops to level Vv (called valley- point voltage) the uni- junction transistor switches OFF allowing the capacitor (C) to charge again. In this way because of the charging and discharging of capacitor the exponential sweep voltage will be obtained at the emitter terminal of UJT. The voltage developed at base 1(VB1) terminal is in the form of narrow pulses commonly known as trigger pulses. The sweep period depends upon time constant (R.C) and the sweep frequency can be varied by changing value of either resistance (R) or capacitor (C). Due to this fact, the resistor $R$ is shown as a variable resistor. <br> The sweep period is given by the relation $\begin{aligned} & T=\text { R.C. loge }(1 / 1-\eta) \\ & T=2.3 \text { R.C. } \log _{10}(1 / 1-\eta) \end{aligned}$ | Circuit diagram : 1M <br> Working: 2M <br> Waveform : 1m |
| :---: | :---: | :---: |
| (d) | Draw the frequency response of DC amplifier. Comment on it. | 4M |
| Ans: | frequency response: | Response : 2M |

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| Q. <br> No. | Sub Q. <br> N. | Answers | Marking <br> Scheme |
| :--- | :--- | :--- | :--- | :--- |
| $\mathbf{4}$ |  | Attempt any FOUR: | 12- Total <br> Marks |
|  | (a) | Draw the drain characteristics of p-channel FET and explain. | 4 M |
|  | Ans: | Drain characteristics:- | Characeristics- <br> 2M |


|  |  <br> As VDs is increased from zero as shown, ID will increased proportionally through the p channel. In this region the channel resistance is constants because the depletion region is not large enough to have significant effect. This is called the "Ohmic region" because VDS \& ID are related by ohm's law. <br> As point $B$, the curve level off \& ID becomes essentially constants. <br> As $V_{D s}$ increases from point $B$ to $C$ the reverse bias voltage from gate to drain ( $V_{G D}$ ) produces a depletion region (i.e. channel resistance). It is proportional to the increase in the $V_{D S}$ so the current $I_{D}$ practically constant at $I_{D S S}$. The value of $V_{D S}$ at which $I_{D}$ becomes essentially constant is the pinch off voltage ( $\mathrm{V}_{\mathrm{p}}$ ). <br> Breakdown occurs at point C. when Io begins to increase very rapidly with any further increase in VDS. So JFET's are always operated below breakdown \& within constant current region, <br> As $\mathrm{V}_{\mathrm{Gs}}$ is set increasing, more positive value by adjusting $\mathrm{V}_{\text {GG }}$. Id decreases as the magnitude of $V_{G S}$ is increased because of narrowing width of channel. <br> The maximum value of $V_{G S}$ at which drain current reaches to zero due to overlapping both the depletion layer. (i.e. channel width zero) is called cutoff voltage or $\mathrm{V}_{\mathrm{GS}}$ (off). | Explaination- $2 \mathrm{M}$ |
| :---: | :---: | :---: |
| (b) | Draw the multistage amplifier circuit diagram using RC coupling. State its advantages. | 4M |

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| Ans: | Advantages: <br> 1. It has a wide frequency response. <br> 2. For coupling the resistor and the capacitor are used and which are not expensive so the cost is low. <br> 3. The circuit is very compact and extremely light. <br> 4. It offers a constant gain over a wide frequency band. <br> 5. It is high fidelity amplifier. <br> 6. It provides less frequency distortion. | Diagram-2M <br> Advantages2M(any two) |
| :---: | :---: | :---: |
| (c) | Draw the construction of p-channel D-MOSFET and state its working principle. | 4M |
| Ans: | Construction of p-channel D-MOSFET: <br> Working principle: | Diagram-2M |

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\begin{tabular}{|c|c|c|}
\hline \& \begin{tabular}{l}
The gate to source voltage is set to zero volts by the direct connection from one terminal to the other \& voltage \(V_{D s}\) is applied across the drain to source terminals. This result the flow of current is positively charged holes. \\
When gate is negative with respect to source then the electrons present under the oxide layer are pushed downward into the substrate with a repulsive force and draws additional holes from the N type substrate. Thus drain current (ID) increases as increase in negative value. \\
For positive voltage at gate, the gate will tend to repel holes towards \(N\) type substrate and attract electrons from the substrate toward insulated layer. Recombination occurs between electron \& holes that will reduce the number of free carriers in the channel for conduction. So drain current reduces. The value of voltage of VGS at which drain current nearly becomes zero is called cut off voltage.
\end{tabular} \& \begin{tabular}{l}
Working \\
Principle-2M
\end{tabular} \\
\hline (d) \& Draw the circuit diagram of complementary symmetry Class B push-pull amplifier and describe its working. \& 4M \\
\hline Ans: \& \begin{tabular}{l}
Diagram of complementary symmetry Class B push-pull amplifier: \\
Working: \\
The above circuit employs a NPN transistor and a PNP transistor connected in push pull configuration. When the input signal is applied, during the positive half cycle of the input signal, the NPN transistor conducts and the PNP transistor cuts off. During the negative half cycle, the NPN transistor cuts off and the PNP transistor conducts.
\end{tabular} \& Diagram-2M

Working-2M <br>
\hline
\end{tabular}

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|  | In this way, the NPN transistor amplifies during positive half cycle of the input, while PNP transistor amplifies during negative half cycle of the input. As the transistors are both complement to each other, act symmetrically while being connected in push pull configuration of class B , this circuit is termed as Complementary symmetry push pull class B amplifier. |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| (e) | Compare between class A and class B amplifier on the basis of <br> (i) Efficiency <br> (ii) Power <br> (iii) Position of Q-point <br> (iv) $\mathrm{O} / \mathrm{P}$ distortion |  |  | 4M |
| Ans: | Parameter Class A <br> Efficiency lowest efficiency <br> $25 \%$ to $50 \%$ |  | Class B | 4M(1M <br> for each point) |
|  |  |  | Above 78.5\% |  |
|  | Power | less | More than class A |  |
|  | Position of Q point | Q point is at the centre of load line. | On X axis |  |
|  | O/P disortion | No distortion | More than class A |  |
| (f) | Draw the circuit diagram of Bootstrap's time base generator and explain its working. |  |  | 4M |
| Ans: | Circuit Diagram |  |  | Diagram-2M |

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|  | This causes voltage across capacitor C (and hence the output voltage) to increase <br> linearly with time. <br> The circuit pulls itself up by its own bootstrap and hence it is known as bootstrap <br> sweep circuit. |  |
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| Q. <br> No. | Sub <br> Q. <br> N. | Answers | Marking <br> Scheme |
| :--- | :--- | :--- | :--- | :--- |
| 5 |  | Attempt any FOUR: | 16- Total <br> Marks |
|  | (a) | Draw the input and output characteristics of CE configuration. | 4 M |
|  | Ans: | Input characteristics of CE configuration: | input <br> characteristics- <br> $2 M$ |

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| :---: | :---: | :---: |
| (b) | An RC phase shaft oscillator has $R=4.7 \mathrm{k} \Omega, C=0.01 \mu \mathrm{l}, \mathrm{R}_{1}=1 \mathrm{k} \Omega$ and $\mathrm{R}_{\mathrm{F}}=22 \mathrm{k} \Omega$ <br> (i) Determine whether the oscillations will be sustained. <br> (ii) What will be the frequency of oscillations? | 4M |
| Ans: | i) The operational amplifier gain ( $\mathrm{Av}_{\mathrm{v}}$ ) must be equal to 29 in order to sustain oscillations. $A_{V}=\frac{R_{F}}{R}=\frac{22}{4.7}=4.68$ <br> Since operation amplifier gain is less than 29 the RC phase shift oscillator will not sustain oscillations. <br> Note: Any other method can be considered for calculating sustained oscillations <br> ii) frequency of oscillations: $\begin{aligned} & f=\frac{1}{2 \pi R C \sqrt{6}} \\ & f= \frac{1}{2 \pi * 4.7 * 10^{3} * 0.01 * 10^{-6} * \sqrt{6}} \\ &=1.38 \mathrm{kHz} \end{aligned}$ | $2 M$ <br>  <br>  <br>  <br>  <br> $2 M$ |
| (c) | Draw the single stage class A power amplifier circuit diagram and draw the input and output waveforms. | 4M |

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Ans: Circuit diagram:-
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Ans:
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load. The input voltage ranges from 9.5 to 40 V and it can regulate voltage from 2 V to 37 V .
i) LM 723 can be used as low voltage regulator:


This circuit is basically used to obtained $2 v$ to 7 v . In order to achieve this (Vo<Vref) a potential divider is required to be connected between Vref pin and ground. Therefore the voltage at the non inverting terminal of the error amplifier due to R1 R2 divider is-
$\mathrm{VNI}=\mathrm{Vref} \frac{\mathrm{R} 2}{\mathrm{R} 1}$

The difference between VNI and the output voltage Vo which is directly fed back to the Inverting terminal is amplified by the error amplifier. The output of the error amplifier drives the pass transistor so as to minimize the difference between the non inverting and inverting input of error amplifier.

Therefore $\mathrm{Vo}=\mathrm{Vref} \frac{\mathrm{R} 2}{\mathrm{R} 1+\mathrm{R} 2}$
ii) LM 723 can be used as high voltage regulator:

Any one 4 M
(either low voltage regulator or high voltage regulator)
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|  |  | Note: Other method for regulator also can be consider. |  |
| :--- | :--- | :--- | :--- |


| $\begin{aligned} & \text { Q. } \\ & \text { No. } \end{aligned}$ | Sub Q. N. | Answers | Marking Scheme |
| :---: | :---: | :---: | :---: |
| 6 |  | Attempt any FOUR: | 16- Total Ma |
|  | (a) | Draw the circuit of voltage divider for BJT \& explain its working. | 4M |
|  | Ans: | Working :- <br> Figure shows the circuit of a voltage divider bias. The name voltage divider is derived from the fact that resistors $R_{1}$ and $R_{2}$ form a potential divider across the supply $V c c$. By suitably selecting this voltage divider network, the operating point of the transistor can be made almost independent of current gain $\beta$. To set the operating point $Q$, first determine the base current. To get more accurate value of base current, Thevenin's Theorem is used. <br> Now applying the Thevenin's theorem, we get the voltage, | Circuit diagr : 2M <br> Working: 2M |

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