17627

21718

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*
(2) Illustrate your answers with neat sketches ***wherever*** *necessary.*
(3) Figures to the ***right*** *indicate* ***full*** *marks.*
(4) Assume suitable data, if ***necessary****.*
(5) Use of Non-programmable Electronic Pocket Calculator is ***permissible****.*
(6) Mobile Phone, Pager and any other Electronic Communication devices are ***not*** *permissible in Examination Hall.*

Marks

1. a) Attempt **any three** of the following : **(3×4=12)**

i) List any four salient features of 80386.

ii) Explain super scalar execution stages of Pentium with neat diagram.

iii) State any four advantages of RISC processor.

iv) State any four difference between .com and .exe program.

b) Attempt a**ny one** of the following : **(1×6=6)**

i) Describe the eight stage pipeline mechanism in floating point unit of Pentium processor.

ii) Draw and explain internal architecture of 80386.

2. Attempt **any four** of the following : **(4×4=16)**

a) Explain any two system address registers of micro-processor 80386 with neat diagram.

b) Draw the block diagram of Pentium-System architecture.

c) What is MMX ? State its benefits.

d) State any four features of SUN Ultra SPARC.

e) State the function of INT 17H. Give any two examples.

f) Explain interrupt processing sequence of X86 microprocessor.

3. Attempt **any four** of the following : **(4×4=16)**

a) Describe enabling and disabling of paging in 80386 with neat diagram.

b) List any four important features of Pentium processor.

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Marks

c) Distinguish between LDTR and GDTR (Any four points).

d) State the instruction latency in RISC processor designing.

e) Describe divide by zero error and single step interrupts of X86 processors.

4. a) Attempt **any three** of the following : **(3×4=12)**

i) Explain the flag register format of 80386 with suitable figure.

ii) Explain separate code and data cache of Pentium micro processor.

iii) Explain the concept of pipelining in RISC processor.

iv) State the functions of following interrupts :

1) INT 10 H : Function 06H and 07H

2) INT 21H : Function 01H and 02H.

b) Attempt **any one** of the following : **(1×6=6)**

i) Describe Pentium-II processor with respect to cache memory, memory banking and input/ output system.

ii) Explain interrupt vector table of X86 processor with neat diagram.

5. Attempt **any four** of the following : **(4×4=16)**

a) Describe the function of following pins of 80386 :

i) $\overline{BE_0} - \overline{BE_3}$ ii) $D/\overline{C}$

iii) $\overline{LOCK}$ iv) $\overline{BUSY}$

b) Explain function of branch prediction unit in Pentium processor.

c) State features of Pentium-III processor. (any four).

d) What do you mean by register windowing in RISC processor ?

e) List hardware interrupts of X86 processors. Explain in brief about overflow interrupt.

f) Draw and explain virtual 8086 mode in 80386.

6. Attempt **any four** of the following : **(4×4=16)**

a) Describe debug and test register of 80386 microprocessor.

b) Describe the features of Pentium MMX (any four).

c) List and explain design issues of RISC processor (any two).

d) List any four features of Pentium-proprocessor.

e) Explain the concept of segment descriptor cache register of 80386 with neat diagram.

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