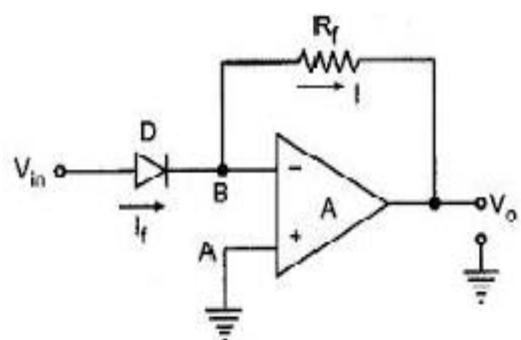
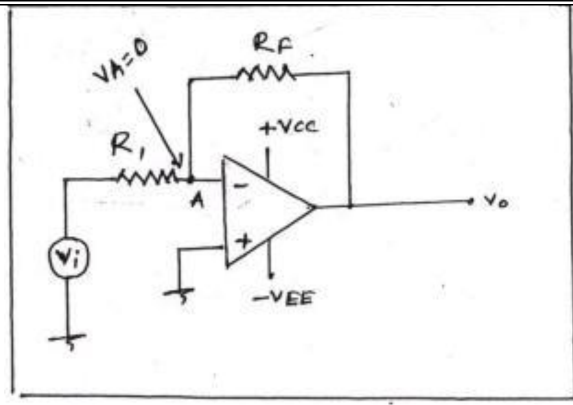
# SUMMER – 2022 EXAMINATION

**Subject Name: Analog Circuits** **Model Answer** **Subject Code: 22433**

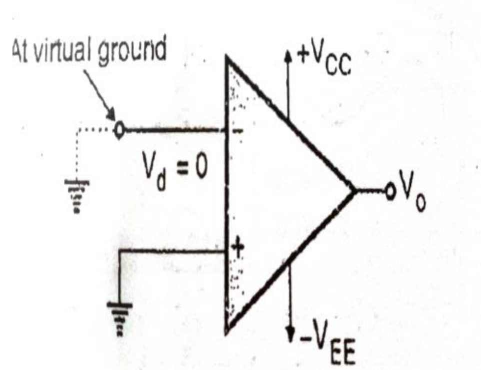
**Important Instructions to examiners:**

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.
8) As per the policy decision of Maharashtra State Government, teaching in English/Marathi and Bilingual (English + Marathi) medium is introduced at first year of AICTE diploma Programme from academic year 2021-2022. Hence if the students in first year (first and second semesters) write answers in Marathi or bilingual language (English +Marathi), the Examiner shall consider the same and assess the answer based on matching of concepts with model answer.

| Q. No. | Sub Q. N. | Answer | Marking Scheme |
|---|---|---|---|
| 1. | | **Attempt any FIVE of the following:** | **10 M** |
| | a | **Draw circuit diagram of antilog amplifier.**<br>**Ans:**<br><br><br>Fig: Antilog amplifier | **02** |
| | b | **Describe virtual ground concept with reference to op-amp.**<br>**Ans:** | |




**OR**




01

In circuit point $V_A$ is virtual ground. Figure shows inverting amplifier using op-amp. In this circuit non-inverting terminal is connected to the actual ground. Due to this potential of inverting terminal become zero. Thus, inverting terminal is not actually connected to the ground. There after its potential is zero. Thus point $V_A$ is known as virtual ground point. This phenomenon of having zero potential without actually grounding is known as virtual ground concept.

01

**c** **Identify the given circuit as shown in Fig No. 1**

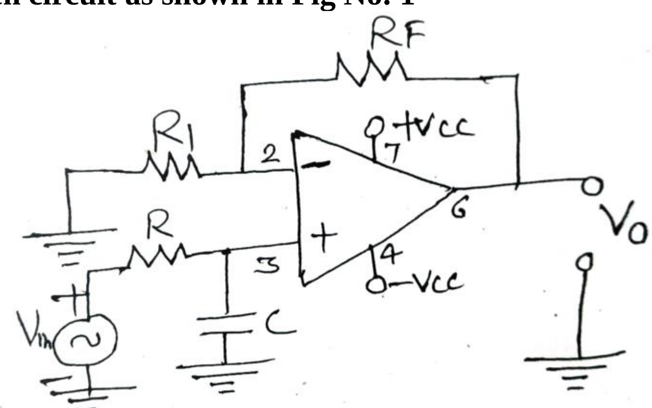



Fig. No. 1.

P.T.O.

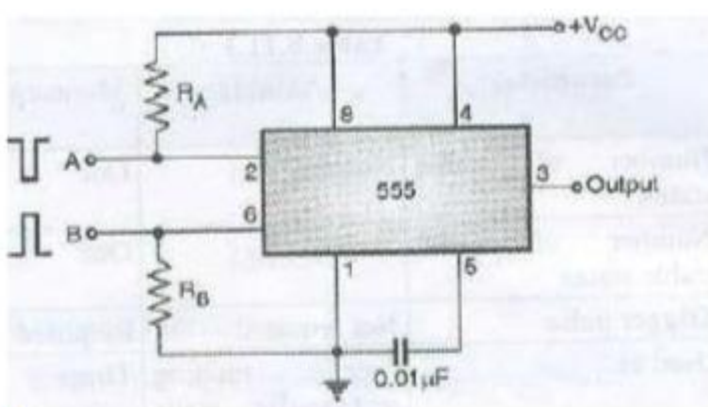
**Ans:**

**Fig. No 1 is First order Low pass Butterworth Filter**

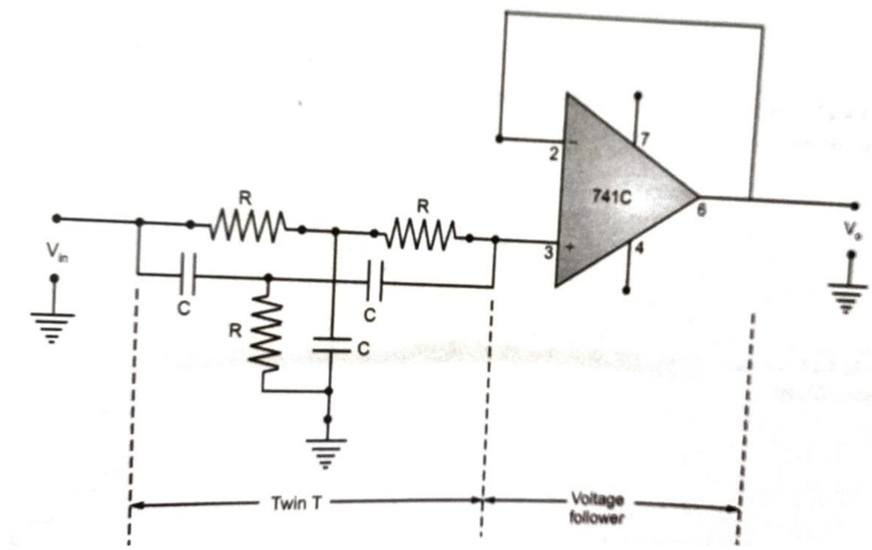
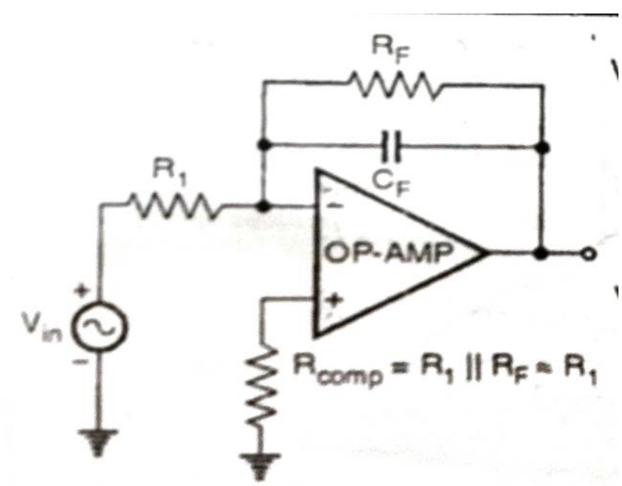
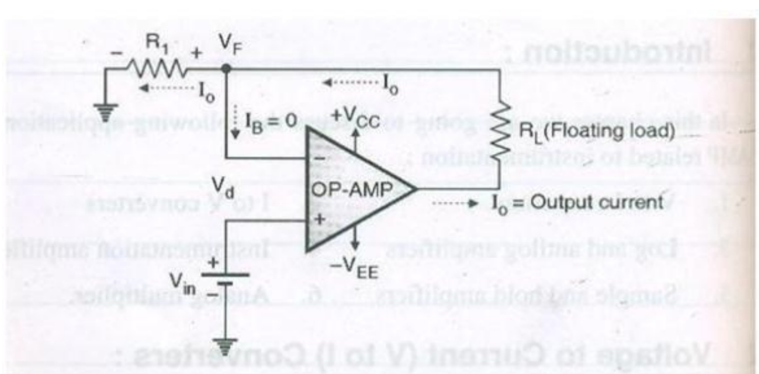
02

**d** **Draw bistable multivibrator using IC555.**

**Ans:**




02

<table>
<tr><td></td><td>e</td><td>Draw circuit diagram of Notch filter using op-amp.<br>Ans:<br><br><br>Circuit diagram of Notch Filter</td><td>02</td></tr>
<tr><td></td><td>f</td><td>Draw circuit diagram of practical integrator using op-amp.<br>Ans:<br><br><br>Practical Integrator</td><td>02</td></tr>
<tr><td></td><td>g</td><td>Draw circuit diagram of V to I converter using of op-amp with floating load.<br><br><br>Fig. : Voltage to current converter with floating load</td><td>02</td></tr>
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| 2. | | **Attempt any <u>THREE</u> of the following:** | **12 M** |
|---|---|---|---|

**a** **Draw and explain the circuit diagram of antilog multiplier using op-amp.**

**Ans:**

(S-18, W-17)

Fig. 3.16 shows the block diagram of analog multiplier. It is the application of log and antilog amplifier.

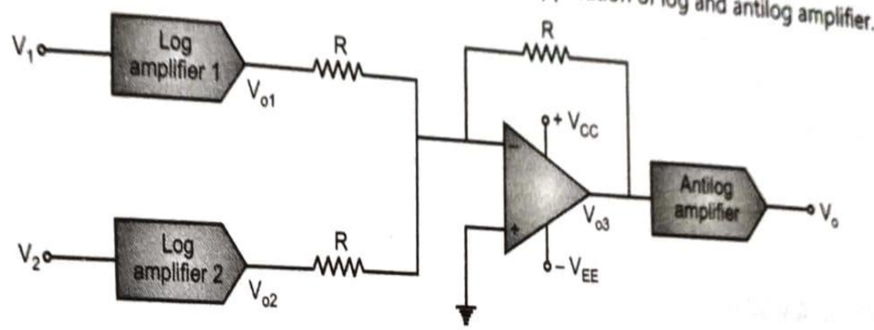



**Fig. 3.16 : Analog Multiplier**

It consists of two log amplifiers, an adder circuit and an antilog amplifier as shown in Fig. 3.16. It is the application of log and antilog amplifiers.

**02**

The output of each log amplifier is given by

$$V_{o1} = -K_1 \log V_1 \text{ and } V_{o2} = -K_1 \log V_2 \quad \dots (3.26)$$

The output of adder is $V_{o3} = -(V_{o1} + V_{o2}) \quad \dots (3.27)$

$$= K_1 \log V_1 + K_1 \log V_2 = K_1 \log V_1 \cdot V_2$$

The output of antilog amplifier will become

$$V_o = K_2 \log^{-1} (K_3 \cdot V_{o3}) = K_2 \log^{-1} (K_3K_1 \log V_1 \cdot V_2)$$

$$V_o = K_2K_3K_1 V_1 \cdot V_2$$

$$\boxed{V_o = K_4 V_1 \cdot V_2} \quad \text{as } K_4 = K_2 \cdot K_3 \cdot K_1 \quad \dots (3.28)$$

**02**

**b** **With neat sketch derive the expression for output voltage of Inverting amplifier.**

**Ans:**

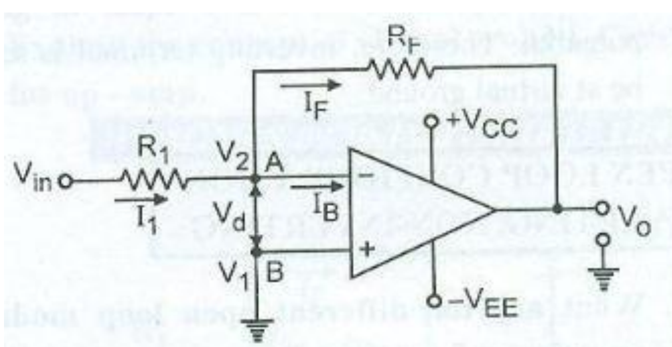



Fig. OP-Amp as an inverting amplifier

**02**

$V_o$= output voltage, $V_{in}$= input voltage, $R_F$= Feedback resistor, $R_1$= Input resistor

1. As input signal $V_{in}$ is applied to inverting input, hence it is called as inverting amplifier and non inverting terminal is grounded.
2. The phase difference between input and output is $180^0$
3. A negative feedback is provided from output to inverting terminal through $R_F$ (Feedback resistor)

Derivation:

Apply KCL at node 'A', we get,

$$I_1 = I_B + I_f \quad \text{--- (1)}$$

But, $R_{in} = \infty$

$\therefore I_B = 0$

$\therefore I_1 = I_F$

$$\therefore \frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_o}{R_F}$$

According to virtual ground condition,

$V_1 = V_2 = 0$

$$\therefore \frac{V_{in}}{R_1} = \frac{-V_o}{R_F}$$

$$\therefore \boxed{V_o = -\left(\frac{R_F}{R_1}\right) V_{in}} \quad \text{--- (2)}$$

$$\therefore \boxed{A_V = \frac{V_o}{V_{in}} = \frac{-R_F}{R_1}} \quad \text{--- (3)}$$

where, $A_V$ = closed loop voltage gain

**02**

**c** **Design the first order low pass Butterworth filter with high cutoff frequency 10 KHz and pass band gain of 11**

**Ans:**

Given : $f_H = 1\,KHz$, $A_F = 11$

To find : $R_F = ?$ , $R_1 = ?$ , $C = ?$

Solution :— Assuming $C = 0.01 \mu F$

$$\therefore C = 0.01 \times 10^{-6} F$$

$$R = \frac{1}{2\pi f C}$$

$$= \frac{1}{2\pi \times 1 \times 10^{3} \times 0.01 \times 10^{-6}}$$

$$\therefore R = 15.92\ k\Omega$$

**02**

$$A_F = 1 + \frac{R_F}{R_1}$$

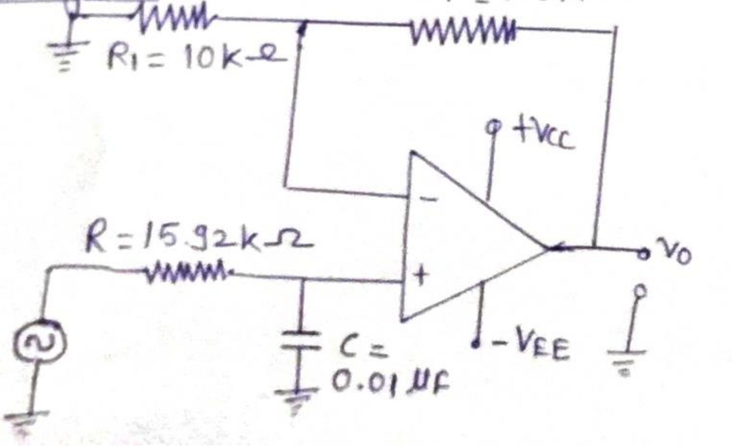
$$\therefore 11 = 1 + \frac{R_F}{R_1} \quad \therefore 11 - 1 = \frac{R_F}{R_1}$$

$$\therefore 10 = \frac{R_F}{R_1}$$

$$\therefore \text{Assuming } \frac{R_F}{R_1} = \frac{100\ k\Omega}{10\ k\Omega}$$

$$\therefore R_F = 100\ k\Omega \text{ and } R_1 = 10\ k\Omega$$

Circuit Diagram: →




**02**

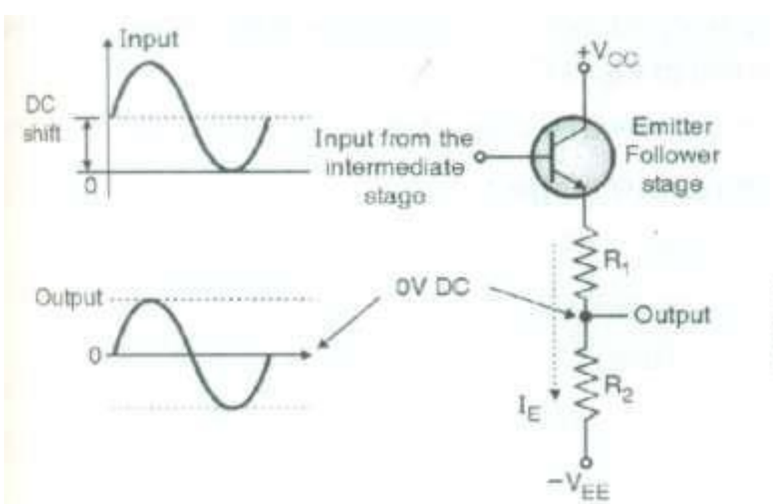
**d** **Compare linear and non-linear op-amp (any four points)** — 04

**Ans:**

| Sr. No | Parameters | **Linear op-amp** | **non-linear op-amp** |
|---|---|---|---|
| 1 | Definition | The output voltage or current which is directly proportional to either input voltage or current are called linear Op-Amp Circuits | A non linear OP-Amp is one in which the output signal is not directly proportional to the input signal. |
| 2 | Example | Inverting amplifier Non-inverting amplifier. Integrator, differentiator | Zero crossing detector, Schmitt trigger, Voltage comparator |
| 3 | Working mode | In linear application op-amp works in amplifier mode | In nonlinear application op-amp works in switching mode |
| 4 | Bandwidth | Bandwidth is high | Bandwidth is low |
| 5 | Gain | Voltage gain is low as compared to non-linear op-amp | Voltage gain is very high |

**3.** **Attempt any THREE of the following:** — **12 M**

**a** **Describe the level shifting stage of op-amp with circuit diagram.** — 02



Level shifting stage is used to bring the dc level to zero volts w.r.t. ground.

Explanation:-Op-amp is a direct coupled amplifier, So when input is zero or at ground potential, the output of op-amp will be at some positive DC level which an error voltage is called as offset voltage. So in order to pull this o/p DC offset voltage to zero, the DC level shifter is used.

**02**

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**b** **Design and draw the circuit diagram following operation using op-amp**
**$V_O = V_1 + V_2 - 2V_3$**
**Ans:**

**Ans.** Assume, $R = 1\ k\Omega$

Hence output of first inverting amplifier $V_{o1} = \frac{-R}{R}(V_1 + V_2) = -(V_1 + V_2)$.

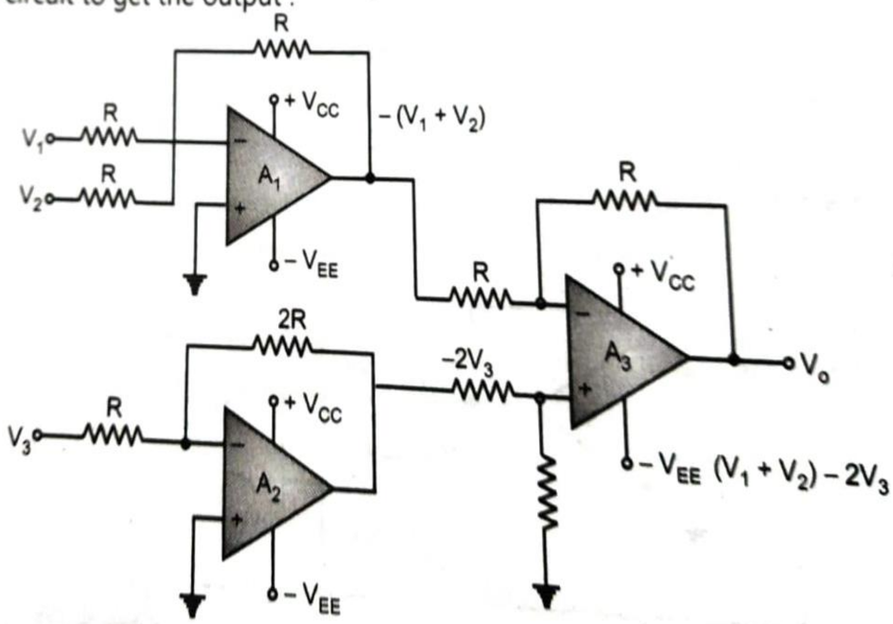
**02**

Output of second inverting amplifier is $V_{o2} = \frac{-2R}{R}(V_3) = -2V_3$

Therefore, final output of third difference amplifier is derived as,

$$V_o = V_{o2} - V_{o1} = [-2V_3 + (V_1 + V_2)] = V_1 + V_2 - 2V_3$$

The designed circuit to get the output :




**02**

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**c** **Draw the circuit diagram of Astable multivibrator using IC 555 to obtain 50% duty cycle. Determine the components used at 1 KHz frequency when $C_T$ = 1µF and draw the waveform of Astable Multivibrator.**
**Ans:**

**Solution:** If the duty cycle ≤ 50%, the diode should be used to bypass resistor $R_B$ (i.e. circuit of square wave generator using astable).

Time period for 1 kHz frequency = 1/f = 1 ms

01

$$T_{on} = T_{off} = 0.5 \text{ ms}$$

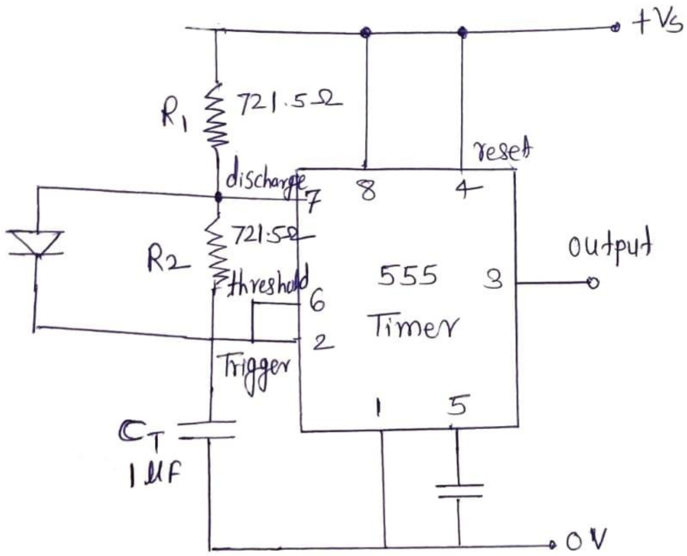
$$C = 1\mu F \text{ (given)}$$

$$T_{ON} = 0.693 R_A C$$

$$\therefore R_A = \frac{T_{ON}}{0.693 \times C} = \frac{0.5 \times 10^{-3}}{0.693 \times 1 \times 10^{-6}} = \mathbf{721.5\ \Omega}$$

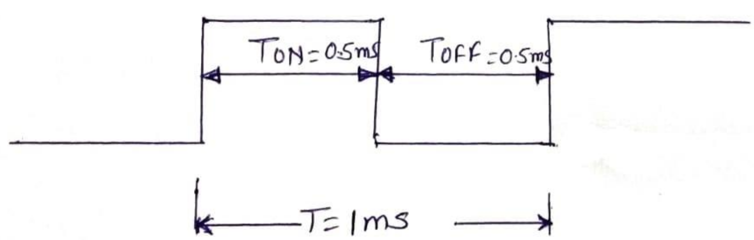
$$R_B = \frac{T_{OFF}}{0.693 \times C} = \frac{0.5 \times 10^{-3}}{0.693 \times 1 \times 10^{-6}} = \mathbf{721.5\ \Omega}$$

* Circuit diagram of astable multivibrator




02

* output waveforms of Astable Multivibrator




01

**d** **Design a second order Butterworth active HPF with cutoff frequency 1.5 KHz and C = 0.01µF.**

**Ans:**

**Solution : Given :** $f_L = 1.5$ kHz. Let $R_2 = R_3 = R$ and $C_2 = C_3 = C = 0.01\ \mu F$.

$$f_L = \frac{1}{2\pi RC}$$

$$\therefore \quad R = \frac{1}{2\pi \times 1.5 \times 10^3 \times 0.01 \times 10^{-6}}$$

$$\boxed{R = 10.6\ k\Omega}$$

**02**

$$A_f = 1 + \frac{R_f}{R_1} = 1.586$$

$$\therefore \quad \frac{R_F}{R_1} = 0.586$$

$$\therefore \quad R_F = 0.586\ R_1$$

Let $R_1 = 10\ k\Omega$

$$\therefore \quad R_F = 0.586 \times 10 \times 10^3 = \boxed{5.86\ k\Omega}$$

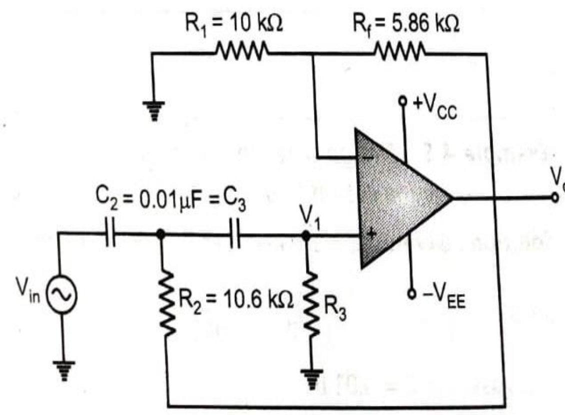
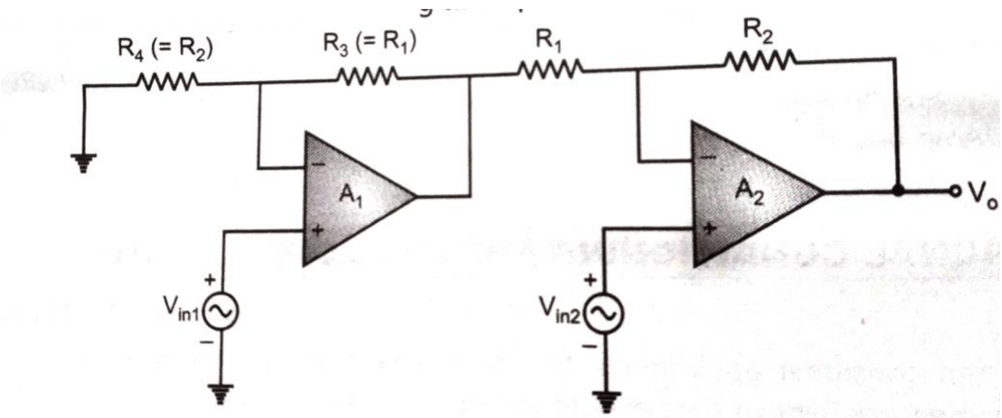



Fig. 4.21

**02**

**4.** **Attempt any <u>THREE</u> of the following:** **12 M**

**a** **Draw circuit diagram and write output equation of instrumentation amplifier using two op-amps.**




. 3.2 : Instrumentation Amplifier using Two OP-AMPs

**03**

**Output equation of instrumentation amplifier using two op-amps:**

$$\boxed{V_o = \left[1 + \frac{R_2}{R_1}\right] [V_{in2} - V_{in1}]}$$

**01**

**b** **Design circuit diagram of open for non-inverting amplifier to obtain the gain of 15 calculate the output for**

**i) $V_{in} = 0.5\ V_{dc}$**

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**ii) $V_{in} = 0.5\ V_{pp}$ sine wave**

**Ans:**

**Soln. :**

**Given :** Non-inverting amplifier. $A_{VF} = 15$

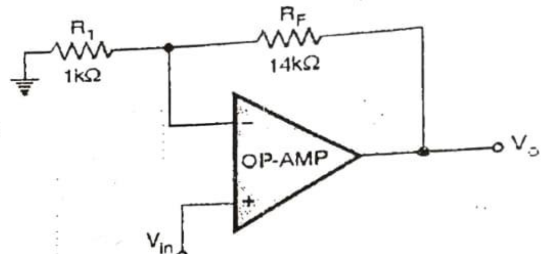
**Step 1 : Draw the circuit diagram :**

$$A_{VF} = 15 = \left(1 + \frac{R_F}{R_1}\right) \quad \ldots\text{(given)}$$

$$\frac{R_F}{R_1} = 14 \qquad \therefore \quad R_F = 14\ R_1$$

Let $R_1 = 1\ k\Omega$

$\therefore \quad R_F = 14\ k\Omega$ **...Ans.**




(K-1059)**Fig. P. 2.4.5(a) : Circuit diagram of non-inverting amplifier**

**Step 2 : Calculate output voltage :**

1. $V_{in} = 0.5\ V_{dc}$

Output voltage $= A_{VF} \times V_{in} = 15 \times 0.5 = 7.5\ V_{dc}$

2. $V_{in} = 0.5\ V_{PP}$

Output voltage $= A_{VF} \times V_{in} = 15 \times 0.5 = 7.5\ V_{PP}$

**Step 3 :**

</td><td>

**02**

**01**

**01**

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<tr><td></td><td>**c**</td><td>

**Identify the circuit shown in Fig NO. 2 and draw the output waveform if the input is a square wave.**

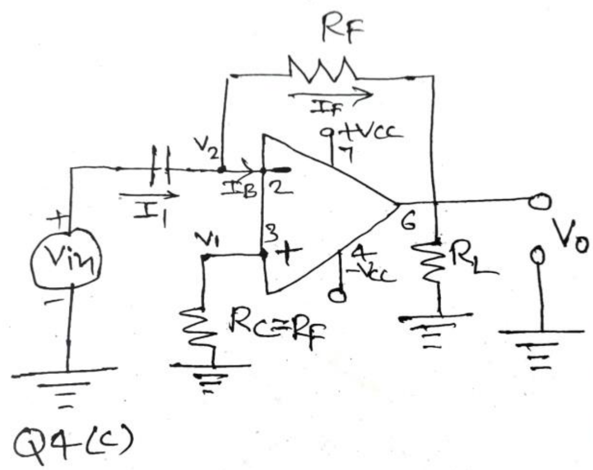


**Fig. No. 2.**

**Ans:**

Fig NO. 2 circuit is active differentiator

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**02**

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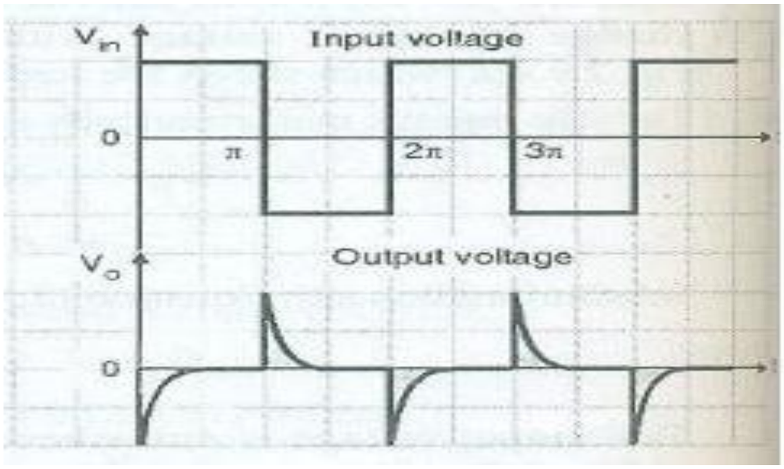
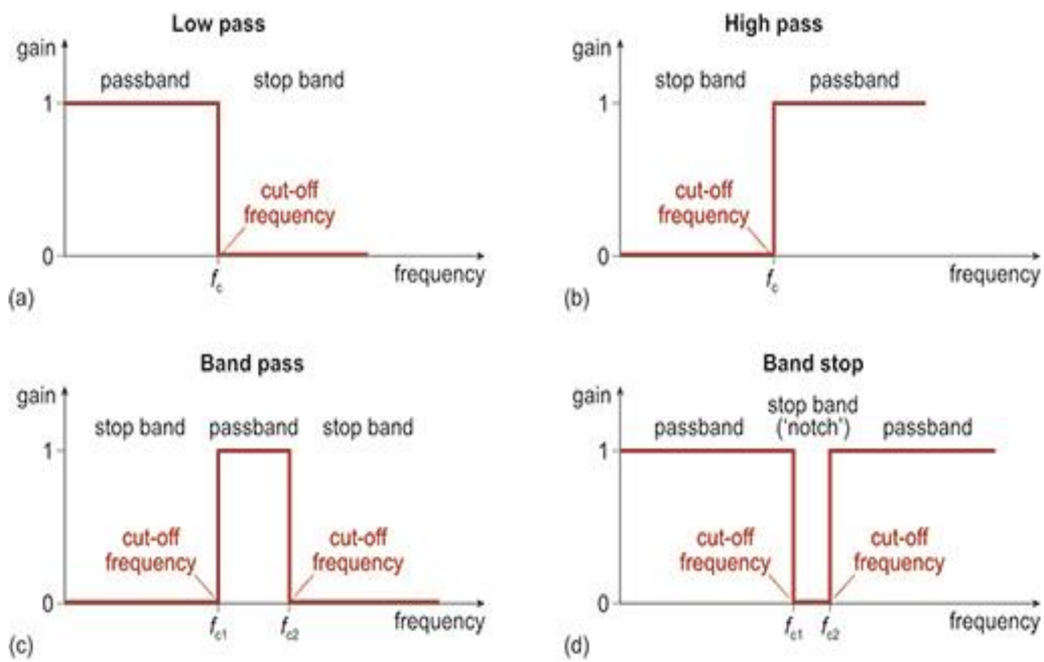



**Input and output voltage waveforms of Differentiator**

**02**

**d** **Draw the ideal frequency response for LPF, HPF, BPF and BRF.**

**Ans:**

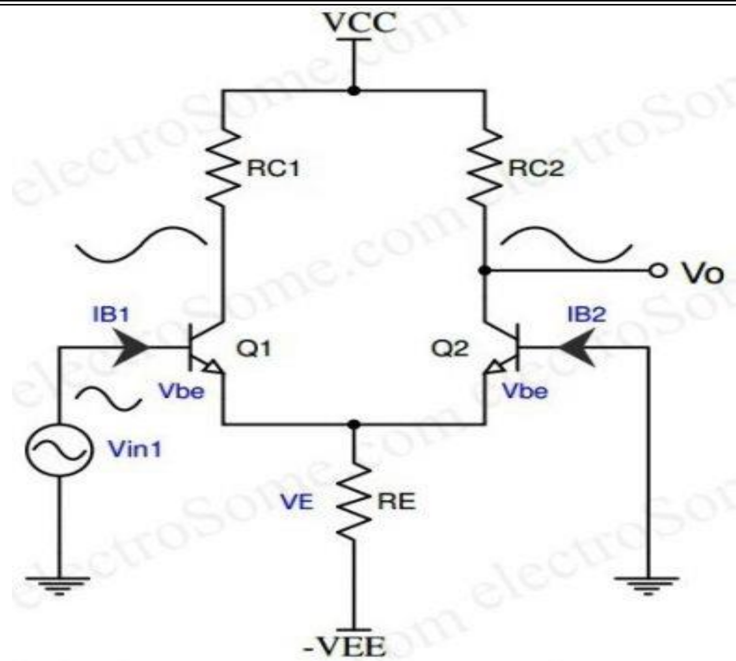
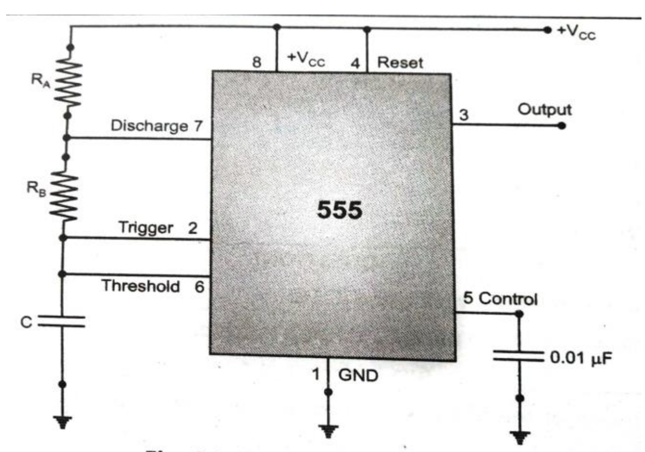


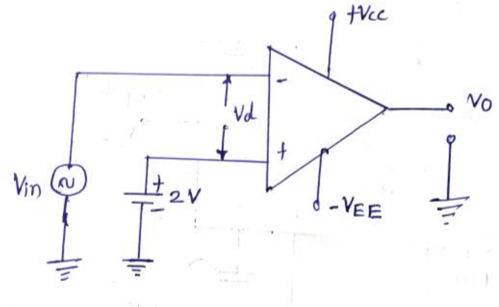

**04**

**5.** **Attempt any <u>TWO</u> of the following:** **12 M**

**a** **Draw and explain circuit diagram of single input unbalanced output differential amplifier.**

**Ans:** In this case, only one input signal is given and the output is taken from only one of the two collectors with respect to ground as shown below.

| | | | |
|---|---|---|---|
| | | <br>When input signal $V_{in1}$ is applied to the transistor Q1, it's amplified and inverted voltage gets generated at the collector of the transistor Q1. At the same time it's amplified and non-inverted voltage gets generated at the collector of the transistor Q2 as shown in the above diagram. Unbalanced output will contain unnecessary dc content as it is a dc coupled amplifier therefore this configuration should follow by a level translator circuit. | 03<br><br>03 |
| | b | **Draw the circuit diagram of Astable multivibrator using IC 555 and give the expression for $T_{ON}$, $T_{OFF}$, $T_{total}$ and duty cycle.**<br>**Ans:**<br><br>**Fig. 6.9: Astable Multivibrator**<br>$T_{ON} = T_C = 0.693 * (R_A + R_B) C$<br>$T_{OFF} = T_D = 0.693 * R_B C$<br>Duty Cycle = $T_{ON} + T_{OFF}$<br>$\%D = ((R_A + R_B)/(R_A + 2 R_B)) * 100$ | 03<br><br>01<br><br>01<br><br>01 |
| | c | **Draw the comparator circuit using op-amp to detect + 2V dc signal.**<br>**Ans:** | |

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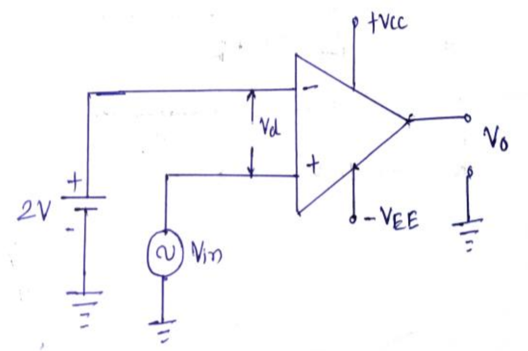


**Inverting mode comparator** **Non- inverting mode comparator**

**06**

**6.** **Attempt any <u>TWO</u> of the following:** **12 M**

**a** **Compare the features of integrator and differentiator. (any six points)**

**Ans:**

| **Integrator** | **Differentiator** |
|---|---|
| A circuit that gives an output voltage directly proportional to the integral of its input is known as an integrating circuit. | A circuit that gives an output voltage directly proportional to the derivative of its input is known as a differentiating circuit. |
| Output Voltage $V_o = -\frac{1}{R_1 C_F}\int_1^t V_{in}\, dt + k$ | Output Voltage $V_o = -R_F C_1 \frac{d}{dt} V_{in}$ |
| It is used as low pass filter | It is used as high pass filter |
| It works good in low frequency | It works good in high frequency |
| Feedback element is capacitor | Feedback element is Resistor |
| Gain decreases with increase in frequency | Gain increases with increase in frequency |
| More stability | Less stability |
| Effect noise is less | Effect noise is more |

**06**

**b** **List ideal and practical parameter of op-amp.**

**Ans:**

**Ideal parameter of op-amp ( Any three)**

1. Infinite Voltage Gain
2. Infinite Input Impedance
3. Zero Output Impedance
4. Zero Input Offset Voltage
5. Zero Output Offset Voltage
6. Zero Input Offset current
7. Zero Input Bias current
8. Infinite Bandwidth
9. Infinite CMRR
10. Infinite Slew Rate
11. Zero Power Supply Rejection Ratio(PSRR)
12. Zero Input capacitance

**03**

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**Practical parameter of op-amp. ( Any three)**

1. Voltage Gain - 200,000
2. Input Impedance - 2MΩ
3. Output Impedance - 75Ω
4. Input Offset Voltage - 6mV
5. Output Offset Voltage - 15mV
6. Input Offset current - 10nA
7. Slew Rate - 0.5V/µS
8. CMRR - 90dB
9. Input Bias current - 80 nA
10. Power Supply Rejection Ratio(PSRR) - 150µv/V
11. Bandwidth – 1MHz
12. Input capacitance – 1.4pF

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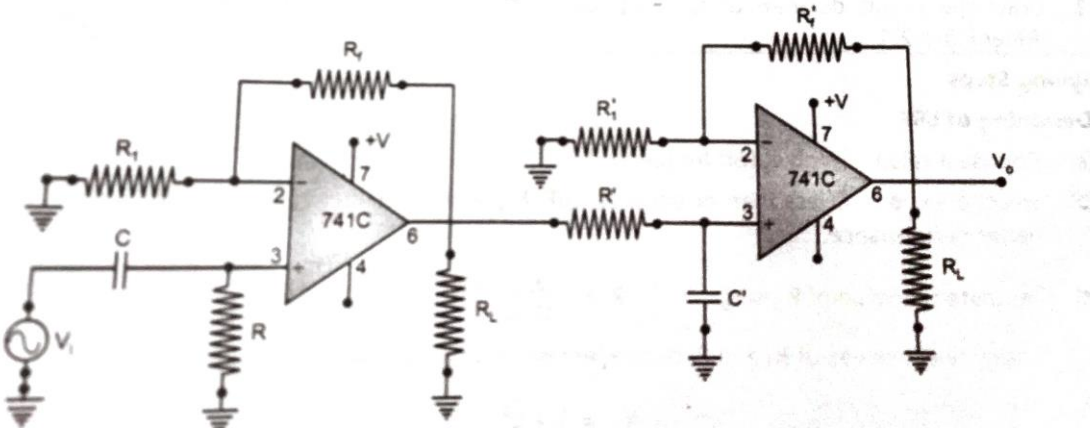
**Describe wideband pass filter with circuit diagram.**
**Ans:**




This filter gives quality factor less than 10, hence response is wider. It can be formed when high pass and low pass filter are cascaded.

To achieve a band pass response, $f_H$ should be greater than the $f_L$. The voltage gain of the band pass filter is the product of the voltage gain of low pass and high pass filter.

$$\left|\frac{V_o}{V_i}\right| = \text{gain of first order LPF} \times \text{Gain of first order HPF} = \frac{A_{f_1}}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}} \times \frac{A_{f2}\left(\frac{f}{f_L}\right)}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}} = \frac{A_{f12}\left(\frac{f}{f_L}\right)}{\sqrt{\left[1+\left(\frac{f}{f_H}\right)^2\right]\left[1+\left(\frac{f}{f_L}\right)^2\right]}}$$

where, $A_{f_{12}}$ is the overall gain of band pass filter.

Wide band pass filter gives figure of merit (i.e. Q) lesser than 10 hence response is wider. This can be made narrow band pass filter if figure of merit is made greater than 10.

Q < 10 – Wide Band Pass Filter.

Q > 10 – Narrow Band Pass Filter.

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