17320

11920

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Assume suitable data, if necessary.

(5) Use of Non-programmable Electronic Pocket Calculator is permissible.

(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. Attempt any TEN of the following: **20**

a) Convert the following decimal numbers to the binary form.

(i) $(25.5)_{10}$

(ii) $10.625)_{10}$

b) Draw truth table for logic gates represented by the following IC's :

(i) IC 7402

(ii) IC 7486

c) State the number of flip flops required to construct the following modulus of a counter.

(i) 11

(ii) 85

P.T.O.

Marks

d) Draw the logical diagram of OR gate using NOR gate and NAND gate only.

e) State different triggering methods in digital circuits.

f) Draw the logic circuit diagram of 1 bit memory cell using NAND gate.

g) Identify SOP and POS equations

(i) A + BC + CD

(ii) (A+B) (C+D)

h) Convert the following binary number to gray code.

(i) 1101001

(ii) 11111

i) Compere E^2 PROM and EPROM (any two points).

j) Convert the following decimal numbers to hexadecimal numbers.

(i) 95.5

(ii) 675

k) Implement the given logical equation using gates $y = A \cdot (B+C)$.

l) Define following characteristics of logic families.

(i) Propagation delay.

(ii) Power dissipation.

m) Draw symbol and truth table of D filpflop.

n) Define Accuracy and settling time w.r.t. DAC.

Marks

2. Attempt any FOUR of the following: **16**

a) Subtract using 2's complement method.

(i) $(1110)_2 - (1001)_2$

(ii) $(0101)_2 - (1001)_2$

b) Design 1:32 MUX using 1:8 MUX.

c) State and prove De Morgan's theorems.

d) Compare volatile and non-volatile memories (any four points).

e) Design half adder using K-map and implement using gates.

f) How many bits are required for a resolution of 5 mV and full scale voltage is 15 V.

3. Attempt any FOUR of the following: **16**

a) Draw the circuit diagram of 3 bit asynchronous counter with its truth table and output wareforms.

b) Draw circuit diagram of TTL NAND gate and explain its working.

c) Compare combinational and sequential circuits (any four points).

d) Realize following expression using MUX.:

$f = \sum m\ (0, 1, 2, 3, 5, 9)$

e) Compare between R–2R ladder DAC and weighted resistor DAC (any four points)

f) Design mod 6 counter using IC 7490

Marks

4. Attempt any FOUR of the following: **16**

a) Describe the Race around condition? How will it be eliminated in J-K flip flop.

b) State the rules of BCD addition.

c) Explain working of single slope ADC with diagram.

d) Identify the given circuit and write its truth table and draw its output waveforms. Refer fig. No. 1

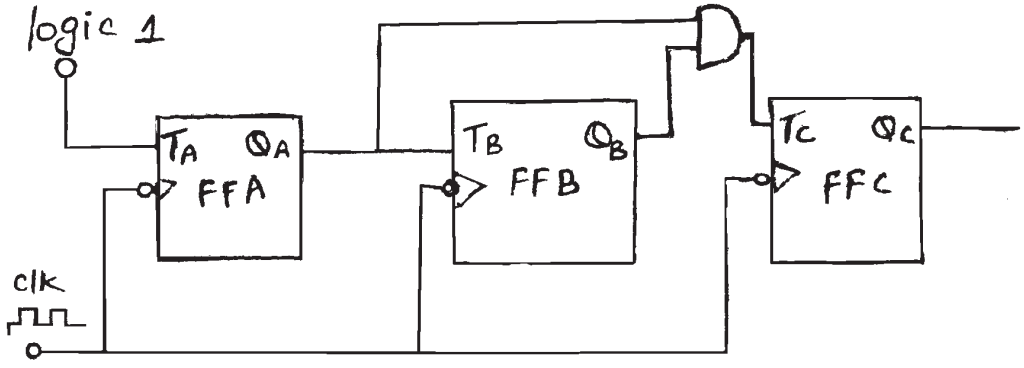

Fig. No. 1

e) Minimize the following expression using K-Map.

f (P, Q, R, S) = $\sum$ m (0, 1, 4, 5, 7, 8, 9, 12, 13, 15)

f) Describe the working of flash memory.

5. Attempt any FOUR of the following: **16**

a) Compare TTL and CMOS w.r.t.

(i) Propagation delay

(ii) Power dissipation

(iii) Fan out

(iv) Basic gates.

b) Design 1:32 demultiplexer using 1:8 demultiplexer.

c) Draw 3 bit twisted ring counter using D flip flop. Give its timing diagram.

Marks

d) Draw circuit diagram of 4 bit R-2R ladder DAC and obtain its output voltage expression.

e) Describe the operation of 1 digit BCD adder using IC 7483.

f) Perform following BCD operations.

(i) $(48)_{10} + (34)_{10}$

(ii) $(52)_{10} - (89)_{10}$

6. Attempt any FOUR of the following: **16**

a) Realize the following functions using demultiplexers:

(i) $F_1 = \sum m\ (0, 1, 3, 7, 11, 13, 15)$

(ii) $F_2 = \sum m\ (2, 4, 8, 10, 12)$

b) Classify memories and identify the IC

(i) IC 7481

(ii) IC 6116

c) Design 3:8 line decoder and give IC number for the same.

d) Prove that

(i) $A + \overline{A}B + A\overline{B} = A + B$

(ii) $\overline{\overline{A} + \overline{B} + \overline{C}} = ABC$

e) Describe operation of SIPO shift register with circuit diagram.

f) Write any three advantages and one disadvantage of dual slope ADC.