22232

3 Hours / 70 Marks Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. Attempt any FIVE of the following : **10**

(a) Define the terms :

(i) Noise margin

(ii) Skew

(b) List the different types of modeling used in VHDL.

(c) Draw the symbol of

(i) NPN transistor

(ii) P-ch MOSFET

(d) List the sequential types of statements used in VHDL.

(e) State advantages of hardware description language over software (any two).

(f) Write the equation of channel resistance (RD).

(g) List the different types of finite state machines.

2. Attempt any THREE of the following : **12**

(a) Draw and explain architecture of CPLD.

(b) Write VHDL code for 4:1 MUX using concurrent construct.

(c) Explain the HDL design flow for synthesis process.

(d) Explain various operators used in VHDL.

3. Attempt any THREE of the following : **12**

(a) Explain :

(i) event scheduling and

(ii) zero modeling w.r.t. VHDL

(b) Write the syntax of

(i) if statement

(ii) wait statement

(c) State Pro's and Con's of VHDL.

(d) Draw state diagram to detect the sequence of '10110'.

4. Attempt any THREE of the following : **12**

(a) Compare Moore machine with Mealy machine.

(b) Write the syntax of

(i) Entity

(ii) Architecture

(c) Draw 2 i/p CMOS NAND gate and write its truth table.

(d) Explain the different delays in VHDL simulation.

(e) Draw and explain steps involved in fabrication of NMOS.

5. Attempt any TWO of the following : **12**

(a) Design Mealy sequence detector using D Flipflop to detect sequence of '110'.

(b) Explain with syntax

(i) Signal

(ii) Constant

(iii) Variables used in VHDL.

(c) Write VHDL code for 3:8 decoder using case statement.

6. Attempt any TWO of the following : **12**

(a) State applications of Test bench and write test bench for 2 input AND Gate.

(b) Implement following function using CMOS logic $Y = \overline{(A \cdot B) + (C \cdot D) + E}$.

(c) Draw ASIC design flow and explain.
