22639

21222

3 Hours / 70 Marks Seat No. | | | | | | | | |

15 minutes extra for each hour

Instructions : (1) All Questions are *compulsory.*

(2) Illustrate your answers with neat sketches wherever necessary.

(3) Figures to the right indicate full marks.

(4) Assume suitable data, if necessary.

Marks

1. Attempt any FIVE of the following : **10**

(a) Define Noise Margin and write its value for CMOS logic.

(b) List two examples of concurrent constructs.

(c) Write the function of (1) Entity and (2) Architecture.

(d) Write the meaning of following statements in typical test bench –

wait for 100 ns;

a ⇐ '1';

b ⇐ '0';

(e) Draw the diagram of Moore machine and write the o/p expression.

(f) Write the syntax of sensitivity list for AND gate with X, Y as inputs.

(g) Draw the circuit of OR gate using NMOS transistor.

2. Attempt any THREE of the following : **12**

(a) Draw the block diagram of FPGA and typical logic block.

(b) Write the VHDL code for full adder.

(c) Draw the circuit diagram of CMOS inverter and its characteristics.

(d) Explain the synthesis process in HDL design flow.

3. Attempt any THREE of the following : **12**

(a) Write the estimation process of resistance fabrication with layout diagram.

(b) Write the VHDL code for 2:1 Mux using with … select statement.

(c) Write only architecture part of VHDL code for OR gate using behavioural and Data flow modelling style.

(d) (i) Write four features of VHDL.

(ii) Write two cons of VHDL.

4. Attempt any THREE of the following : **12**

(a) Draw the state diagram of Moore and Mealy machine for detecting sequence 110.

(b) Design the CMOS circuit to implement the function, $F = A + (B \cdot C)$

(c) Explain the optimization methods for optimizing logic expression in VLSI design flow.

(d) Draw a neat diagram of ASIC design flow.

(e) Explain the working of transmission gate with circuit diagram and symbol.

5. Attempt any TWO of the following : **12**

(a) Design Moore machine for detecting sequence 1101 (Non-overlapping) using D-flip-flop.

(b) (i) Explain the steps in NMOS fabrication with diagram.

(ii) Write the advantages of twin-tub process.

(c) (i) Write the VHDL code for shift register (shift left operation).

(ii) Explain Test bench with diagram.

6. Attempt any TWO of the following : **12**

(a) (i) Compare software with hardware language (any 3 pts).

(ii) Explain the delta delay.

(b) Compare CPLD and FPGA (any six points).

(c) (i) List different data types in VHDL.

(ii) Write the syntax for signal and variable with suitable example.

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