SUMMER – 2022 EXAMINATION

Subject Name: Linear Integrated Circuit. **Subject Code:** 22423

Model Answer

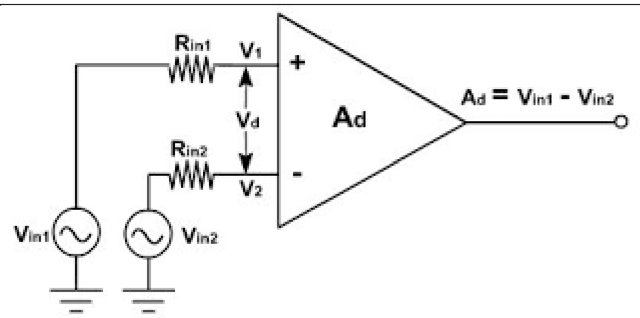
1

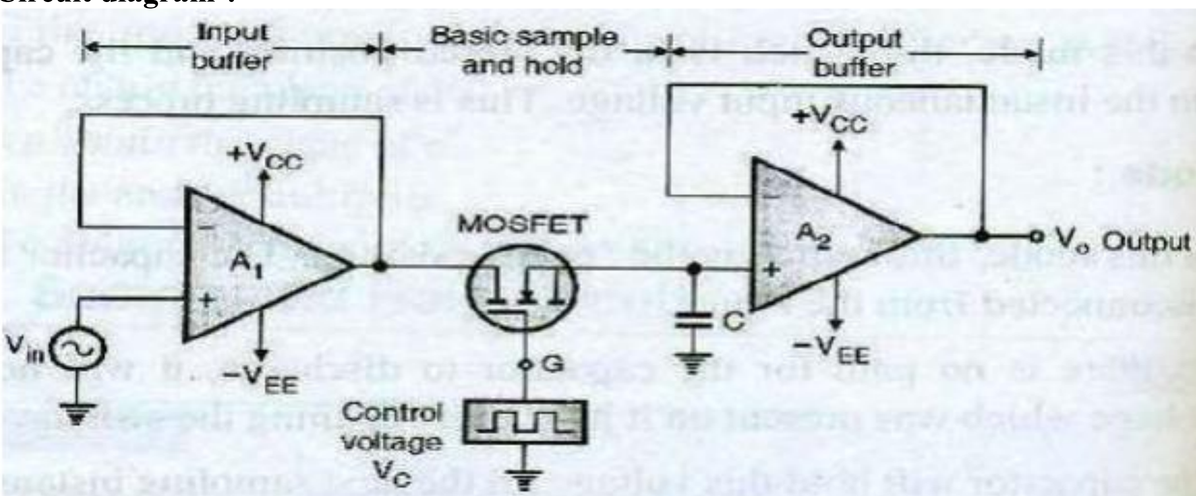
Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.
8) As per the policy decision of Maharashtra State Government, teaching in English/Marathi and Bilingual (English + Marathi) medium is introduced at first year of AICTE diploma Programme from academic year 2021-2022. Hence if the students in first year (first and second semesters) write answers in Marathi or bilingual language (English +Marathi), the Examiner shall consider the same and assess the answer based on matching of concepts with model answer.

Q. No.	Sub Q. N.	Answers	Marking Scheme
1	**(A)**	**Attempt any FIVE of the following:**	**10- Total Marks**
	(a)	**State ideal and practical value of given parameters for Op-Amp IC-741** **i) Input resistance** **ii) Slew rate**	**2M**
	Ans:	(see table below)	**1/2 M for each value**

Sr. no	Parameter	Ideal values	Typical Practical values
1	Input resistance	∞	2MΩ
2	Slew rate	∞	0.5V/µs

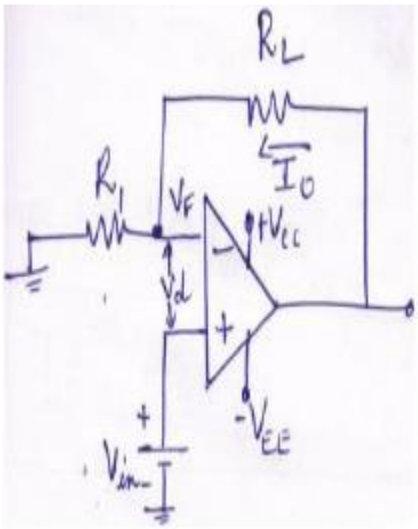
	(b)	**Sketch the circuit diagram of Op-Amp based differential amplifier in open loop mode.**	**2M**
	Ans:	 	**2 M for correct sketch**
	(c)	**List four specifications of LM 324.**	**2M**
	Ans:	• **Supply voltage =32 V.** • **Differential i/p voltage= -0.3 V to +32 V.** • **Operating temp= 00 c to +700 c** • **Input current =50mA.** • **Power dissipation = molded DIP=1130mw** • **Cavity DIP= 1260 mw**	**Any 4- (Each 1/2M)**
	(d)	**List any four merits of active filters over passive filters.**	**2M**
	Ans:	**Merits of active filters over passive filters:-** 1. Less cost due to the variety of cheaper op-amp and absence of costly inductors. 2. Gain and frequency adjustment flexibility since the op-amp is able to providing gain; the input signal is not attenuated as in case of passive filters. 3. Active filter is easier to tune or adjust as compare to passive filters. 4. No loading problem because active filter provides excellent isolation between individual stages due to high input impedance. 5. Active filters are small in size and less bulky (due to absence of "L") and rugged. 6. Non floating input and output	**Any 4 (Each 1/2 M)**

	e)	**Draw sample and hold circuit using op-amp.**	**2M**
	Ans:	**Circuit diagram-:** 	**2M for correct diagram**
	f)	**Define following terms related with phase lock loop (PLL).** **i) Lock range** **ii) Capture range**	**2M**
	Ans:	**i) Lock range**: The range of frequencies over which the PLL can maintain the phase lock with the incoming signal Fs, is defined as the lock in range. Lock range = FL = 2 Δ FL Where FL = 8 F0 / V **ii)Capture range** : It is defined as the range of frequencies over which the PLL can acquire lock with the input signal Fs Capture range = 2 Δ FC Where FC = FL/ (2π *3.6 *103 * C)	**1M** **1M**
	g)	**State the classification of filters based on frequency response.**	**2M**
	Ans:	The classification of filters based on frequency response are- i) High Pass Filter ii) Low Pass Filter iii) Band Pass Filter iv) Band Reject Filter	**1/2 mark for each type**

Q. No.	Sub Q. N.	Answers	Marking Scheme
2		**Attempt any THREE of the following:**	**12-Total Marks**
	a)	**State the difference between open loop and ciosed loop configuration of OP-AMP (any four points).**	**4M**
	Ans:	(see table below)	**1 M for each point of difference**

Sr. No.	Parameter	Open Loop Configuration	Closed loop configuration
1	Feedback	Absent	Present
2	Voltage Gain	High ideally infinite	Low
3	Gain control	Not possible	possible
4	Input Resistance	Very high	Depends on the circuit
5	Output Resistance	Low	Very low
6	Bandwidth	Low	High
7	Offset voltage	No change or Cannot Control	Can Control by adjusting feedback component
8	Application	Comparator, zero crossing detector	All application circuit such asamplifier, oscillator, filter ,adder subtracter or and so on
9	Stability	unstable	stable

Q. No.	Sub Q. N.	Answers	Marking Scheme
	b)	**Draw a circuit diagram of V-I converter of floating load . Derive expression for its output.**	**4M**

	Ans:	**Circuit Diagram:-**  The load resistor R2 is floating not connected to ground. The input voltage is applied to the non-inverting input terminal and the feedback voltage across R1 drives the inverting terminal. Writing KVL to the input loop, $V_{in} = V_{id} + V_F$ But Vid= 0 v since A is very large, $V_{in}=V_F$ Vin= R_1*I_0 I_O=Vin/R_1 Thus, Output current is proportional to input voltage. Input voltage is converted into an output current.	**2M** – Circuit diagram**,** **2M**- Derivation
	c)	**Sketch the Timer IC 555 based monostable multivibrator with suitable value of R and C for pulse width .**	

Refer Fig. No. 1 .

tp = 1 msec.

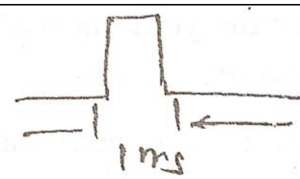


Fig. No. 1.

Ans:

Solution-The Pulse width of the output of the Monostable multivibrator is given by the formula

T_{on} =1.1 R C

C=0.1 µF

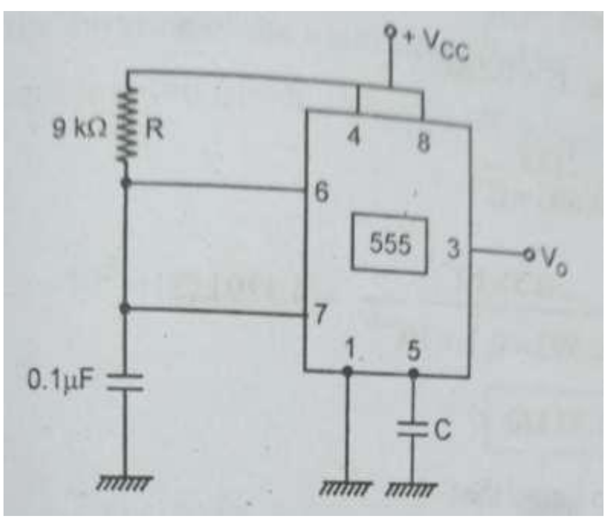
T_{on} =1 ms

$$R = \frac{1*10^{-3}\,s}{1.1*0.1*10^{-6}}$$

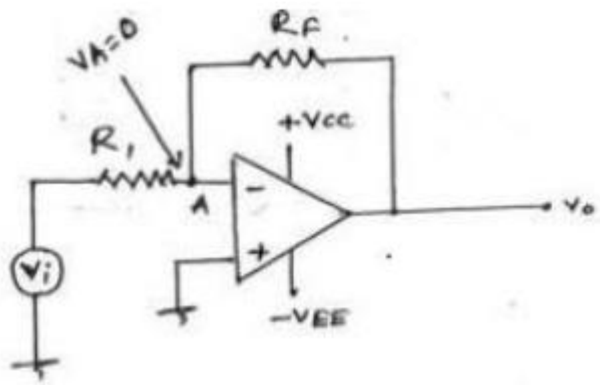
$$= \frac{10^{-3}}{1.1*10^{-7}}$$

$=0.909 \times 10^{4}\,\Omega$

=9 k Ω



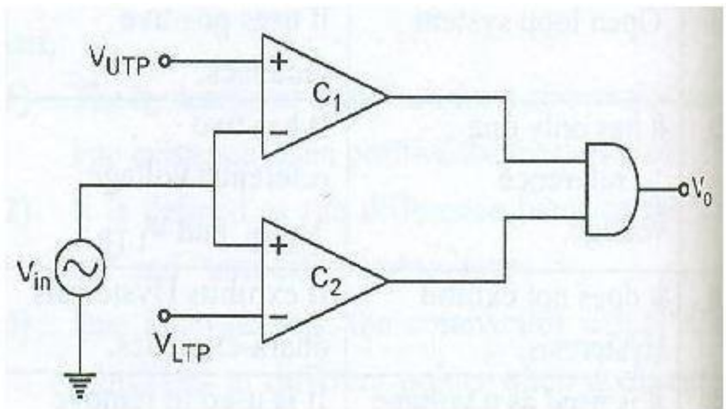
Design steps- 2 mks, diagram with proper values- 2 mks

	d)	**Explain virtual ground concept. In which basic amplifier virtual ground is present.**	**4M**
	Ans:	**Circuit diagram-:**  • In circuit point VA is virtual ground. Figure shows inverting amplifier using op-amp. • In this circuit non-inverting terminal is connected to the actual ground. • Due to this potential of inverting terminal become zero. Thus, inverting terminal is not actually connected to the ground. There after its potential is zero. • Thus point VA is known as virtual ground point. This phenomenon of having zero potential without actually grounding is known as virtual ground concept. **Virtual Ground is present in Closed Loop Inverting Amplifier Circuit.**	Circuit diagram- -1M, Explaination- 2 M, Application-1M
Q. No.	Sub Q. N.	Answers	Marking Scheme
3		**Attempt any <u>THREE</u> of the following:**	**12- Total Marks**
	a)	**If R_1= 2KΩ , R_F = 100 KΩ , V_{CC} = ± 15V and rms input voltage V_i = 20mV. Calculate the output voltage in inverting and non-inverting mode.**	**4M**
	Ans:		

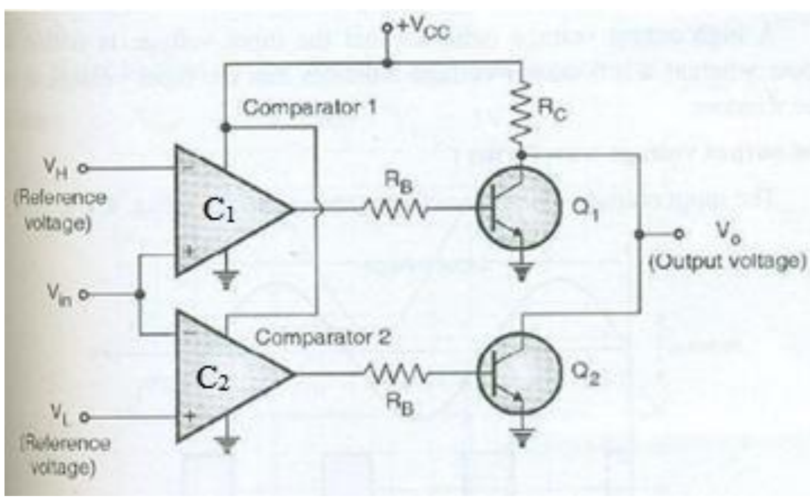
		$R_1 = 2K\Omega \quad R_f = 100K\Omega \quad V_{rms} = 20mV. \quad V_o = ?$ $V_{rms} = \frac{1}{2\sqrt{2}} V_{p-p}$ $V_{p-p} = 2 * \sqrt{2} * V_{rms}$ $= 2 * \sqrt{2} * 20 \times 10^{-3}$ $V_{p-p} = 56.56\ mV$	2M
		Inverting Mode :- $V_o = -\frac{R_f}{R_1} * V_{p-p}$ $= -\frac{100 \times 10^3}{2 \times 10^3} * 56.56\ mV$ $V_o = -2.828\ V.$	1M
		Non- Inverting Mode :- $V_o = (1 + R_f/R_1) * V_{p-p}$ $= (1 + \frac{100 \times 10^3}{2 \times 10^3}) * 56.56 \times 10^{-3}$ $V_o = 2.88456\ V$	1M

	b)	**Explain the operation of window detector with neat sketch and its input and output waveforms.**	**4M**

Ans: **Diagram:** **2M**



OR

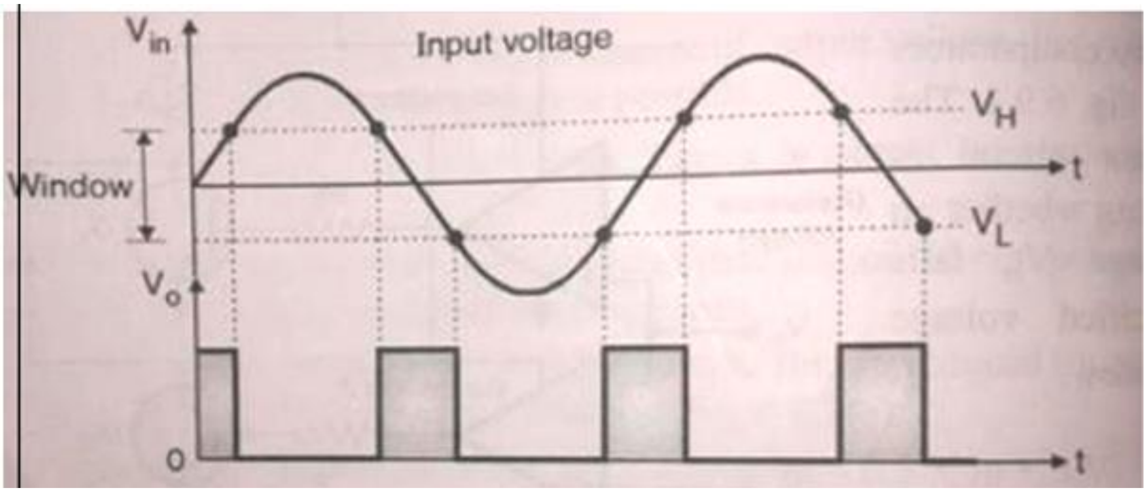
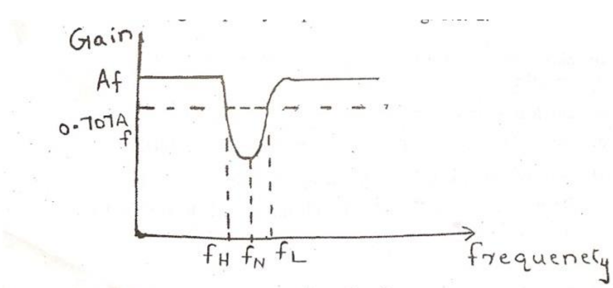


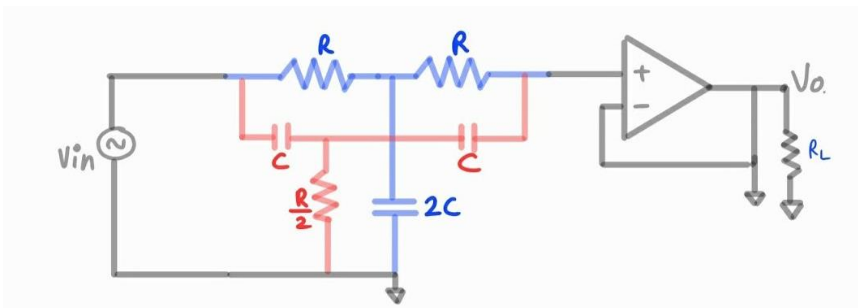
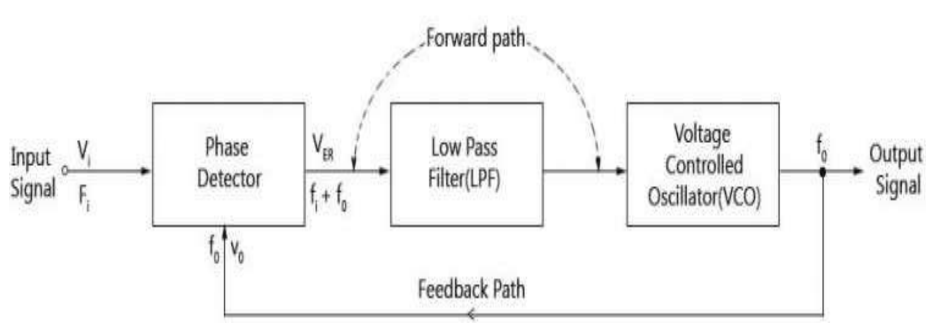
WORKING:

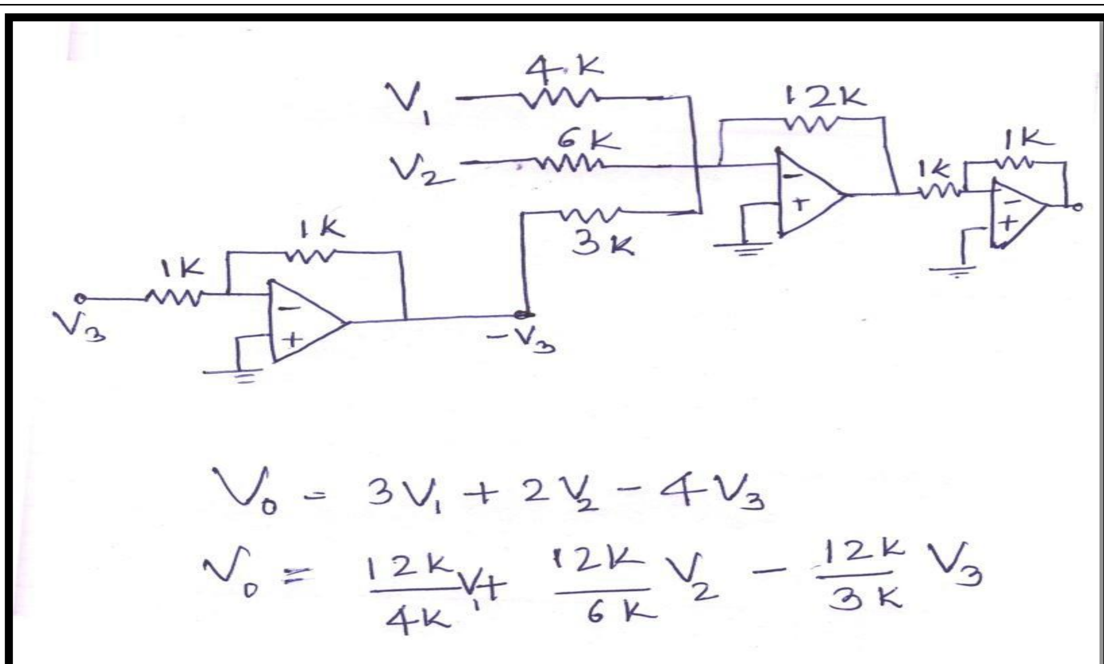
Window detector uses two comparators C_1 and C_2. The reference voltage of inverting comparator C_1 is V_{UTP} and the reference voltage of the non inverting comparator C_2 is V_{LTP}.Assume $V_{LTP} < V_{UTP}$. **1M**

: When Vin < V_{LTP} (V_L)then the differential voltage of C_2 is negative. Hence outputofC_2 is low. Vin is also less than V_{UTP}. Hence output of C_1 is high and output Vo of gate is low.

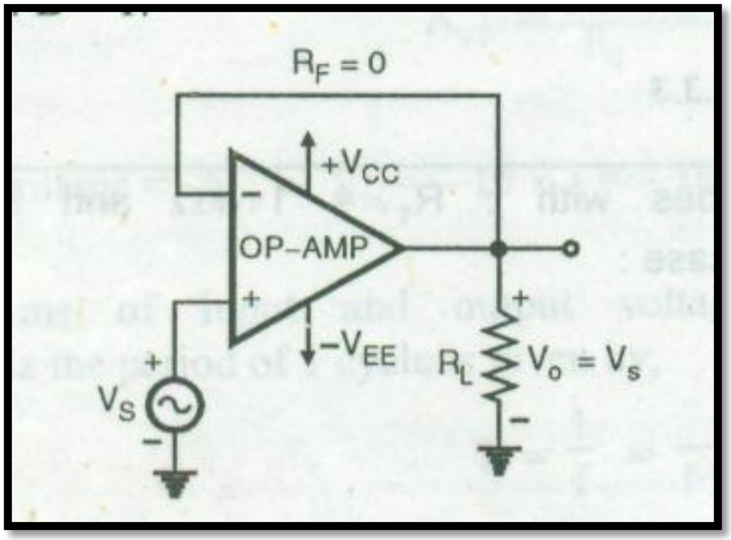
I: When Vin > V_{UTP}(V_H), then the differential input voltage of C_2 is high. The differential

		input voltage of C_1 is negative. The differential input voltage of C_1 is negative. output of C_1 is low and output Vo of AND gate is low. **II**: When V_{LTP}< Vin< V_{UTP}, OR V_L< Vin< V_H the differential input voltage of C_1 and $C_2$is positive and output is high. The output of AND gate is high. **WAVEFORMS:** 	**1M**
	c)	**Identify and draw the Op-Amp based filter circuit to fulfill following frequency response. Refer Fig. No.2.**  Fig. No. 2.	**4M**

	Ans:	**IDENTIFICATION:** This is a frequency response of **NARROW BAND REJECT FILTER (NBRF) /NOTCH FILTER.** **CIRCUIT DIAGRAM:**  	2M 2M
	d)	**Draw the block diagram of PLL and state the function of each block.**	4M
	Ans:	**Diagram:**  PLL is Phase locked loop is basic closed loop system used for different frequency and phase control application. It consists of Phase detector, Low Pass filter and Voltage controlled oscillator circuits. **Phase Detector:** The input signal „Vi" with an input frequency „Fi" is conceded by a phase detector. Basically the phase detector is a comparator that compares the input frequency fi through the feedback frequency fo. The output of the phase detector is (fi+fo) which is a DC voltage. **Low Pass Filter:** The out of the phase detector, i.e., DC voltage is input to the low pass filter (LPF); it removes the high-frequency noise and produces a steady DC level, i.e., Fi-Fo. The Vf is also a dynamic characteristic of the PLL **VCO:**	2M 2M

		The output of the low pass filter, i.e., DC level is passed on to the VCO. The input signal is directly proportional to the output frequency of the VCO (fo). The input and output frequencies are compared and adjusted through the feedback loop until the output frequency is equal to the input frequency. Hence, the PLL works like free running, capture, and phase lock.	
Q. No.	Sub Q. N.	Answers	Marking Scheme
4		**Attempt any THREE of the following:**	**12- Total Marks**
	(a)	**Draw the circuit diagram to generate the following output using op-amps.** **$V_O = 3V_1 + 2V_2 - 4V_3$: V_1, V_2, V_3 are input voltages.**	**4M**
	Ans:		**Correct diagram 4 mks**
	(b)	**Define the following parameters of op-amp** **i) Input bias current** **ii) Input offset current**	**4M**

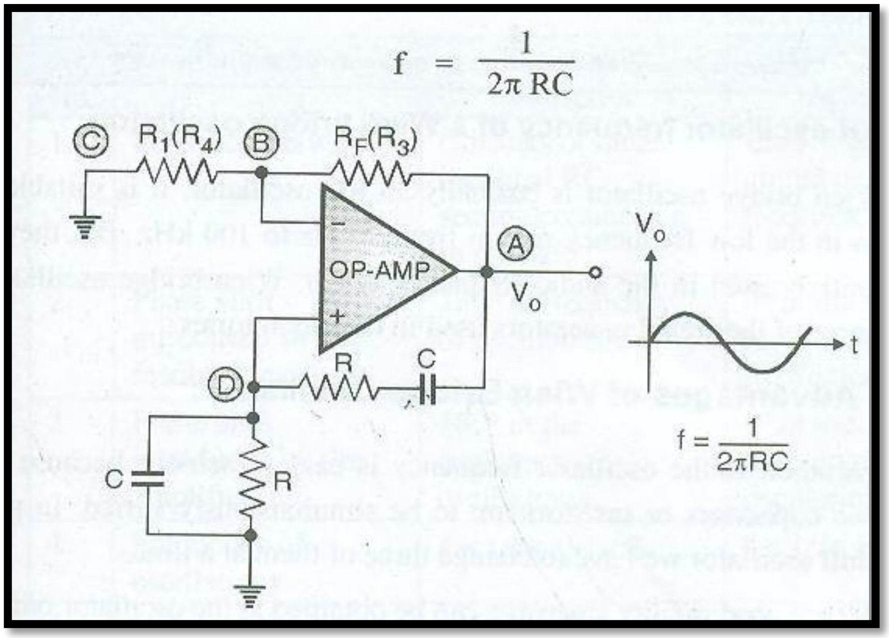
		iii) Slew rate **iv) CMRR**	
	Ans:	**i) Input bias current-** An input bias current IB is defined as the average of the two input bias current, IB1 & IB2, IB= (IB1 + IB2)/2 Where IB1= dc bias current flowing into the non - inverting input IB2= dc bias current flowing into the inverting input **ii) Input offset current-** The input offset current Iio is defined as the algebraic difference between two input bias currents IB1 & IB2. Iio =| IB1 - IB2| **iii) Slew rate-** It is defined as the maximum rate of change of output voltage per unit time. S.R .= ΔVo /Δ t , Unit- V/µs. **iv) CMRR- It defined as the ratio of differential gain to the common mode gain. It is the ability of an amplifier to reject the common mode signal such as noise. Expressed in dB.**	**Each correct definition -1 mks**
	(c)	**Sketch the diagram of voltage follower. Why it is called voltage follower. State its one application.**	**4M**
	Ans:	Circuit diagram of voltage follower-	Diagram:2 mks; Voltage follower: 1mks ; Application(any one) : 1mks

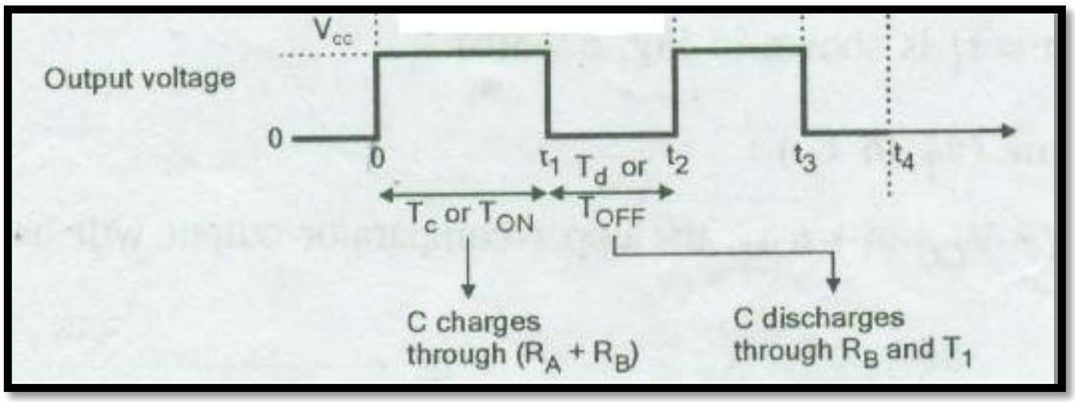


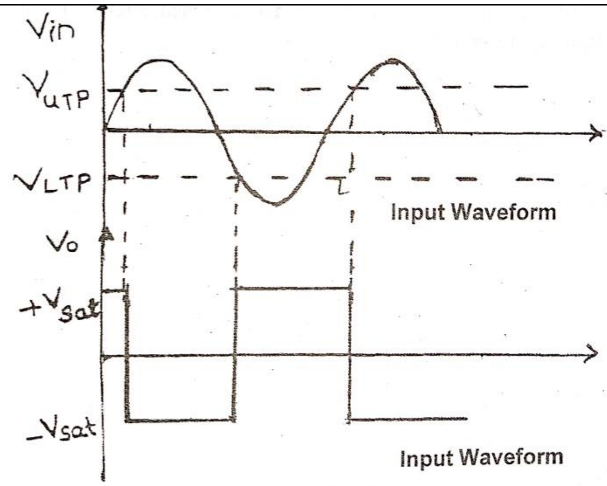
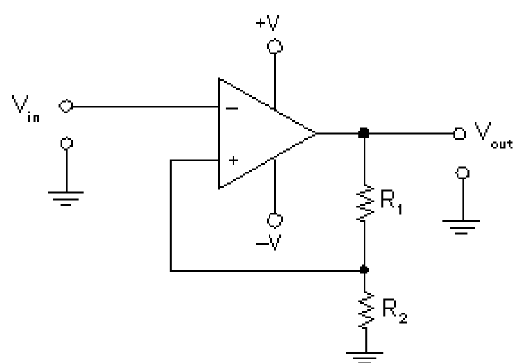
When R1= ∞ and RF= 0 the non-inverting amplifier gets converted into a voltage follower or unity gain amplifier.
When the non- inverting amplifier is configured so as to obtain a gain of 1, it is called as voltage follower or unity gain non- inverting buffer.

Applications: (Any one)
1. As a buffer amplifier so as to avoid the loading of the source.
2. As the output stage.
3. For impedance matching.

(d)	**Sketch the op-amp based Wein Bridge Oscillator for frequency = 1KHz**	**4M**
Ans:	**Given- Frequency of oscillation F=1KHz** **F=1/2π RC** **Let C=0.1 μ F** **$1 *10^3 = 1/(2 \pi R* 0.1 *10^{-6})$** **R=1592 Ω = 1.59 KΩ** **Let** **R1=RF=10 KΩ**	**1mks** **1 mks**

			**2mks** **OR** **As the question is sketch….** **4 mks for circuit with proper values can be given.**
	(e)	**For IC 555 configured as astable multivibrator $R_1 = 5.6k\Omega$, $R_2 = 2.7\ k\Omega$ and C= 0.1 µF. Find the frequency of oscillation and duty cycle. Sketch its output waveforms..**	**4M**
	Ans:	Given: R1= 5.6 KΩ , R2= 2.7 KΩ and C= 0.1 µ F Solution: The time period of one cycle of the output voltage waveform is given by, T= Ton + Toff = 0.693 (R1 + 2R2) C $= 0.693\ [5.6 \times 10^3 + 2x\ (2.78 \times 10^3)] \times 0.1 \times 10^{-6}$ $= 7.73 \times 10^{-4}$ T= 0.773 m sec **(1M)** Therefore, Hence the frequency of oscillations is given by, F= 1/T F= 1/ 0.773 x 10-3 F = 1.293 KHz **(1M)** Duty cycle (D) = R1 + R2 / R1 + 2R2 $= (5.6 \times 10^3) + (2.7 \times 10^3) / (5.6 \times 10^3) + 2(2.7 \times 10^3)$ = 8300/ 11000 = 0.7545 Therefore, % D = 75.45 % **(1M)**	

		Output waveform- $R_1=R_A$, $R_2=R_B$  (1 M)	
Q. No.	Sub Q. N.	Answers	Marking Scheme
5.		**Attempt any TWO of the following:**	**12- Total Marks**
	a)	**Identify waveforms shown in Figure No. 3. Name the circuit to obtain the above waveform. Sketch the circuit diagram for it.**	**6M**

		 Fig. No. 3	
	Ans:	**Identification:** The circuit which provides given Waveforms is **Schmitt Trigger using Op-amp.** **Circuit Diagram:**  	**3M** **3M**
	b)	**Design a bandpass filter for $F_{L} =$ 100 Hz, F_H = 1KH and passband gain = 4**	**6M**
	Ans:		

Q.5 (b) $f_L = 100\,Hz$ $f_H = 1\,KHz$ Gain = 4

Assume ⇒ $C_1 = C_2 = C = 0.01\mu F$

* Design High pass filter

$f_L = \frac{1}{2\pi R.C}$

$R = \frac{1}{2\pi f_L C}$

$= \frac{1}{2\pi \times 100 \times 0.01 \times 10^{-6}}$

$R = 159.15\ K\Omega$

* Design Low pass filter

$f_H = \frac{1}{2\pi R C}$

$R = \frac{1}{2\pi f_H C}$

$= \frac{1}{2\times\pi \times 1\times10^3 \times 0.01\times10^{-6}}$

$R = 15.91\ K\Omega$

2M

$A_{Total} = A_H * A_L = 4$

$2 * 2 = 4$

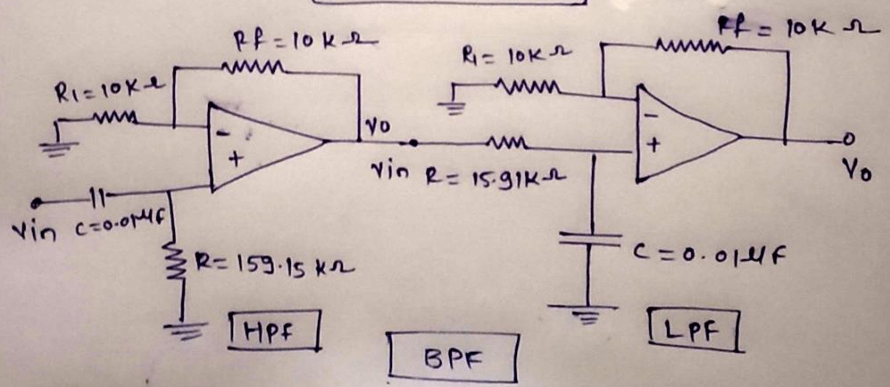
$A_H = A_L = \left(1 + \frac{R_f}{R_1}\right)$

$2 = (1 + R_f/R_1)$

$1 = R_f/R_1 \quad \therefore R_f = R_1$

Let $R_f = R_1 = 10\,K\Omega$

2M



2M

c)	**Sketch output signal along with input signal as sine wave of 2v peak to peak for following Op-Amp based circuits with ideal conditions.**	**6M**

<table>
<tr><td></td><td></td><td>

i) **Inverting amplifier with gain 5**
ii) **Positive peak detector**
iii) **Active integrator**
iv) **Non-inverting zero crossing detector**
v) **Non-inverting unity gain amplifier**
vi) **Active differentiator**

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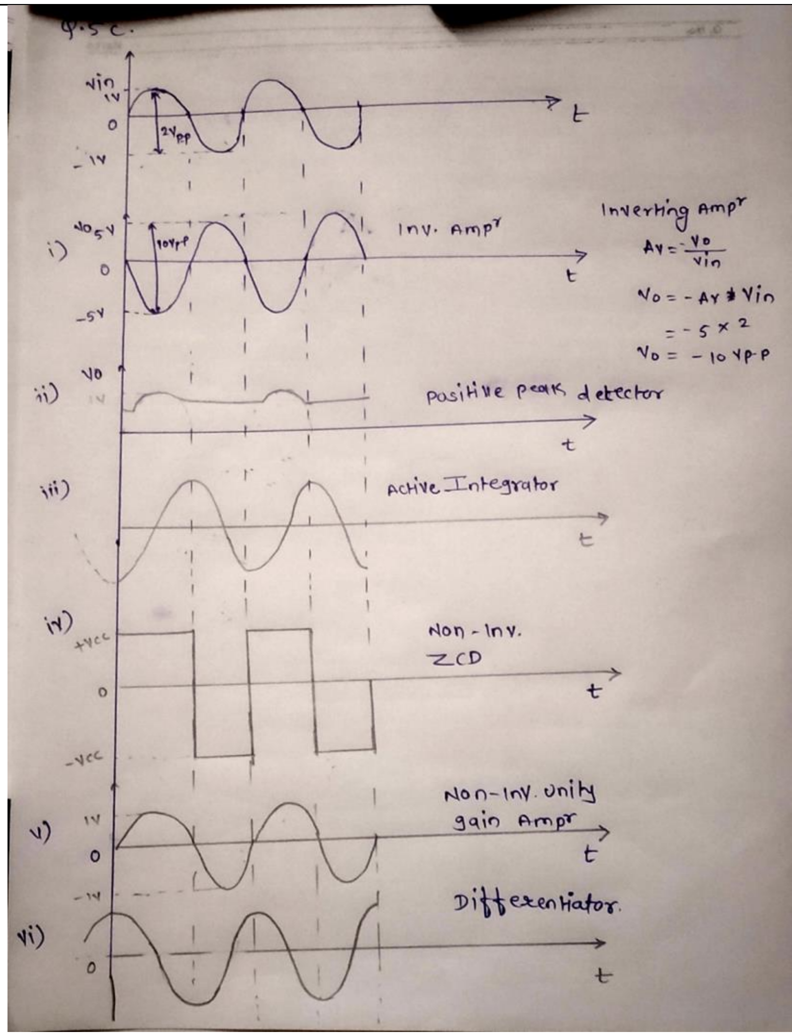
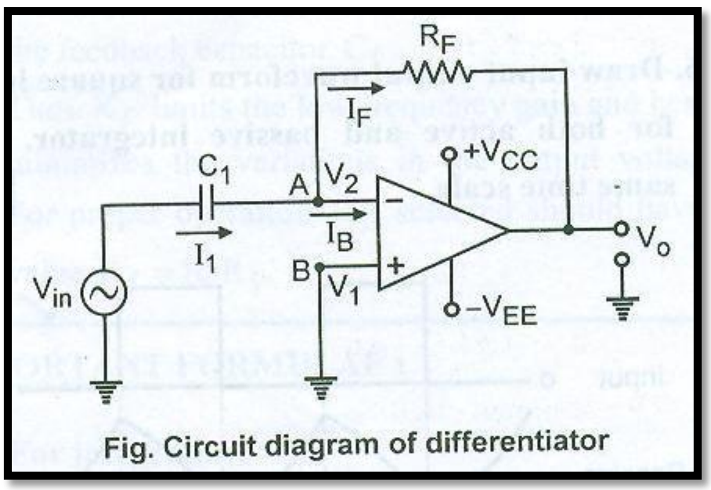
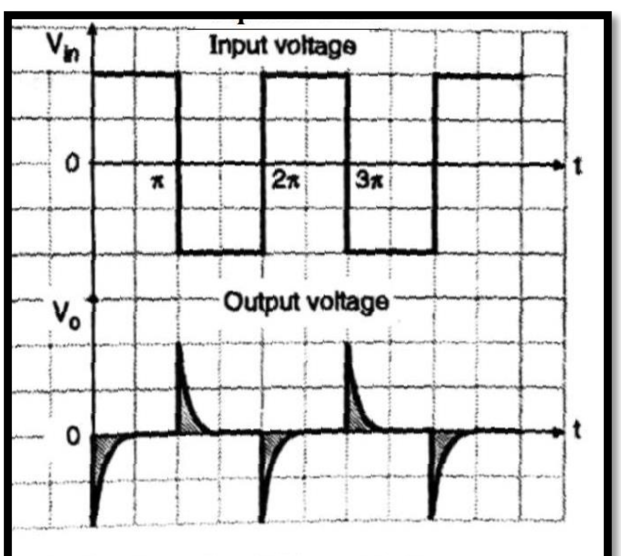
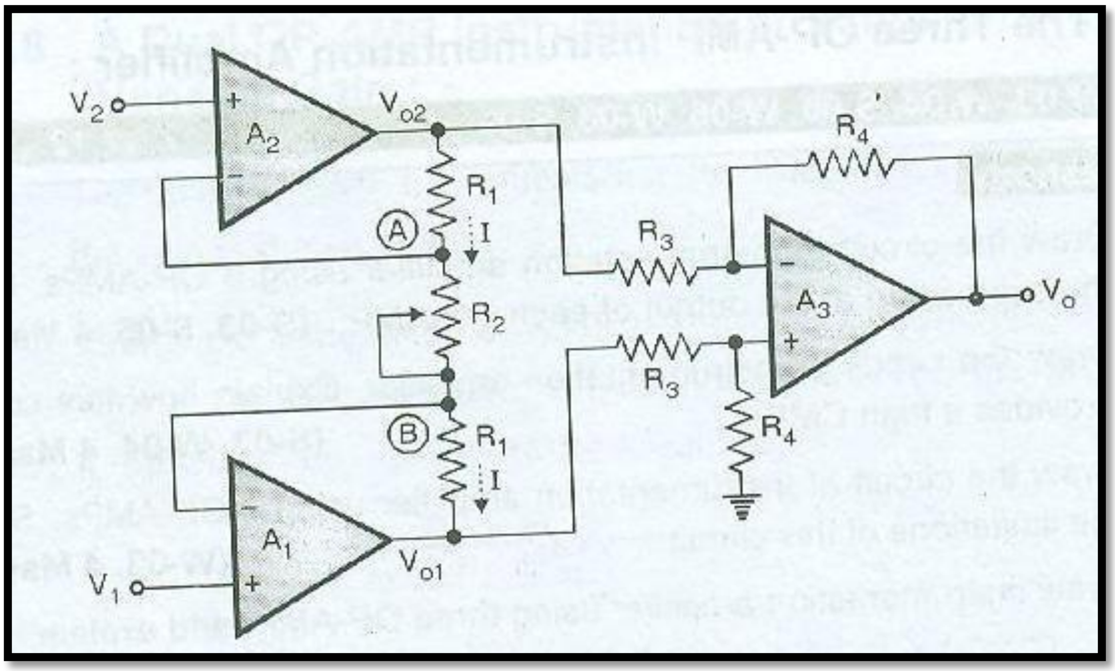
<tr><td></td><td>**Ans:**</td><td>

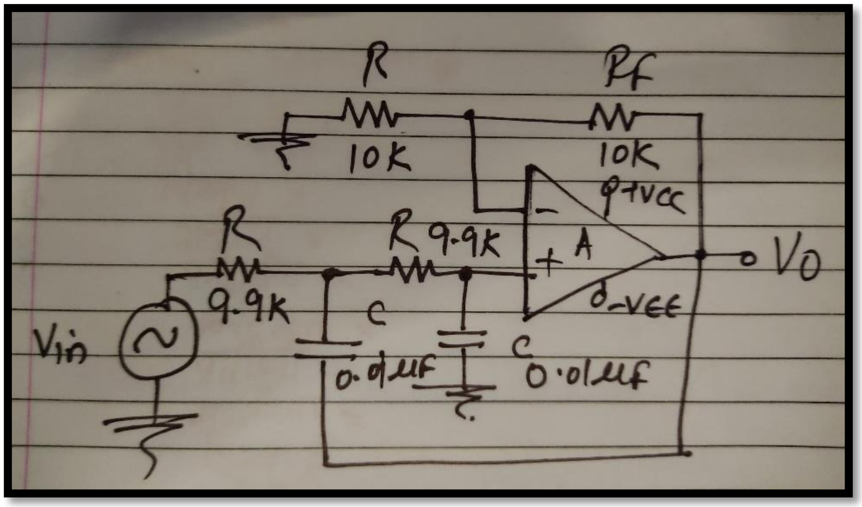


</td><td>**1M FOR EACH W/F**</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>Q. No.</td><td>Sub Q. N.</td><td>Answers</td><td>Marking Scheme</td></tr>
</table>

6.		**Attempt any <u>TWO</u> of the following :**	**12- Total Marks**
	a)	**For the given equation Sketch the circuit diagram and output waveforms for square wave input.** $V_O = -R_F C_1 \frac{d(Vin)}{dt}$	**6M**
	Ans:	**The given equation is the output equation of a differentiator circuit-**  Fig. Circuit diagram of differentiator **Output waveforms for square wave input-**  	**Correct sketch 3 mks, input and output waveforms-3 mks**

	b)	**Explain the operation of instrumentation amplifier using three op-amps with neat sketch.**	**6M**
	Ans:	**Circuit diagram-**  **Operation-**The high impedance instrumentation amplifier using cross coupled difference amplifiers is as shown in figure . A1 and A2 in Fig are basically non inverting amplifiers with their inverting (-) terminal connected to resistors R2 instead of connecting it to ground. As the input impedance of all OP- AMPs used in assumed to be infinite their input current is zero. Therefore current flowing through the resistors R1, R2 and R3 is same i.e .I and the output is given as- **Vo=(1+2R1/R2)R4/R3*(V1-V2)** **Vo/(V1-V2)=Av=(1+2R1/R2)*R4/R3** The overall gain of Av of the three Op-Amp instrumentation amplifier is given by Av = Av1 x Av2 Hence by using a variable resistor R2 the overall gain can be easily and linearly varied. The output is then given by ,Vo = Av x (V1 – V2)	**Circuit diagram - 3 mks, operation – 2 mks, o/p equation – 1mks**
	c)	**Design a second order low pass butter worth filter with a cut-off frequency 1.6KHz .**	**6M**

		sketch the designed circuit and its frequency response	
	Ans:	**Given:- Cut off frequency Fc = 1.6 Khz** **Let Passband gain Af = 2** Pass band Gain (A_f) is given by the formula $A_f = 1 + \frac{R_f}{R_1}$ Here, $A_f = 2$ Therefore, $2 = 1 + \frac{R_f}{R_1}$ So, $1 = \frac{R_f}{R_1}$ Therefore, $R_f = R_1$ Let $R_f = 10k\Omega$ Therefore, $R_1 = 10k\Omega$ Assume C = 0.01uF But $f_c = \frac{1}{2\pi RC}$ **Given- Fc=1.6 Khz = 1600 Hz** **1600=1/(2* π *R*0.01*10-6)** **R= 9992 Ω =9.992 KΩ (or 10 KΩ)** **The designed circuit is-**	**Correct numerical values -2 mks, circuit diagram with component values -2 mks, correct frequency response -2 mks**



Frequency Response-