DIGITAL SYSTEM DESIGN **Course Code : 316339**

Programme Name/s : **Digital Electronics**
Programme Code : **DE**
Semester : **Sixth**
Course Title : **DIGITAL SYSTEM DESIGN**
Course Code : **316339**

I. RATIONALE

Digitization signifies the use of digital circuits and systems in the Automation and Industrial applications world of work. The Digital System Design course equips students with the essential skills to design, optimize digital circuits and troubleshoot digital circuits and systems.

II. INDUSTRY / EMPLOYER EXPECTED OUTCOME

The aim of this course is to help students to attain the following industry/employer expected outcome through various teaching learning experiences:
" Apply digital system design concepts to address the real-world problems."

III. COURSE LEVEL LEARNING OUTCOMES (COS)

Students will be able to achieve & demonstrate the following COs on completion of course based learning

- CO1 - Design combinational logic circuits for given applications using Map Entered Variable (MEV) Method.
- CO2 - Develop sequential circuits based on Algorithm State Machine (ASM) chart.
- CO3 - Implement various asynchronous sequential circuits.
- CO4 - Use PLDs to implement combinational circuits.
- CO5 - Develop VHDL code for the given application.

IV. TEACHING-LEARNING & ASSESSMENT SCHEME

Course Code	Course Title	Abbr	Course Category/s	Learning Scheme					Credits	Assessment Scheme											
				Actual Contact Hrs./Week			SLH	NLH		Paper Duration	Theory				Based on LL & TL				Based on SL		Total Marks
															Practical						
				CL	TL	LL					FA-TH	SA-TH	Total		FA-PR		SA-PR		SLA		
											Max	Max	Max	Min	Max	Min	Max	Min	Max	Min	
316339	DIGITAL SYSTEM DESIGN	DSD	DSE	4	-	2	2	8	4	3	30	70	100	40	25	10	25#	10	25	10	175

Total IKS Hrs for Sem. : 0 Hrs
Abbreviations: CL- ClassRoom Learning , TL- Tutorial Learning, LL-Laboratory Learning, SLH-Self Learning Hours, NLH-Notional Learning Hours, FA - Formative Assessment, SA -Summative assessment, IKS - Indian Knowledge System, SLA - Self Learning Assessment
Legends: @ Internal Assessment, # External Assessment, *# On Line Examination , @$ Internal Online Examination
Note :

1. FA-TH represents average of two class tests of 30 marks each conducted during the semester.
2. If candidate is not securing minimum passing marks in FA-PR of any course then the candidate shall be declared as "Detained" in that semester.
3. If candidate is not securing minimum passing marks in SLA of any course then the candidate shall be declared as fail and will have to repeat and resubmit SLA work.
4. Notional Learning hours for the semester are (CL+LL+TL+SL)hrs.* 15 Weeks
5. 1 credit is equivalent to 30 Notional hrs.
6. * Self learning hours shall not be reflected in the Time Table.
7. * Self learning includes micro project / assignment / other activities.

V. THEORY LEARNING OUTCOMES AND ALIGNED COURSE CONTENT

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Sr.No	Theory Learning Outcomes (TLO's)aligned to CO's.	Learning content mapped with Theory Learning Outcomes (TLO's) and CO's.	Suggested Learning Pedagogies.
1	TLO 1.1 Develop logic circuits in standard SOP/POS form for the given logical expression. TLO 1.2 Minimize the given logical expression using given minimization method. TLO 1.3 Realize the given type of parity generating circuit using IC 74180. TLO 1.4 Simplify logic functions with MSI circuits. TLO 1.5 Describe static and dynamic hazards of combinational circuits with examples.	**Unit - I Combinational Logic Circuit Design** 1.1 Sum of Product (SOP) and Product of Sum (POS)- min term and max term 1.2 K -map for 5 & 6 variables, Quine Mc Cluskey method, Map Entered Variable method 1.3 Combinational logic circuits : Standard logic functions with MSI circuits (Multiplexers and De-multiplexers, Encoders and Decoders) and design problems 1.4 Odd/Even parity generator using IC 74180 1.5 Comparators using IC 7485 for one, two and three bits 1.6 Static and Dynamic hazards in combinational logic circuits	Presentations Lecture Using Chalk-Board Video Demonstrations
2	TLO 2.1 Prepare the equivalent state diagram of the given ASM chart. TLO 2.2 Design the controller with D flip flop and gates of the given ASM chart. TLO 2.3 Derive the state diagram of the n bit serial binary adder. TLO 2.4 Design ASM chart of given counter.	**Unit - II Sequential Logic Circuit Design** 2.1 Finite State Machine (FSM) models- Mealy, Moore : block diagram, advantages, disadvantages, applications 2.2 State table, state diagram and state reduction of Sequential circuits 2.3 State diagram of serial binary adder, two bit up/ down counter, sequence generator 2.4 Algorithmic State Machines (ASM): Introduction, working, flowchart, state transition, applications (such as controller, counter)	Video Demonstrations Hands-on Presentations
3	TLO 3.1 Describe with a block diagram working of the given asynchronous sequential circuit. TLO 3.2 Use excitation table of a given flip flop to design specific type of counter. TLO 3.3 Explain the concepts of cycles, races, hazards and delays. TLO 3.4 Implement hazard free circuit for given logic function.	**Unit - III Asynchronous Sequential Circuits** 3.1 Asynchronous sequential circuits- Block diagram, advantages and disadvantages, applications 3.2 Realization of asynchronous sequential circuits- up counter, down counter, up-down counter(3 bit and 4 bit), mod n counter using T/JK flip-flops 3.3 Conversion of flip- flops 3.4 Cycles, races, delays and hazards in sequential circuits 3.5 Static, dynamic and essential hazards, elimination	Presentations Video Demonstrations Lecture Using Chalk-Board
4	TLO 4.1 Classify Programmable Logic Devices. TLO 4.2 Design the combinational circuit for the given function. TLO 4.3 Design the given function using PLA. TLO 4.4 Design the given function using PAL. TLO 4.5 Compare CPLD and FPGA systems.	**Unit - IV Programmable Logic Devices** 4.1 Programmable logic devices(PAL, PLA, CPLD, FPGA): Introduction, classification, advantages and applications 4.2 Design of the given function using ROM: 3 bit binary to gray code converter, gray to binary code converter, Full adder, advantages and disadvantages of ROM as PLD 4.3 Programming Logic Array PLA: block diagram, implementation of combinational circuit using PLA for the given Boolean function(maximum 3 input, 4 product term and 2 outputs) 4.4 Programming Array Logic PAL: block diagram, implementation of combinational circuit using PAL for	Video Demonstrations Presentations Lecture Using Chalk-Board Hands-on

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Sr.No	Theory Learning Outcomes (TLO's)aligned to CO's.	Learning content mapped with Theory Learning Outcomes (TLO's) and CO's.	Suggested Learning Pedagogies.
		the given Boolean function (max 4 inputs, 3 product terms and 4 outputs) 4.5 Complex Programmable Logic Device(CPLD) : Block diagram , XC 9500 CPLD family and features, Field Programmable Gate Array (FPGA): Block diagram, Xilinx XC 4000 FPGA family and features, compare CPLD and FPGA	
5	TLO 5.1 Describe the hardware descriptive language, its components programming syntax. TLO 5.2 Describe the VHDL programming format . TLO 5.3 List the architecture modelling styles in VHDL. TLO 5.4 Design the combinational and sequential circuit using VHDL. TLO 5.5 Compare the different VHDL modelling styles.	**Unit - V Introduction to VHDL and it's Programming** 5.1 HDL: Introduction, components, features and advantages, VHDL: Introduction and features 5.2 VHDL Modelling : Behavioral, dataflow and structural modelling styles 5.3 VHDL code for combinational circuits : Gates, half adder/subtractor, 2:4 decoder 5.4 VHDL code for sequential circuits : D flipflop, T flipflop, 3 bit asynchronous counter, 3 bit serial in serial out(SISO) shift register 5.5 Compare various VHDL modelling styles, introduction to VHDL statements - concurrent and sequential statements	Lecture using Chalk-Board Video Demonstrations Presentations Hands-on

VI. LABORATORY LEARNING OUTCOME AND ALIGNED PRACTICAL / TUTORIAL EXPERIENCES.

Practical / Tutorial / Laboratory Learning Outcome (LLO)	Sr No	Laboratory Experiment / Practical Titles / Tutorial Titles	Number of hrs.	Relevant COs
LLO 1.1 Test the logic circuit in standard SOP/POS form for the given logical expression.	1	Testing of given SOP/POS expression	2	CO1
LLO 2.1 Build and test the even/odd parity generating circuit using IC 74180.	2	*Implementation of 4-bit even /odd parity generator using IC 74180	2	CO1
LLO 3.1 Build and verify the n-bit comparator circuit using IC 7485.	3	*Implementation of 3-bit binary comparator circuit	2	CO1
LLO 4.1 To implement and test the 4 variable Boolean function using multiplexer IC 74151.	4	Implementation of the given 4 variable function using multiplexer IC 74151	2	CO1
LLO 5.1 Build and test the 8-bit binary adder using IC 7483.	5	Implementation of the 8-bit binary adder using IC 7483	2	CO2
LLO 6.1 Build and test a sequence generator circuit for the given sequence.	6	*Implementation of a sequence generator circuit for the given sequence	2	CO2
LLO 7.1 Develop and simulate a controller circuit of the given function using suitable software.	7	* Simulation of a controller circuit for the given function	2	CO2
LLO 8.1 Design and test a 4 bit asynchronous counter using IC 74163.	8	Implementation of a 4-bit asynchronous counter using IC 74163.	2	CO3
LLO 9.1 Develop and simulate a 3 or 4-bit asynchronous counter using simulation software .	9	*Simulation of 3-bit or 4-bit asynchronous counter using simulation software(proeteus/Pspice)	2	CO3
LLO 10.1 Build and test the conversion of JK flipflop to D flipflop .	10	Realization of D flipflop using JK flipflop	2	CO3
LLO 11.1 Develop and simulate full adder circuit using PLA.	11	*Simulation of full adder circuit using PLA	2	CO4
LLO 12.1 Develop and simulate the given Boolean function using PAL.	12	Simulation of the given Boolean function using PAL	2	CO4

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Practical / Tutorial / Laboratory Learning Outcome (LLO)	Sr No	Laboratory Experiment / Practical Titles / Tutorial Titles	Number of hrs.	Relevant COs
LLO 13.1 Build and test D flipflop using sequential logic PLA.	13	Implementation of the D flipflop using sequential logic PLA	2	CO4
LLO 14.1 Test the VHDL code for the given n-bit parity generator using suitable simulator (Xilinx).	14	*Implementation of VHDL code for the given n-bit parity generator	2	CO5
LLO 15.1 Test the VHDL code for a 4-bit shift register using suitable simulator (Xilinx).	15	Implementation of VHDL code for a 4-bit shift register	2	CO5
LLO 16.1 Test the VHDL code for 2:4 decoder using suitable simulator (Xilinx).	16	* Testing the VHDL code for 2:4 decoder	2	CO5

Note : Out of above suggestive LLOs -

- '*' Marked Practicals (LLOs) Are mandatory.
- Minimum 80% of above list of lab experiment are to be performed.
- Judicial mix of LLOs are to be performed to achieve desired outcomes.

VII. SUGGESTED MICRO PROJECT / ASSIGNMENT/ ACTIVITIES FOR SPECIFIC LEARNING / SKILLS DEVELOPMENT (SELF LEARNING)

Micro project

- Develop and build a 3 bit comparator circuit using IC 7485 on general purpose PCB.
- Develop and test a sequence generator for the given sequence(1001001) on PCB and test the LED outputs.
- Build and test a 3 bit asynchronous up-counter using T flipflop on breadboard.
- Simulate the 4 bit even parity generator circuit.
- Build a code converter circuit and test its outputs for its given inputs (4 bit Gray to Binary code converter) using suitable simulator.
- Develop a circuit for 4 bit SISO register using suitable simulator.

Develop a circuit for 4 bit up-down counter using suitable simulator.

Assignment

- Solve the given function using Quine Mc Clusky method and implement using minimum gates- Y(A,B,C,D)= ∑m(0,1,2,3,5,7,8,9,11,14).
- Simplify the given expression using the MEV Kmap technique- Y=F(A,B,C,D) = ∑m(0,1,4,5,6,7,11,15).
- Design a sequence generator for the sequence 10110…. and draw the timing diagram.
- Design a 4 bit up-down counter using T flipflop and represent the output with timing diagram.
- Design a full subtractor circuit using Kmap and implement using PLA .
- Implement the given combinational circuit using PLA- F1(A,B,C)=∑m(4,5,7) F2(A,B,C)=∑m(3,5,7)
- Implement the given Boolean function using PAL- F1(A,B,C,D)=∑m(1,3,4,6,9,11,12,14)
  F2(A,B,C,D)=∑m(1,3,4,6,9,11,12,14,15)
  F3(A,B,C,D)=∑m(0,2,4,6,8,12)
  F4(A,B,C,D)=∑m(2,3,8,9,12,13)

Expert Session

- Expert lecture on VLSI and Embedded system design.

Visit

- Visit to Embedded system design company.

Note :

- Above is just a suggestive list of microprojects and assignments; faculty must prepare their own bank of

microprojects, assignments, and activities in a similar way.

- The faculty must allocate judicial mix of tasks, considering the weaknesses and / strengths of the student in acquiring the desired skills.
- If a microproject is assigned, it is expected to be completed as a group activity.
- SLA marks shall be awarded as per the continuous assessment record.
- For courses with no SLA component the list of suggestive microprojects / assignments/ activities are optional, faculty may encourage students to perform these tasks for enhanced learning experiences.
- If the course does not have associated SLA component, above suggestive listings is applicable to Tutorials and maybe considered for FA-PR evaluations.

VIII. LABORATORY EQUIPMENT / INSTRUMENTS / TOOLS / SOFTWARE REQUIRED

Sr.No	Equipment Name with Broad Specifications	Relevant LLO Number
1	Digital Multimeter : 3 and 1/2 digit with component measurement.	1,2,3,4,5,6,8,10
2	Breadboard development system: With DC power :5V,+/- 12 V and 0-5V variable, digital voltmeter ,ammeter, LED indicators 8 no., logic inputs input switches 8 no., clock generator, manual pulser, Breadboard with about 1600 points, potentiometer, relays etc.	1,2,3,4,5,6,8,10
3	Digital IC tester : Tests a wide range of Analog and Digital ICs such as TTL ICs 74 series, CMOS ICs 40 series.	1,2,3,4,5,6,8,10
4	Trainer kit for digital ICs : Consisting of logic gates , 7 segment decoder ICs (7447/7448), D type latch -IC 7475, Decoder IC (74154/74155) ,Multiplexer IC 74153, flipflops, shift registers ,counters along with toggle switches for inputs and seven segment displays at the outputs, built in power supply.	1,2,3,4,5,6,8,10
5	Pulse Generator:TTL pulse generator.	6,8,10
6	CRO: Dual Channel ,4 Trace/TFT based ,bandwidth 20 Mhz/30 Mhz X10 magnification 20 ns max sweep rate, Alternate triggering component tester and with optional feature of digital read out.	6,8,10
7	Xilinx, PSpice or equivalent EDA tool.	7,9,11,12,13,14,15,16

IX. SUGGESTED WEIGHTAGE TO LEARNING EFFORTS & ASSESSMENT PURPOSE (Specification Table)

Sr.No	Unit	Unit Title	Aligned COs	Learning Hours	R-Level	U-Level	A-Level	Total Marks
1	I	Combinational Logic Circuit Design	CO1	12	2	4	4	10
2	II	Sequential Logic Circuit Design	CO2	10	2	4	4	10
3	III	Asynchronous Sequential Circuits	CO3	10	4	4	4	12
4	IV	Programmable Logic Devices	CO4	14	6	6	8	20
5	V	Introduction to VHDL and it's Programming	CO5	14	4	4	10	18
Grand Total				**60**	**18**	**22**	**30**	**70**

X. ASSESSMENT METHODOLOGIES/TOOLS

Formative assessment (Assessment for Learning)

- Two offline unit tests of 30 marks and average of two unit test marks will be consider for out of 30 marks.
- For formative assessment of laboratory learning 25 marks.
- Each practical will be assessed considering 60% weightage to process, 40% weightage to product.

Summative Assessment (Assessment of Learning)

- End semester assessment is of 70 marks.
- End semester summative assessment is of 25 marks for laboratory learning.

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XI. SUGGESTED COS - POS MATRIX FORM

Course Outcomes (COs)	Programme Outcomes (POs)							Programme Specific Outcomes* (PSOs)		
	PO-1 Basic and Discipline Specific Knowledge	PO-2 Problem Analysis	PO-3 Design/ Development of Solutions	PO-4 Engineering Tools	PO-5 Engineering Practices for Society, Sustainability and Environment	PO-6 Project Management	PO-7 Life Long Learning	PSO-1	PSO-2	PSO-3
CO1	2	1	1	1	1	1	1			
CO2	2	2	2	1	1	1	2			
CO3	2	2	2	2	2	2	2			
CO4	3	2	2	2	2	2	2			
CO5	3	3	3	2	2	2	3			

Legends :- High:03, Medium:02,Low:01, No Mapping: -
*PSOs are to be formulated at institute level

XII. SUGGESTED LEARNING MATERIALS / BOOKS

Sr.No	Author	Title	Publisher with ISBN Number
1	R P Jain	Modern Digital Electronics	Mc Graw Hill, 2011 ISBN: 9780070669116
2	John F Wakerly	Digital Design ,Principles and Practices	PHI New Delhi ISBN : 8120327527
3	M Morris Mano,Michael D Ciletti	Digital Design with an introduction to the Verilog HDL	Pearson ISBN : 9788131794746
4	William I Fletcher	An Engineering Approach to Digital Design	PHI ISBN 0132776995
5	John M Yarbrough	Digital Logic Applications and Design	Vikas Publishing House ISBN : 0314066756

XIII . LEARNING WEBSITES & PORTALS

Sr.No	Link / Portal	Description
1	https://onlinecourses.nptel.ac.in/noc24_ee147/unit?unit=136&lesson=137	Digital Circuits
2	https://youtu.be/O3If0Nr9to0	Mealy and Moore circuits
3	http://elearn.psgcas.ac.in/nptel/courses/video/108105132/L47.html	Digital System
4	https://www.youtube.com/watch?v=gCAYY0fHPq4	PAL, PLA ,CPLD,FPGA
5	https://www.youtube.com/watch?v=uIW_CHP5gRg	ASM chart: Controller design -Counters, registers, sequence generator
6	https://www.youtube.com/watch?v=Dyp1EDgyUhA	ASM chart- Moore model and Mealy model
7	https://www.youtube.com/watch?v=9PczHQ8XdnQ	Simulation of asynchronous counters
8	https://www.youtube.com/watch?v=whNdDdVAITE	Simulation of counters.
9	https://www.youtube.com/watch?v=NsRUaM4HjiE	PSpice simulation for Digital Circuits
10	https://dld-iitb.vlabs.ac.in/exp/four-bit-digital-comparator/simulation.html	4 bit digital Comparator

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Sr.No	Link / Portal	Description

Note :

- Teachers are requested to check the creative common license status/financial implications of the suggested online educational resources before use by the students

MSBTE Approval Dt. 04/09/2025 **Semester - 6, K Scheme**