WINTER – 2018 EXAMINATION
MODEL ANSWER

Subject: Digital Techniques **Subject Code: 17333**

Important Instructions to examiners:
1) The answers should be examined by key words and not as word-to-word as given in themodel answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may tryto assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given moreImportance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No	Sub Q.N.	Answer	Marking Scheme
1.	**A)** **1)** **Ans.**	**Attempt any six:** **What is Positive logic and Negative logic in digital system?** **Positive Logic**: A logic 1 level represents a more positive of the two voltage levels while the least positive of the two voltage levels represents a logic 0 level. Example, If +5 V represents a logic 1 level And 0 V represents a logic 0 level Logic 1 = +5V Logic 0 = 0V Or if logic 1= +5V, logic 0 = +2V **Negative Logic**: A logic 1 level represents a most negative of the two voltage levels while the least negative of the two voltage levels represents a logic 0 level. Example, If 0V represents a logic 1 level And +5V represents a logic 0 level Logic 1 = 0V Logic 0 = +5V Or if logic 1= +2V, logic 0 = +5V	**12** **2M** ***Each term 1M***

2) Ans.

Define: i) Propagation delay ii) Noise margin. — **2M** ***Each definition 1M***

i) Propagation delay: Propagation delay is the average transition delay time for the signal to propagate from input to output when the signals change in value. It is expressed in ns.

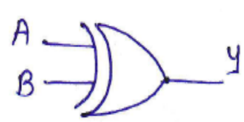
ii)Noise Margin: Noise immunity is defined as the ability of a logic circuit to tolerate the noise without causing any unwanted changes in the output. A quantitative measure of noise immunity is called as 'noise margin'.

3) Ans.

Draw the symbol and T.T. of i) EX-OR ii) NAND gate. — **2M** ***Each symbol with truth table 1M***

i) EX-OR

Symbol



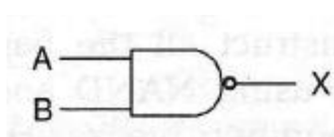
Truth Table

Truth Table for two input EX-OR gate. A logical gate whose output is one when odd number of inputs are one, for any other condition output is low.

Inputs		Output
A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

ii) NAND gate:

Symbol



Truth Table

Truth table

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

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4) Ans. **State De-Morgan's theorem.** — **2M** (*Each theorem 1M*)

Theorem1: It state that the, complement of a sum is equal to product of its complements

$$\overline{A + B} = \bar{A} . \bar{B}$$

Theorem2: It states that, the complement of a product is equal to sum of the complements.

$$\overline{AB} = \bar{A} + \bar{B}$$

5) Ans. **State any four Boolean laws.** — **2M** (*Any four laws ½ M each*)

	Theorem	Theorem No.
Commutative Laws	$A + B = B + A$	1
	$A . B = B . A$	2
Associative Laws	$A + (B + C) = (A + B) + C$	3
	$A(BC) = (AB)C$	4
Distributive Law	$A(B + C) = AB + AC$	5
AND Laws	$A . 1 = A$	6
	$A . A = A$	7
	$A . 0 = 0$	8
	$A . \bar{A} = 0$	9
OR Laws	$A + 0 = A$	10
	$A + A = A$	11
	$A + 1 = 1$	12
	$A + \bar{A} = 1$	13
Double Inversion Law	$\bar{\bar{A}} = A$	14
Absorption Laws	$A(A + B) = A$	15
	$A + AB = A$	16
Other Laws	$A + \bar{A}B = A + B$	17
	$(A + B)(A + C) = A + BC$	18
	$AB + \bar{A}\bar{B} = A$	19
	$AB + A\bar{B} = A$	20
De Morgan's Theorem	$\overline{AB} = \bar{A} + \bar{B}$	21

6) **Solve the following:** — **2M**

i) $(110101)_2 + (101101)_2$

ii) $(1010)_2 - (1000)_2$ using 1's complement method.

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	Ans.	**i) $(110101)_2 + (101101)_2$**
		i) $(110101)_2 + (101101)_2$
		Ans: carry 1 1 1 1
		  1 1 0 1 0 1
		+ 1 0 1 1 0 1
		1 1 0 0 0 1 0
		Ans: $(1100010)_2$
		
		ii) $(1010)_2$ - $(1000)_2$ using 1's complement method.
		Step 1: → 1000
		↓↓↓↓
		0111 (1's compliment of 2nd No.)
		Step 2 → carry 1 1
		1010 (First No)
		+ 0111 (1's compliment of 2nd No.)
		Step 3 Carry → 1 0001
		     1 (Add the carry with the result)
		0010
		Step 4: Result is in true form
		Ans: $(1010)_2 - (1000) = (0010)_2$
			Each Solution 1M

	7)	**Draw the logic diagram of IC 7485.** ***Note: Any other relevant diagram shall be considered.***	**2M**

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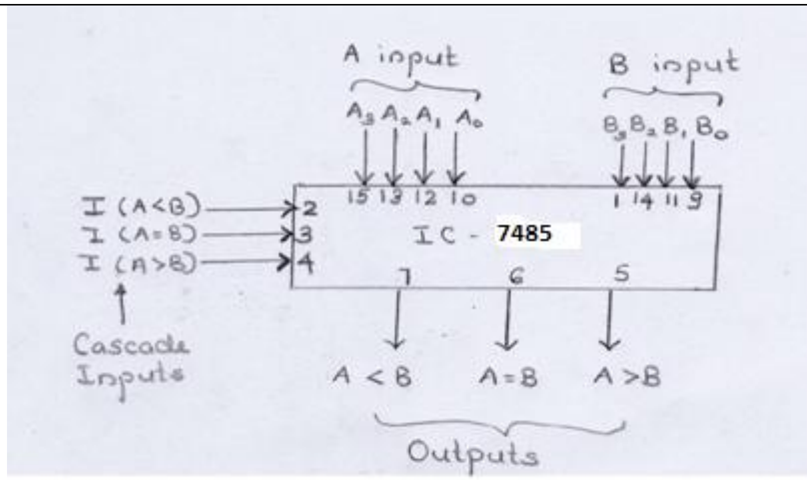
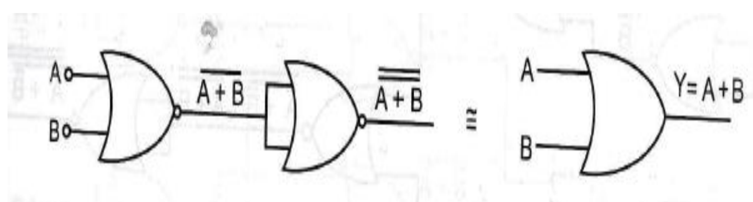
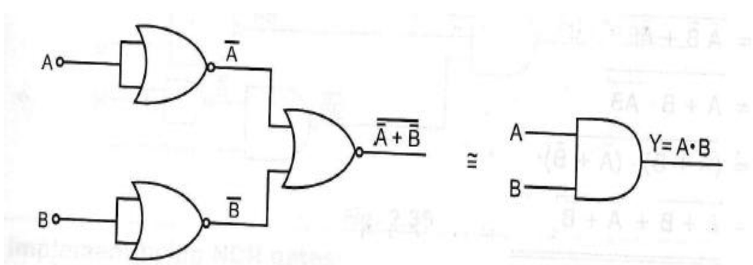
	Ans.		***Correct diagram 2M***
	8) **Ans.**	**Define any two specifications of ADC.** **1. Resolution:** The voltage input change necessary for a one-bit change in the output is called the resolution. It can also be expressed as a percentage. The resolution in terms of voltage is the full-scale input voltage divided by the total number of bits. % Resolution = $\frac{V_{FS}}{2^n - 1}$ x 100 **2. Accuracy:** The accuracy of the A/D converter depends upon the accuracy of its circuit components. The relative accuracy of an A/D converter is the maximum deviation of the digital output from the ideal linear line. **3. Conversion time:** The conversion time is the time required for conversion from an analog input voltage to the stable digital output. This conversion time is also called as speed**.** **4. Linearity:** Linearity is conventionally equal to the deviation of the performance of the converter from a best straight line. **5. Differential Linearity:** The differential linearity is defined as the maximum amount of voltage change necessary to cause the digital output to change one bit minus the ideal voltage change necessary to change one bit.	**2M** ***Any two specifications 1M each***

		6. Monotoxicity: In response to a continuously increasing input signal, the output of an A/D converter should not at any point decrease or skip one or more codes. This is called the monotoxicity of the A/D converter. **7. Analog Input voltage:** This is the maximum allowable input voltage range. **8. Format of Digital output:** An A/D converter can be made for any standard digital code. **9. Quantization error:** The approximation process is known as quantization. The error due to the quantization process is known as quantization error.	
1.	**B)** **a)** **Ans.**	**Attempt any two:** **Design OR and AND gate using NOR gate only.** **OR gate using NOR gate:** Expression for OR gate is Y = A + B = $\overline{\overline{A + B}}$  **AND gate using NOR gate:** Expression for AND gate is Y = AB = $\overline{\overline{AB}}$ (as $\overline{\overline{A}} = A$) Applying De Morgan's second theorem, Y = $\overline{\overline{A} + \overline{B}}$, we can implement using NOR gates at this stage. 	**8** **4M** ***OR gate using NOR gate 2M*** ***AND gate using NOR gate 2M***

	b) **Ans.**	**Perform BCD addition:** **i) $(264)_{10} + (668)_{10}$** **ii) $(454)_{10} + (379)_{10}$** **i) $(264)_{10} + (668)_{10}$** BCD addition:- $(264)_{10}$ ⟶ 0010 0110 0100 $(668)_{10}$ ⟶ 0110 0110 1000 Addition: 1000 1100 1100 invalid BCD >9 Add $(06)_{10}$: 0110 0110 1001 0011 0010 ↓ ↓ ↓ 9 3 2 $(264)_{10} + (668)_{10} = (932)_{10}$ **ii) $(454)_{10} + (379)_{10}$** $(454)_{10}$ ⟶ 0100 0101 0100 $(379)_{10}$ ⟶ 0011 0111 1001 Addition: 0111 1100 1101 Invalid BCD >9 Add $(06)_{10}$: 0110 0110 1000 0011 0011 ↓ ↓ ↓ 8 3 3 $(454)_{10} + (379)_{10} = (833)_{10}$	**4M** ***Each addition 2M***

c) **Compare TTL and CMOS Logic family on the basis of propagation delay, power dissipation, Fan out and components used.** **4M**

Ans.

Parameter	TTL	CMOS
Propagation Delay	10 ns	70 ns
Power dissipation	10 mW	0.01mW
Fan out	10	50
Components Used	Fabricate Bipolar Transistor on the chip	MOS family fabricates. MOS field effect transistors (MOSFETs)

Each comparison 1M

2. **Attempt any four:** **16**

a) **Draw EX-OR gate using NAND gate only. Also write O/P of each gate.** **4M**

Ans.

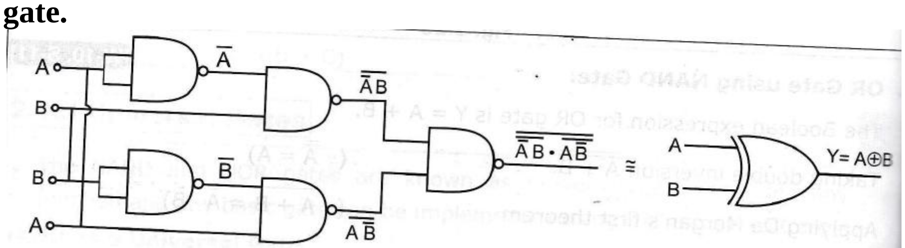
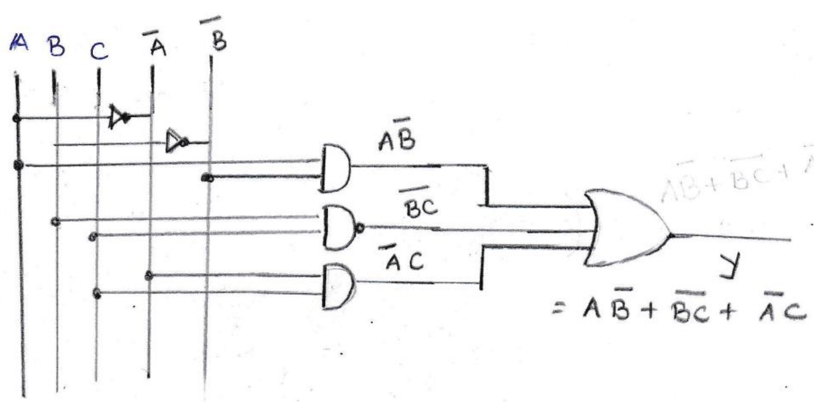


Diagram 2M

Output 2M

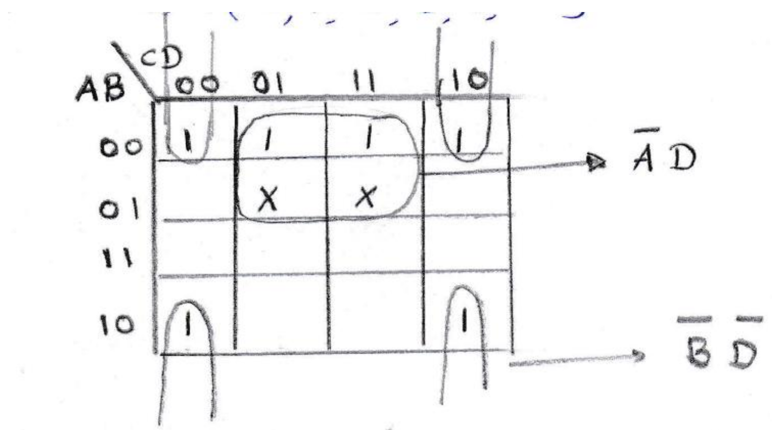
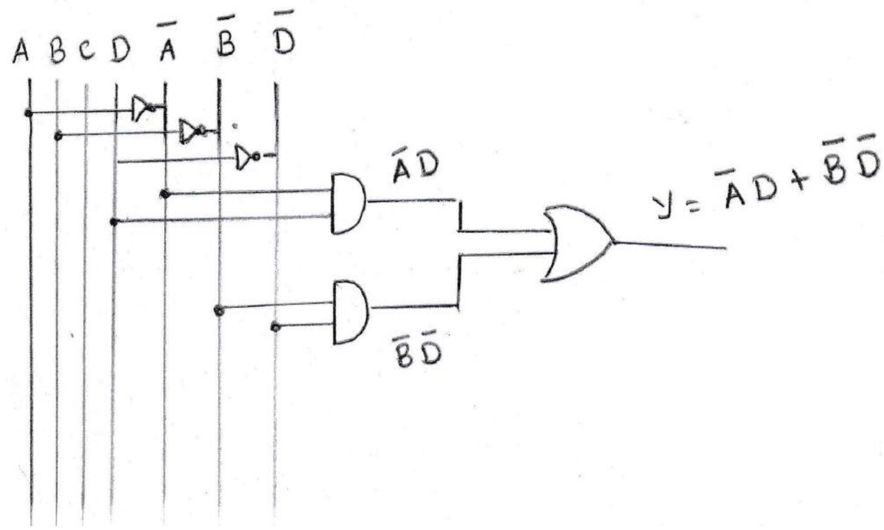
b) **Given Y = A $\overline{B}$ + $\overline{BC}$ + $\overline{A}$C.** **4M**
Implement the logical expression using gates.

Ans.



Correct implementation 4M

	c) Ans.	**Perform 2's complement subtraction $(59)_{10}$ - $(62)_{10}$.**	4M
		$(59)_{10} = (111011)_2$ $(62)_{10} = (111110)_2$ ↓↓↓↓↓↓ step 1 → 000001 (1's compliment of 2nd No) + 1 000010 (2's compliment of 2nd No) step 2 → 111011 (1st No) + 000010 (2's compliment of 2nd No) 111101 (59: 2|59, 2|29-1, 2|14-1, 2|7-0, 2|3-1, 1-1; 62: 2|62, 2|31-0, 2|15-1, 2|7-1, 2|3-1, 1-1) **Step 3** No carry. Answer is -ve. Take 2s compliment of Result 111101 —1's Compliment→ 000010 + 1 000011 (2's compliment of Result) **Step 4** Answer is $(000011)_2 = 1\times2^0 + 1\times2^1 + 0 + 0 + 0$ $= 1 + 2$ $= 3$ Answer is -ve $(59)_{10} - (62)_{10} = (-3)_{10}$	*Each step 1M*

	d)	**Simplify the following equation using K-map and realize it using logic gates.** $$Y = \sum m(0,1,2,3,8,10) + \sum d(5,7).$$	**4M**
	Ans.	 $Y = \bar{A}D + \bar{B}\bar{D}$ 	***Simplify 2M*** ***Realize 2M***

e) **Draw block diagram of Decimal to BCD encoder and write its truth table.** **4M**

Ans.

Block diagram

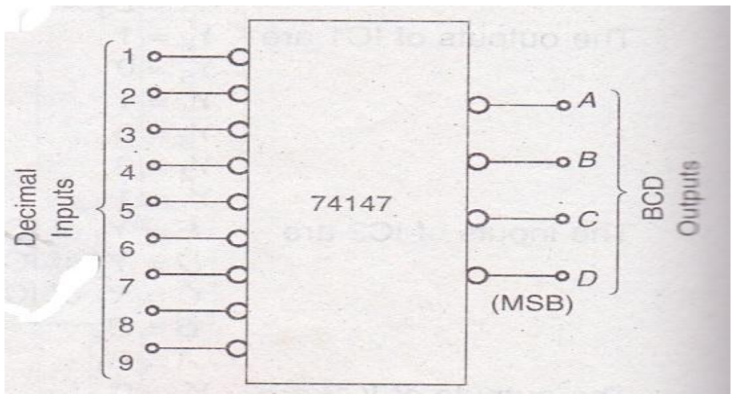


Diagram 2M

Truth Table

Active-low decimal inputs									Active-low BCD outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	0
×	0	1	1	1	1	1	1	1	1	1	0	1
×	×	0	1	1	1	1	1	1	1	1	0	0
×	×	×	0	1	1	1	1	1	1	0	1	1
×	×	×	×	0	1	1	1	1	1	0	1	0
×	×	×	×	×	0	1	1	1	1	0	0	1
×	×	×	×	×	×	0	1	1	1	0	0	0
×	×	×	×	×	×	×	0	1	0	1	1	1
×	×	×	×	×	×	×	×	0	0	1	1	0

Truth Table 2M

f) **Design Half adder using K-map and basic gates.** **4M**

Ans. **Half adder:** A logic circuit for the addition of two one-bit numbers is referred to as a half-adder. The addition process a reproduced in truth table form in Table. Here, A and B are the two inputs and S(SUM) and C (CARRY) are the two outputs

Table: Truth table of a half-adder

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Using K-map 2M

K-map for Sum

	$\overline{B}$	B
$\overline{A}$	0	1
A	1	0

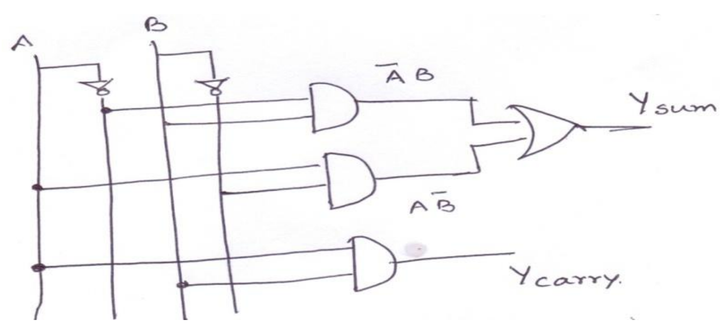
K-map for Carry.

	$\overline{B}$	B
$\overline{A}$	0	0
A	0	1

$Y_{sum} = \overline{A}B + A\overline{B}$

$Y = A \oplus B$.

$Y_{carry} = AB$.



Using basic gates- 2M

3.	**a)**	**Attempt any four:** **Simplify using De-Morgan's theorem and realize it using basic gates:** $\mathbf{Y} = \overline{(A\overline{B} + \overline{A}\overline{B})\,(AB + \overline{A}B)}$	**16** **4M**

Ans.

$$Y = \overline{(A\bar{B} + \bar{A}\bar{B})(AB + \bar{A}B)}$$

Solution :- using Demorgans theorem, $\overline{AB} = \bar{A} + \bar{B}$

$$Y = \overline{(A\bar{B} + \bar{A}\bar{B})} + \overline{(AB + \bar{A}B)} \quad \text{.........} \quad (1M)$$

$$= \left[\overline{A\bar{B}} \cdot \overline{\bar{A}\bar{B}}\right] + \left[\overline{AB} \cdot \overline{\bar{A}B}\right]$$

$$(\because \bar{A} + \bar{B} = \overline{AB})$$

$$= \left[(\bar{A} + \bar{\bar{B}}) \cdot (\bar{\bar{A}} + \bar{\bar{B}})\right] + \left[(\bar{A} + \bar{B}) \cdot (\bar{\bar{A}} + \bar{B})\right] \quad \text{......} \quad (1m)$$

$$= \left[(\bar{A} + B)(A + B)\right] + \left[(\bar{A} + \bar{B})(A + \bar{B})\right]$$

$$(\because \bar{\bar{A}} = A, \ \bar{\bar{B}} = B)$$

$$= \left[A\bar{A} + \bar{A}B + AB + BB\right] + \left[\bar{A}A + \bar{A}\bar{B} + A\bar{B} + \bar{B}\bar{B}\right]$$

$$= 0 + \bar{A}B + AB + B + 0 + \bar{A}\bar{B} + A\bar{B} + \bar{B} \quad \text{........} \quad (1M)$$

$$\left(\because \begin{array}{l} A\bar{A} = 0 \\ BB = B \\ \bar{B}\bar{B} = \bar{B} \end{array}\right)$$

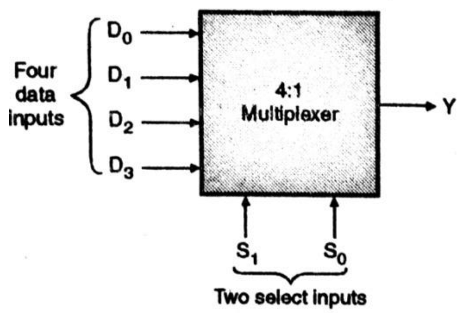
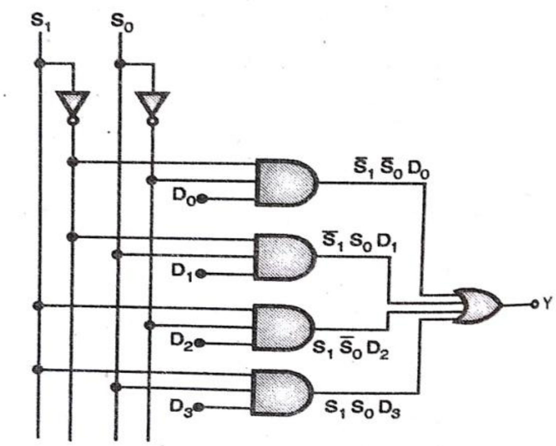
$$Y = B(\bar{A} + A + 1) + \bar{B}(\bar{A} + A + 1)$$

$$= B + \bar{B} \qquad (\because 1 + A + \bar{A} = 1) \quad \text{..........} \quad (1m)$$

$$\boxed{Y = 1}$$

Since the output is equal to 1 the input line can be directly connected to logic 1 line**.**

b) **Draw the logical block diagram of 4:1 mux and describe its working. Give the expression for the o/p and draw the circuit diagram using gates.** **4M**

	Ans.	**Logical Block Diagram**  **Working:** If S1S0=00, the data bit D0 will be selected and routed to the output. Similarly if, S1S0=01, the data bit D1 will be selected and routed to the output S1S0=10, the data bit D2 will be selected and routed to the output S1S0=11, the data bit D3 will be selected and routed to the output i.e. Output will be high when the selected input D0 & D1is 1. Hence the logical expression for output is in SOP form. **Output Expression** $Y = \overline{S}_1 \overline{S}_0 D_0 + \overline{S}_1 S_0 D_1 + S_1 \overline{S}_0 D_2 + S_1 S_0 D_3$ **Circuit Diagram Using Gates**  	***Logical block diagram 1M*** ***Working 1M*** ***Output expression 1M*** ***Circuit diagram using gates 1M***

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c) **Draw the block diagram of BCD to seven segment decoder/driver using IC 7447. Also draw its Truth Table.** **4M**

Note: Any one type of display shall be considered

Ans.

1. BCD to **7** segment decoder is a combinational circuit that accepts 4 bit BCD input and generates appropriate 7 segment output. ***Explanation 1M***

2. In order to produce the required numbers from 0 to 9 on the display the correct combination of LED segments need to be illuminated.

3. A standard 7 segment LED display generally has 8 input connections, one from each LED segment & one that acts as a common terminal or connection for all the internal segments

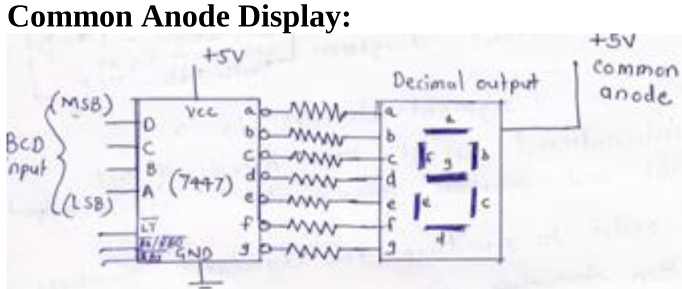
4. Therefore there are 2 types of display

1. Common Anode Display

2. Common Cathode Display

Common Anode Display:

Circuit diagram 2M



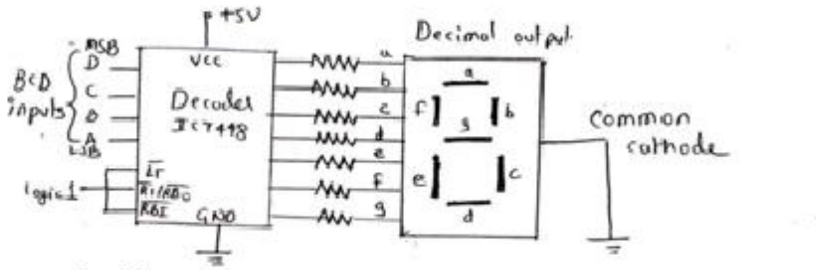
For normal functioning $\overline{LT}$, $\overline{BI}/\overline{RBO}$ & $\overline{RBI}$ should be connected to logic 1

Truth Table ***Truth Table 1M***

For seven segment decoder using common anode display

BCD Inputs				7 segment coded outputs							Display outputs
D	C	B	A	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	1	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	1	1	0	0	9

Common Cathode Display:

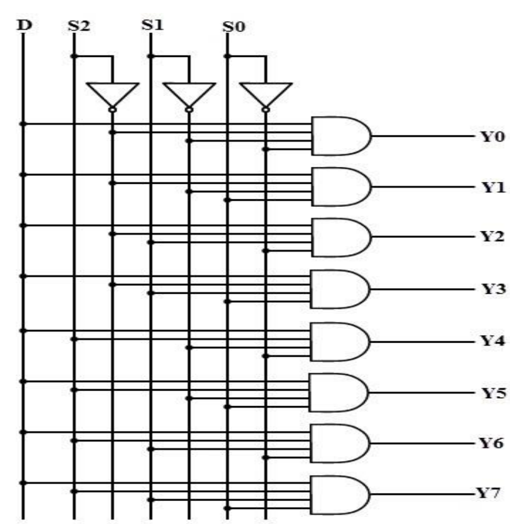


Truth Table

BCD inputs				7 segment coded outputs							Display outputs
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	0	0	1	1	9

d) Ans. **Design 1 : 8 demux using basic gates.** **4M**

Circuit diagram:



Correct diagram 4M

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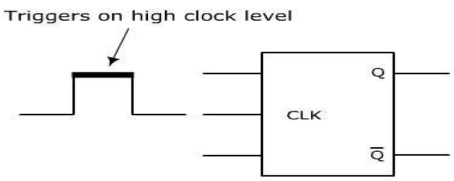
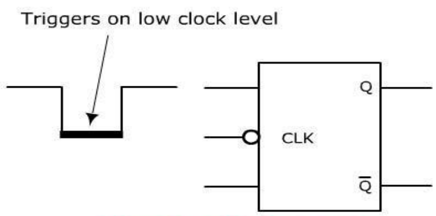
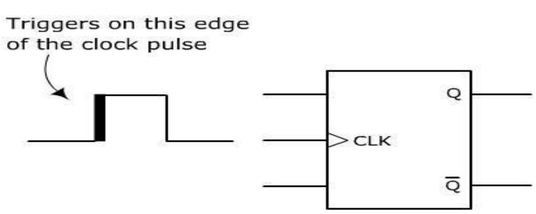
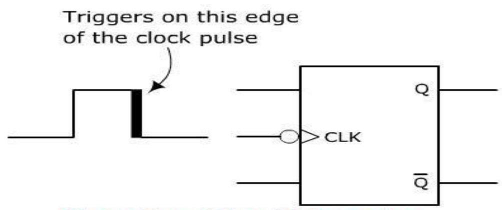
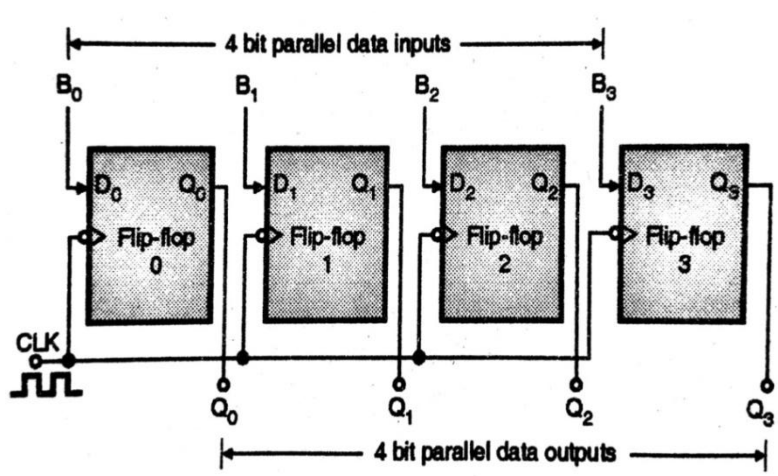
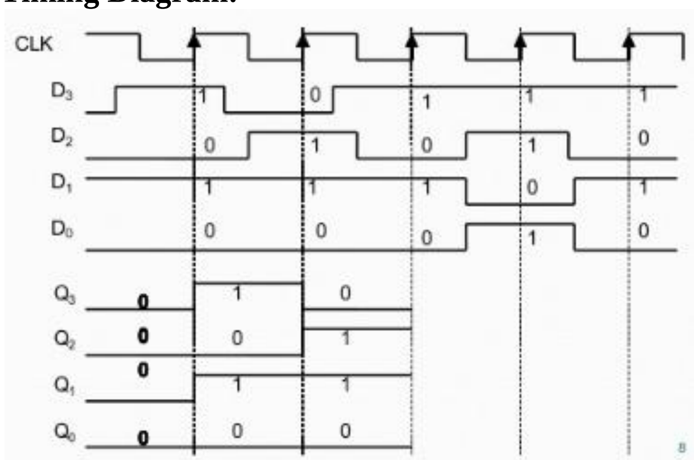
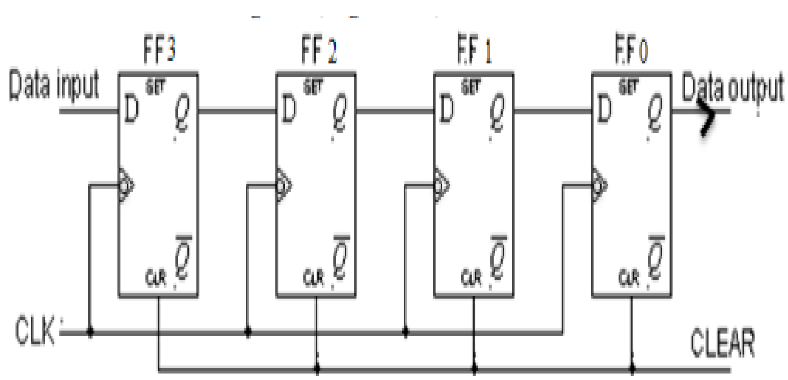
	e) **Ans.**	**Explain different triggering methods used in Flip Flops.** There are four types of pulse-triggering methods: 1.**Positive (High) Level Triggering:** When a flip flop is required to respond at its HIGH state a HIGH level triggering method is used. It is mainly identified from the straight lead from the clock input. Take a look at the symbolic representation shown below.  High Level Triggering **2. Negative (Low) Level Triggering:** When a flip flop is required to respond at its LOW state, a LOW level triggering method is used. It is mainly identified from the clock input lead along with a low state indicator bubble. Take a look at the symbolic representation shown below.  Low Level Triggering **3. Positive Edge Triggering:** When a flip flop is required to respond at a LOW to HIGH transition state, POSITIVE edge triggering method is used. It is mainly identified from the clock input lead along with a triangle. Take a look at the symbolic representation shown below.  Positive Edge Triggering	**4M** ***Four triggering Methods 1M each***

		4. Negative Edge Triggering: When a flip flop is required to respond during the HIGH to LOW transition state, a NEGATIVE edge triggering method is used. It is mainly identified from the clock input lead along with a low-state indicator and a triangle.  Negative Edge Triggering	
	f) **Ans.**	**Explain working of PIPO with neat logic diagram and timing diagram.** **Logic Diagram:**  **Explanation:** 1. 4- bit binary input i.e. B0, B1, B2, B3 is applied to the data inputs D0, D1, D2, D3 respectively of the four flip flops. 2. As soon as the clock edge is applied , the input binary bits will be loaded into the flip-flops simultaneously. 3.The loaded bits will appear simultaneously to the output side. Only one clock pulse is needed to load all bits hence PIPO mode is the fastest mode of operation.	**4M** ***Logic diagram 2M*** ***Explanation 1M***

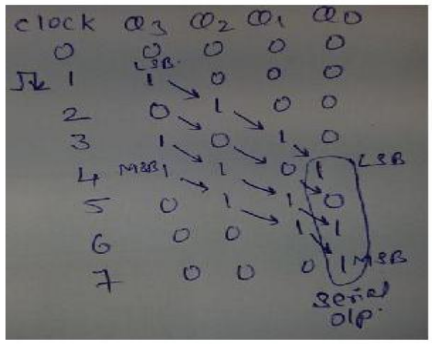
<table>
<tr><td></td><td></td><td>Timing Diagram:
</td><td>Timing diagram 1M</td></tr>
<tr><td>4</td><td>a)

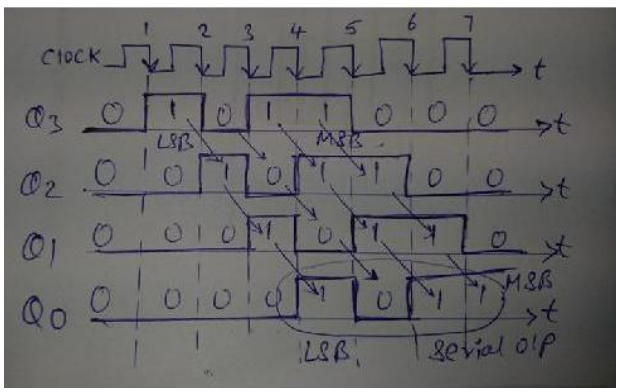
Ans.</td><td>Attempt any four:
Draw 4-bit SISO shift register using D-F/F and explain its working with timing diagram.
Diagram:

Description-As shown a 4 bit SISO shift register consists of 4 D flip-flop, data is fed from first flip-flop and on application of clock pulses the data is shifted from first flip-flop to the last flip-flop, working as serial in and serial out shift register.
Let the data be -1101.</td><td>16
4M

Logic Diagram 2M</td></tr>
</table>

The truth table and timing diagram is as shown below

Truth table & timing diagram 2M





b) Ans. **Explain successive approximation type ADC with neat diagram.** **4M**

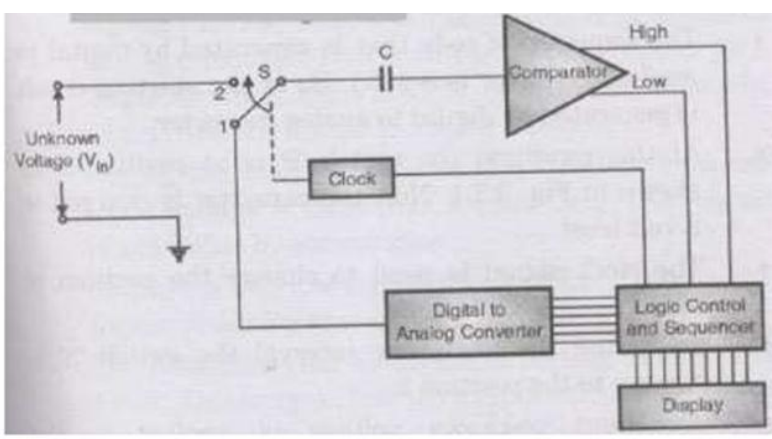


Diagram 2M

		Explanation: DAC= Digital to Analog converter EOC= End of conversion SAR =Successive approximation register S/H= Sample and hold circuit Vin= input voltage Vref= reference voltage The successive approximation Analog to Digital converter circuit typically consisting of four sub circuits- 1. A sample and hold circuit to acquire the input voltage Vin. 2. An analog voltage comparator that compares Vin to the output of internal DAC and outputs the result of comparison to successive approximation register(SAR). 3. SAR sub circuits designed to supply an approximate digital code of Vin to the internal DAC. 4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of digital code output of SAR for comparison with Vin. The successive approximation register is initialized so that most significant bit (MSB) is equal to digital 1. This code is fed into DAC which the supplies the analog equivalent of this digital code Vref/2 into the comparator circuit for the comparison with sampled input voltage. If this analog voltage exceeds Vin the comparator causes the SAR to reset the bit, otherwise a bit is left as 1. Then the next bit is set to 1 and the same test is done continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by DAC at end of the conversion (EOC).	***Explanation 2M***
	c)	**Describe working of RS Flip Flop using NAND gates only.** ***Note: Short explanation of truth table shall be considered***	**4M**

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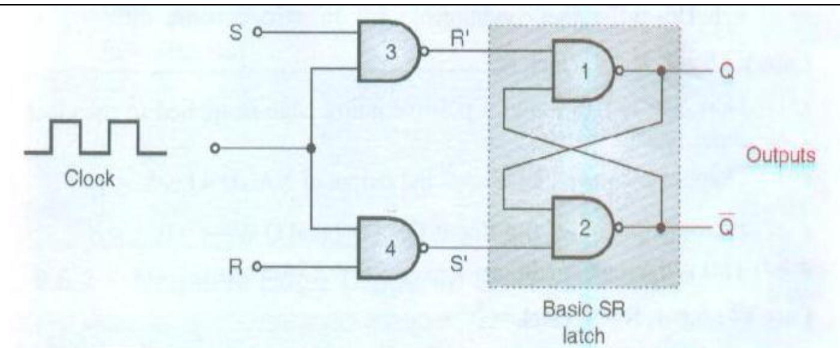
	Ans.	Clocked S - R Flip-flop (Positive edge triggered) This circuit will operate as an SR flip-flop only for the positive clock edge but there is no change in output if clock = 0 or even for the negative going clock edge. **Operation :** **Case I : S = X, R = X, clock = 0** • Since clock = 0, the outputs of NAND gates 3 and 4 will be forced to be 1 irrespective of the values of S and R. That means R'= S' = 1. These are the inputs of the SR latch. • Hence the outputs of basic SR/F/F i.e. Q and Q will not change. Thus if clock = 0, then there is no change in the output of the clocked SR flip-flop. **Case II : S = X, R=X, clock = 1 (High level)** • As this flip flop does respond not respond to levels applied at the clock input, the outputs Q and Q will not change. So, Q n+1 = Qn **Case III : S = R = 0 : No change** • If S=R=0 then outputs of NAND gate 3 and 4 are forced to become 1. • Hence R' and S' both will be equal to 1. Since R' and S' are the inputs of the basic S – R flip-flop using NAND gates. There will be no change in the state of outputs. **Case IV : S =1, R = 0, clock = ↑** • Now S=0, R=1 and a positive going edge is applied to the clock input.	***Diagram 2M*** ***Explanation 2M***

- Output of NAND 3 i.e. R’ = 0 and output of NAND 4 i.e. S’ = 1.
- Hence output of SR flip-flop is Q n+1 = and Q n+1 = 0.
- This is the reset condition.

Case V : S =1, R = 0, clock =↑

- Now S=0, R=1 and a positive edge is applied to the clock input.
- Since S=0, output of NAND – 3 i.e. R´= 1. And as R’ = 1 and clock = 1 the output of NAND-4 i.e. S´ = 0. Hence this is the reset condition.

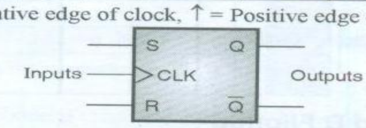
Case VI : S =1, R = 1, clock ↑

- As S=1, R=1 and clock = 1, the outputs of NAND gates 3 and 4 both are 0 i.e. S' = R'=0.
- Hence the “Race Around” condition will occur in the basic SR flip-flop.
- The symbol of positive edge triggered SR flip flop is as shown in figure and the truth table is also shown in figure.

Truth table of a positive edge triggered SR flip flop

Inputs			Outputs		Remark
CLK	S	R	Q_{n+1}	$\bar{Q}_{n+1}$	
0	×	×	Q_n	$\bar{Q}_n$	No change (NC)
1	×	×	Q_n	$\bar{Q}_n$	No change (NC)
↓	×	×	Q_n	$\bar{Q}_n$	No change (NC)
↑	0	0	Q_n	$\bar{Q}_n$	No change (NC)
↑	0	1	0	1	Reset
↑	1	0	1	0	Set
↑	1	1	Race	Race	Avoid

↓ = Negative edge of clock, ↑ = Positive edge of clock



Symbol of positive

- Note that for clock input to be at negative or positive levels as the edge triggered flip flop does not respond. Similarly it does not respond to the negative edge of the clock.

		1. The flip-flop will respond only to the positive edge of clock. 2.With positive edge of the clock, the SR flip flop behaves in the following way : S = R = 0 → No change in output S = 0, R = 1 → $Q_{n+1} = 0, \bar{Q}_{n+1} = 1$ Reset condition S = 1, R = 0 → $Q_{n+1} = 1, \bar{Q}_{n+1} = 0$ Set condition S = R = 1 → Race condition.	
	d) **Ans.**	**Explain the techniques used in elimination of Race-around condition.** **Race-around condition is eliminated by:** 1. Design the clock (enable)with time less than toggling time (but this method is not economical) 2. Use edge triggering. 3. Use Master slave JK flip-flop **Use edge triggering:** If the Clock On or High time is less than the propagation delay of the flip flop then racing can be avoided. This is done by using edge triggering rather than level triggering. **Use Master slave JK flip-flop:** A master slave JK flip flops is a cascade of two JK flip-flops, with feedback from the output of the second to the inputs of the first. Direct clock pulses are applied to the first flip flop and clock pulses are inverted before these are applied to the second flip flop. At the same time, the second flip-flop is inhibited. Whenclk=0, the second flip flop is enabled and the first flip-flop is inhibited. Therefore the outputs Q and $\bar{Q}$ follow the output Qmand $\bar{Q}_m$. Since the second flip flop simply follows the first one, it is referred to as the slave and the first one as the master. Hence the configuration is referred as master-slave (M-S) flip flop.	**4M** ***Each condition 2M***

e) **Define memory. Give classification of memory. Compare PROM and EPROM. (any 2 points)** **4M**

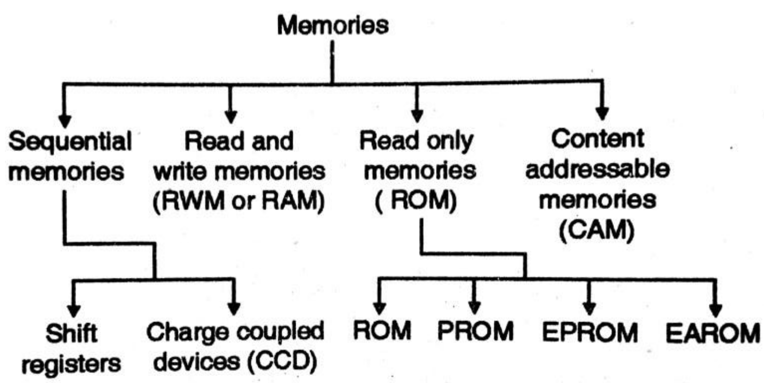
Ans.

Definition:

It is a subsystem of digital processing system which can store unprocessed, partially processed data & result is called as Memory.

Definition 1M

Classification:



Classification 1M,

Comparison

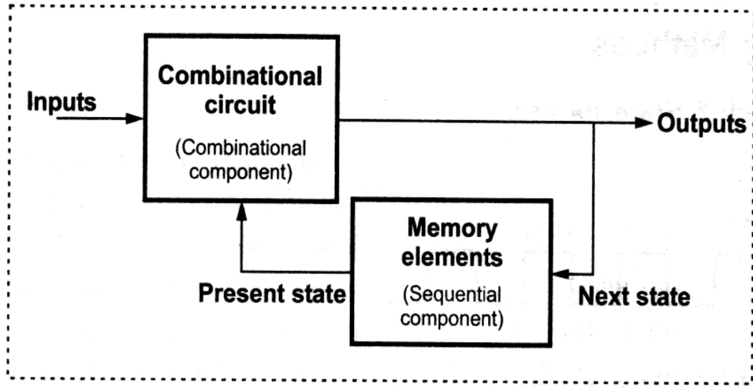
Any two points 2M

Sr. No.	PROM	EPROM
1.	PROMs can be programmed only once.	EPROMs are reusable and can be programmed multiple times.
2.	The process in the programming of PROMs is irreversible. Hence the memory is permanent.	In EPROMs memory can be erased by exposure to UV light.
3.	PROMs are enclosed in complete plastic packaging ; therefore UV has no effect on PROMs.	EPROMs have a fused quartz window in the packaging to allow this.
4.	In PROMs data is written/ programmed onto the chip by blowing the fuses at each bit using much higher voltages than the average voltages used in digital circuits.	EPROMs also use high voltage, but not enough to alter the semiconductor layer permanently.

	f) **Ans.**	**What is the need of data converters? List specifications of DAC.** **Need of data converters:** It is often necessary that before processing the analog data, by a digital system, it should be changed to digital form as noise may get added hence difficult to process, store or transmit. Similarly, after processing the data, it may be desirable that the final result obtained in digital form be converted back to the analog form therefore data converters are needed. **Specifications of DAC:** **Following are the specifications of DAC** 1. Resolution 2. Linearity 3. Accuracy 4. Settling Time 5. Temperature Sensitivity 6. Long term drift 7. Supply Rejection 8. Speed	**4M** ***Need 2M*** ***Any four specifications 1/2 M each***
5.	 **a)** **Ans**	**Attempt any four:** **Convert the following:** i) $(366.54)_8 \rightarrow (?)_{10}$ and ii) $(2015.32)_{10} \rightarrow (?)_{16}$ i) $(366.54)_8 = (\quad)_{10}$ 3 6 6 . 5 4 $= 3\times8^2 + 6\times8^1 + 6\times8^0 . 5\times8^{-1} + 4\times8^{-2}$ $= 192 + 48 + 6 . (0.625 + 0.0625)$ $= 246 . 06875$ $\therefore (366.54)_8 = (246.06875)_{10}$ 2) $(2015.32)_{10} = (\quad)_{16}$ (a) 16 | 2015 16 | 125 — 15 16 | 7 — 13 0 — 7 (b) $0.32 \times 16 = 5.12$ $0.12 \times 16 = 1.92$ $0.92 \times 16 = 14.72$ $\therefore (2015.32)_{10} = (7DF.51E)_H$	**16** **4M** ***Each Conversion 2M***

b) **Draw the block diagram of sequential logic and state the importance of clock signal in it.** **4M**

Ans.



Sequential circuit

Diagram 2M

Clock: A clock signal is a particular type of signal that oscillates between a high and a low state and is utilized to co-ordinate actions of the sequential circuits. It is produced by clock generator. The time required to complete one cycle is called as "clock period" or "clock cycle".

Importance:

- Most integrated circuits (ICs) of sufficient complexity use a clock signal in order to synchronize different parts of the circuit, cycling at a rate slower than the worst-case internal propagation delays.
- In some cases, more than one clock cycle is required to perform a predictable action.
- A clock signal might also be gated, that is, combined with a controlling signal that enables or disables the clock signal for a certain part of a circuit. This technique is often used to save power by effectively shutting down portions of a digital circuit when they are not in use, but comes at a cost of increased complexity in timing analysis.
- It is also used to open and close digital paths, allow or stop a process and in general provide timing for the circuit.

Importance 2M

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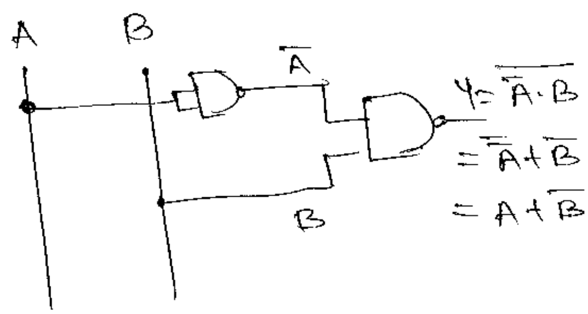
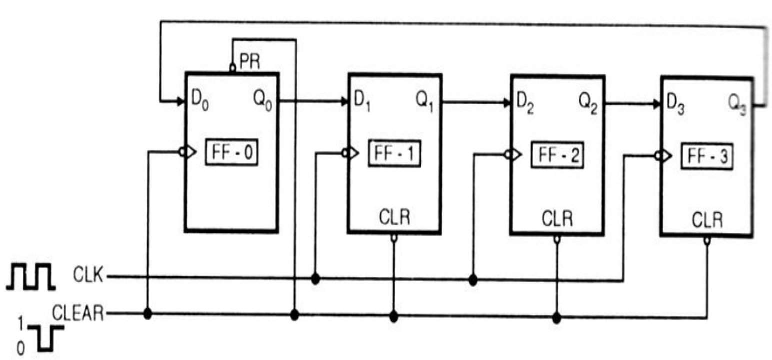
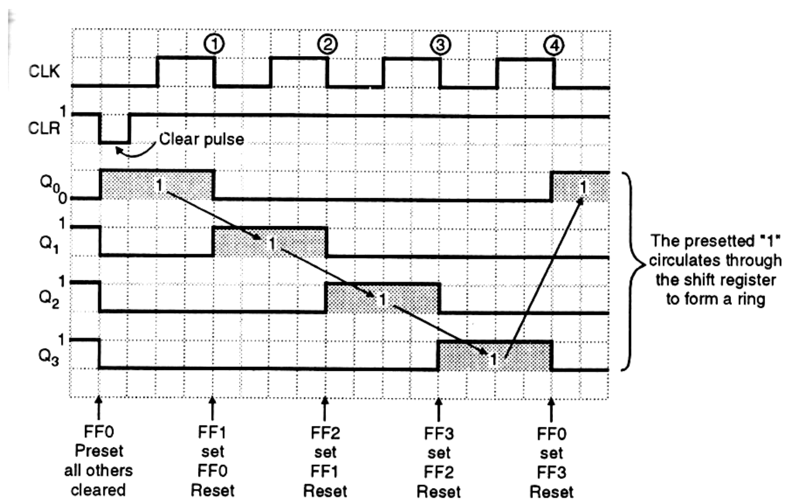
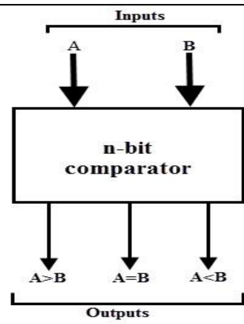
	c) **Ans.**	**Simplify the following and realize it.** $\mathbf{Y = A + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + ABC + \bar{A}\bar{B}}$ $Y = A + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + ABC + \bar{A}\bar{B}$ $Y = A + \bar{B}C + \bar{A}\bar{B} + ABC$ $Y = A + \bar{B} + C(\bar{B} + AB)$ $Y = A + \bar{B} + C(\bar{B} + A)$ $Y = A + \bar{B} + \bar{B}C + AC$ $Y = A(1 + C) + \bar{B}(1 + C)$ $Y = A + \bar{B}$ 	**4M** ***Simplify 3M*** ***Realize 1M***
	d) **Ans.**	**Draw the circuit of ring counter and describe with timing diagram.** The output of FF-3 is connected back to FF-0 input. This is a special type of shift register. Initially a low clear pulse is applied to all flip-flops. Hence all flip-flops except FF-0 are cleared but FF-0 is preset hence the corresponding outputs are Q3- Q0 = 0001. 	**4M** ***Circuit Diagram 2M***

		The waveforms of Ring Counter are as shown: 	***Timing Diagram 2M***
	e) **Ans.**	**Describe block diagram of digital comparator and write truth table of 2-bit comparator.** A magnitude digital comparator is a combinational circuit that compares two digital or binary numbers (consider A and B) and determines their relative magnitudes in order to find out whether one number is equal, less than or greater than the other digital number. Three binary variables are used to indicate the outcome of the comparison as A>B, A<B, or A=B. The below figure shows the block diagram of a n-bit comparator which compares the two numbers of n-bit length and generates their relation between themselves.	**4M** ***Block Diagram 2M***



2 Bit comparator: The first number A is designated as A = A1A0 and the second number is designated as B = B1B0. This comparator produces three outputs as G (G = 1 if A>B), E (E = 1, if A = B) and L (L = 1 if A<B).

Truth Table 2M

Inputs				Outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

<table>
<tr><td></td><td>f)

Ans.</td><td>Compare Synchronous and Asynchronous counter (any 4 points).

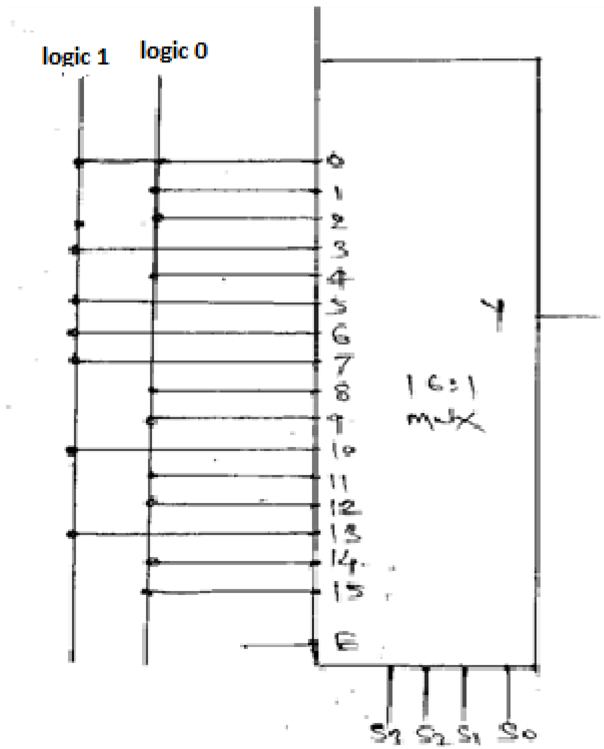
<table>
<tr><th>Sr. No</th><th>Asynchronous counter</th><th>Synchronous Counter</th></tr>
<tr><td>1.</td><td>In this type of counter the flip flops are connected in such a way that output of first flip flop drives the clock for the next flip flop.</td><td>In this type of counter there is no connection between the output of first flip flop and clock input of next flip flop.</td></tr>
<tr><td>2.</td><td>All the flip flops are not clocked simultaneously.</td><td>All the flip flops are simultaneously clocked.</td></tr>
<tr><td>3.</td><td>Logic circuit is very simple even for more number of states.</td><td>Design involves complex logic circuit as number of states increases.</td></tr>
<tr><td>4.</td><td>Main drawback of these counters is that their low speed as the clock is propagated through number of flip flops before it reaches last flip flop.</td><td>As clock is simultaneously given to all flip flops there is no problem of propagation delay. Hence they are high speed counters and are preferred when number of flip flops increases in the given design.</td></tr>
</table></td><td>4M

Any four points 1M each</td></tr>
<tr><td>6.</td><td>a)

Ans.</td><td>Attempt any two:
i) Convert the following SOP equation into std. SOP equation.
$Y = AB + \bar{A}B + A\bar{B}\bar{C}$
$Y = AB + \bar{A}B + A\bar{B}\bar{C}$
$Y = AB(C+\bar{C}) + \bar{A}B(C+\bar{C}) + A\bar{B}\bar{C}$
$Y = ABC + AB\bar{C} + \bar{A}BC + \bar{A}B\bar{C} + A\bar{B}\bar{C}$</td><td>16
2M
Correct Conversion 2M</td></tr>
<tr><td></td><td></td><td>ii) List any four applications of multiplexer and implement the following logic expression using 16 : 1 Mux.
$Y = \sum m(0, 3, 5, 6, 7, 10, 13)$</td><td>6M</td></tr>
</table>

<table>
<tr><td></td><td>Ans.</td><td><u>Applications of Multiplexer IC's:</u>

1. It is used as a data selector to select one out of many data inputs.
2. It is used for simplification of logic design.
3. In the data acquisition system.
4. In designing the combinational circuit.
5. In the DAC.
6. To minimize the number of connections.


</td><td>Any four application ½ M each

Implementation 4M</td></tr>
<tr><td></td><td>b)
Ans.</td><td>i) List two applications of flip flops.
1. It can be used as memory element.
2. It can be used to eliminate key debounce.
3. It is used as a basic building block in sequential circuits such as counters and registers.
4. It can be used as delay element.</td><td>2M
Any two applications 1M each</td></tr>
</table>

ii) What is Modulus of counter? Show the method to determine the no. of flip flops for a mod-52 counter. **2M**

Ans. The total number of counts or stable states a counter can indicate is called as Modulus of counter. It is used to describe the count capability of counters.

For mod 52 counter:

The number of states and number of flips flops are related by formula: $2^n \geq m$

Where n= no of states and m = no of flips flops.

For 52 states (n= 52)

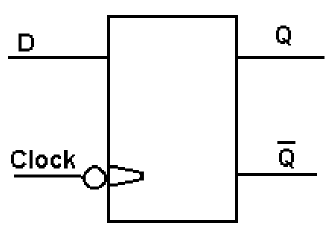
number of flip flops are: 6

Modulus of counter definition 1M
No of flip flops determination 1M

b) **iii) Draw symbol and truth table of negative edge triggered D-flip-flop and positive edge triggered JK-flip flop.** **4M**

Ans. **Negative edge triggered D flip flop:**

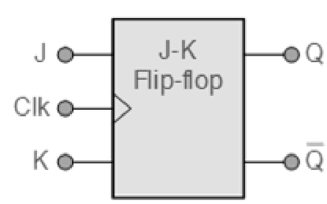
Symbol **Truth Table**



Input D_n	Output Q_{n+1}
0	0
1	1

Positive edge triggered JK flip flop:

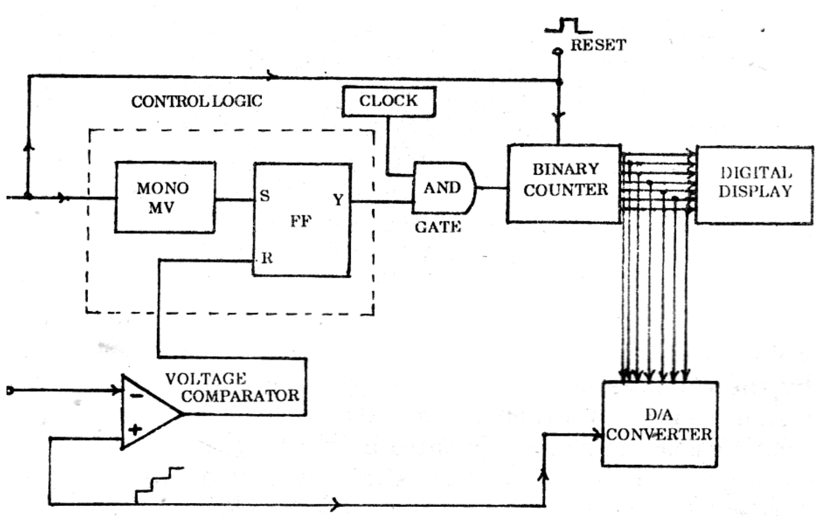
Symbol



Truth Table

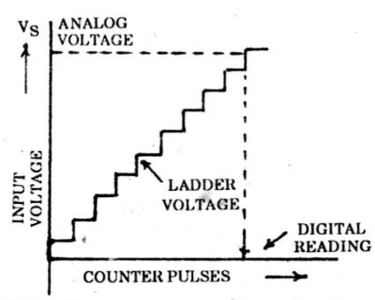
Inputs			Outputs		Comments
J	K	CLK	Q	$\bar{Q}$	Comments
0	0	↑	Q_0	$\bar{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	Q_0	Toggle

Each symbol with truth table 2M

	c) **Ans.**	**i) List any four specifications of DAC.** **Following are the specifications of DAC** **1. Resolution** **2. Linearity** **3. Accuracy** **4. Settling Time** **5. Temperature Sensitivity**	**2M** ***Any four specifications ½ M each***
	c) **Ans.**	**ii) Draw neat block diagram of RAMP ADC and explain its working.** This method of A/D conversion uses a binary counter, to count a continuous train of pulses. The pulses are produced from a clock. They pass through a gate, which is normally closed. It opens only when a start signal is applied to initiate a linear ramp. The gate remains open till the linear ramp voltage reaches a value equal to the input voltage to be measured. The counter thus records a number of clock pulses which is proportional to the input voltage. This method is also called counter method. The fig. shows a schematic diagram of a staircase ramp or counter type A/D converter. This method uses a clock source, a counter and a D/A converter.  	**6M** ***Block diagram 3M*** ***Working 3M***

An analog input is applied to one input of an OP AMP which is used as a voltage comparator. A start or convert pulse is applied to the set input of the flip-flop through a monostable multivibrator (i.e. control logic) and also to the reset input of the binary counter. This pulse resets the binary counter and makes it ready for counting. As the counter resets, output of the D/A converter reduces to zero and thus with positive analog input to the voltage comparator, the output of the comparator goes low, which makes R = 0. The start pulse also triggers the monostable multivibrator, which introduces the desired delay in the action of the other circuits. Thus the output of the monostable multivibrator goes high. This makes S = 1, while R was already made 0.

The RS flip-flop sets and the Y output goes high. The AND gate is enabled & the counter starts the counting the clock pulses. The output of the counter is fed to n D/A converter which produces an analog output in response to the digital signal as its input. This binary output starts increasing continuously with time. The output of the D/A converter also starts increasing in steps. The analog output is a staircase signal as shown in fig.



This D/A output is fed to the reference voltage for the comparator. The staircase signal (i.e. digital output) is compared by the comparator with the analog voltage. So long as the input signal, Vs is greater than the digital output the gate remains enabled and clock pulses are counted by the counter, thus continuously raising the digital output. But as soon as the staircase digital output exceeds the given analog input, the output of the comparator changes from a low to a high level. This makes R = 1, while S is at 0. Thus, the flip-flop resets and Y output goes low. Hence the AND gate is disabled and no clock pulses can now reach the counter. This stops the counting and the binary output of the counter represents the final digital output.

		The staircase ramp or counter method is simple and least expensive. It is faster as compared to dual slope method. It needs longer time for conversion because of the following of the reasons (a) The counter starts after it is reset to zero, (b) The rate of clock pulses also decides the conversion time, and (c) Conversion time is different for analog voltages of different magnitudes.	