17445

MODEL ANSWER

SUMMER– 19 EXAMINATION

Subject Title: Linear Integrated Circuits Subject Code:17445

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

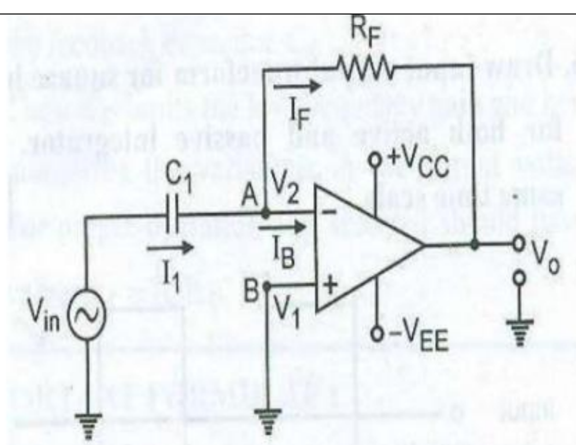
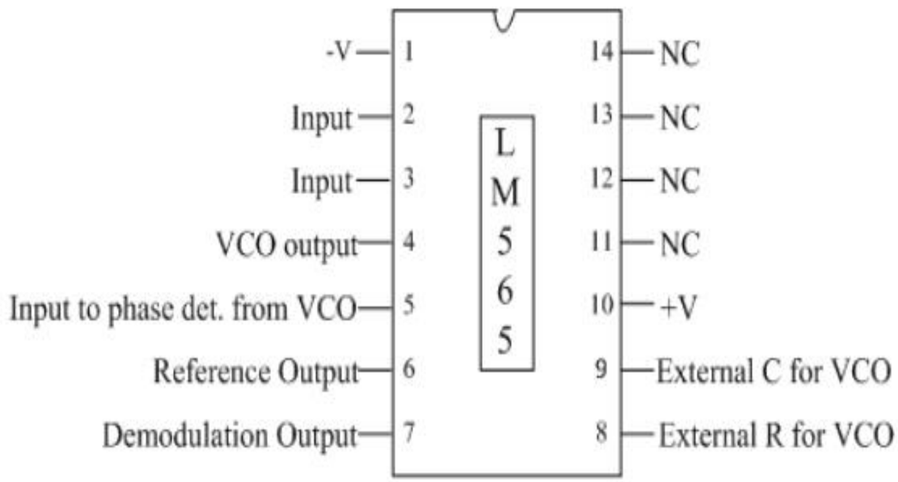
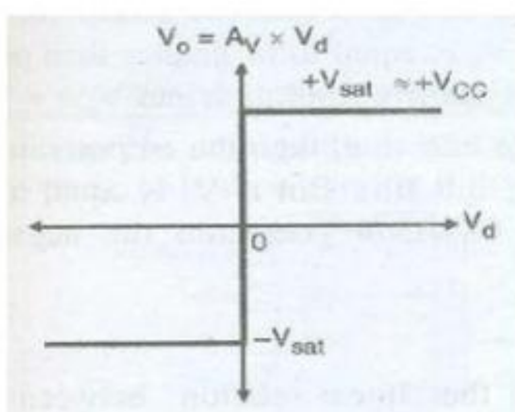
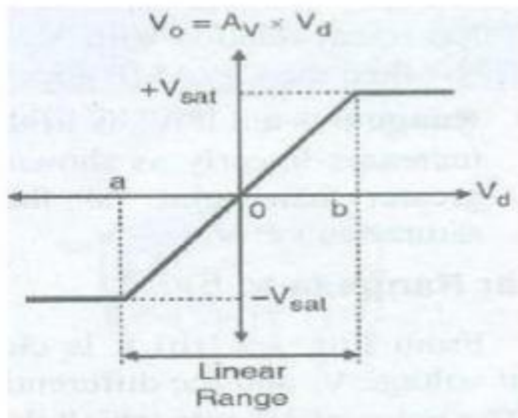
Q. No.	Sub Q.N.	Answers:	Marking Scheme
Q.1		**Attempt any Six:**	**12M**
	i)	**Define :** **1)CMMR** **2) Slew Rate**	**2M**
	Ans:	**CMRR:** It defined as the ratio of differential gain to the common mode gain. **OR** It is the ability of an amplifier to reject the common mode signal. Ideally CMRR= ∞. **Slew Rate-:** It is defined as the maximum rate of change of output voltage per unit time. Ideally Slew Rate = ∞	**1M each**
	ii)	**Draw basic differentiator using op-amp.**	**2M**
	Ans:		**2M**

		Fig: Circuit diagram of Active Differentiator	
	iii)	**List any four specifications of IC LM 324**	**2M**
	Ans:	• Supply voltage =32 V. • Differential i/p voltage= -0.3 V to +32 V. • Operating temp= 00 c to +700 c • Input current =50mA. • Power dissipation = molded DIP=1130mw • Cavity DIP= 1260 mw	**Any 4 Each 1/2M**
	iv)	**Give advantages and applications of instrumentation amplifier (each two).**	**2M**
	Ans:	**Advantages: (Any 2)** **1.** Accurate Testing and Measurement **2.** Stable and Easy to Use **3.** Reliability of the Setup and Results **4.** Highly Scalable **Applications (Any 2)** **1.** Electronic weighing scale **2.** Temperature indicator **3.** Temperature controller **4.** Pressure monitoring and control **5.** Light intensity meter	**½ M each** **½ M each**
	v)	**Define sample period and hold period. With reference to sample and hold circuit.**	**2M**
	Ans:	**Sample period:** The time period during which the voltage across capacitor is equal to input voltage is called sample period. **Hold period:** The time period during which the voltage across capacitor is constant is called Hold period.	**1M** **1M**
	vi)	**Define :** **1)Q- factor** **2) Cut off frequency**	**2M**
	Ans:	**(1) Q Factor of filter:** It is defined as the ratio of Centre frequency to the bandwidth **Q= Fc/ B.W** **(2) Cut off frequency:** It is defined as a frequency where power deliver to load is reduce to 70% of its maximum value.	**1M** **1M**
	vii)	**Give classification of filter.**	**2M**

	Ans:	**1)** On the basis of component used- active and passive filters(LC filers, RC filters) **2)** On the basis of frequency range- AF (audio frequency) and RF (radio frequency) filters. **3)** On the basis of frequency response filters- high pass, low pass, band pass and band reject filters. **4)** On the basis of nature of pass band and stop band- narrow band pass, wide band pass, narrow band reject and wide band reject filters.	
	viii)	**Draw pin diagram of IC 565.**	
	Ans:	 **Pin diagram of IC 565**	**2M**
b		**Attempt any Two of the following:**	**8M**
	i)	**Draw and explain ideal voltage transfer characteristics of op-amp.**	**4M**
	Ans:		**2M**

Ideal voltage transfer characteristics of an ideal OP- AMP



Voltage transfer curve of practical OP- AMP

2M

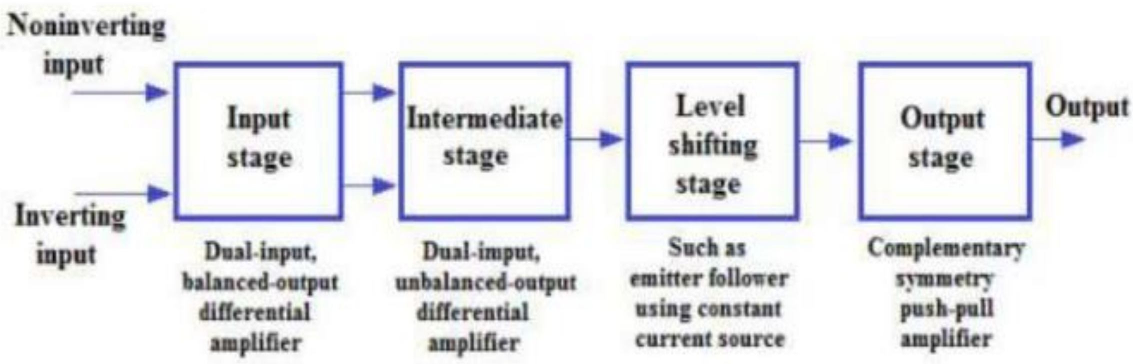
Explanation:-

Output voltage V_0 is plotted against input difference voltage V_{id}, Keeping gain A constant.

1) The output voltage cannot exceed the positive and negative saturation voltages. The saturation voltages are specified by an output voltage, swing rating of the op-amp for giv values of supply voltage.

2) This means that the output voltage is directly proportional to the input difference voltage on until it reaches the saturation voltage and that thereafter output voltage remains constant. Tl curve is called ideal because output offset voltage is assume to be zero.

ii)	**Describe the function of input stage and level shifting stage of op-amp with its block diagram.**	**4M**
Ans:	**(Block Diagram = 2M, Functions = 1M each)**	**2M**



Input Stage – The input stage is a dual input, balanced output differential. This stage provides most of the voltage gain of the OP-AMP and decides the input resistance value R_i.

Level shifting stage – Level shifting stage is used to bring dc level to zero volts with respect to ground.

iii) **Compare ideal And practical parameters of op-amp values w.r.t** — **4M**

1) **PSRR**
2) **Gain bandwidth product**
3) **CMRR**
4) **Input bias current**

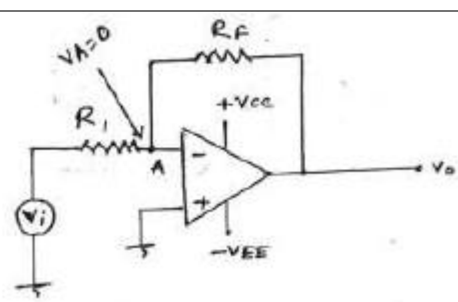
Ans: — **Each Point 1M**

Sr. No	Parameter	Ideal value	Practical value
1	**PSRR**	∞	**150 µV/V**
2	**Gain bandwidth product**	∞	**1 MHz**
3	**CMRR**	∞	**90 dB**
4	**Input bias current**	**0**	**20nA**

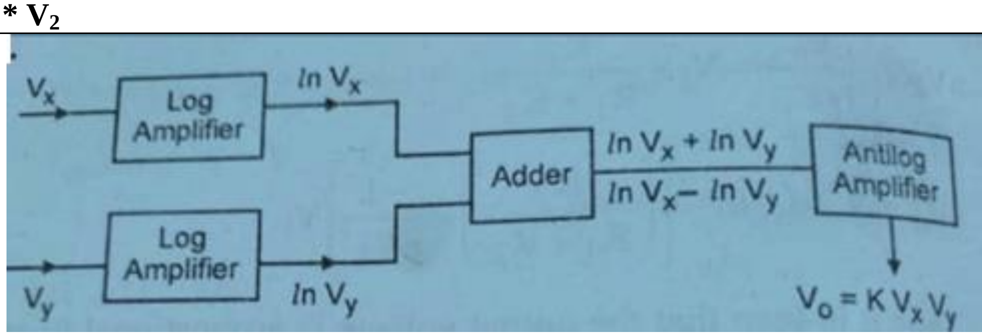
Q.2 **Attempt any Four of the following** — **16M**

a) **State the virtual ground concept in op-amp. Write its mathematical equation.** — **4M**

Ans: — **2M**



Virtual ground concept:-

		• In circuit point V_A is virtual ground. Figure shows inverting amplifier using op-amp. • In this circuit non-inverting terminal is connected to the actual ground. • Due to this potential of inverting terminal become zero. Thus, inverting terminal is not actually connected to the ground. There after its potential is zero. • Thus point V_A is known as virtual ground point. This phenomenon of having zero potential without actually grounding is known as virtual ground concept.	2M
	b)	**Stage the need of signal conditioning and signal processing. List any four applications of instrumentation amplifier.**	**4M**
	Ans:	**Need of signal conditioning and signal processing.** • In an instrumentation system, a transducer is used for sensing various parameters. The output of transducer is an electrical signal proportional to the physical quantity sensed such as pressure, temperature etc. • However the transducer output cannot be used directly as an input to the rest of the instrumentation system. In many applications, the signal needs to be conditioned and processed. • The signal conditioning can be of different types such as rectification, clipping, clamping etc. • Sometimes the input signal needs to undergo certain processing such as integration, differentiation, amplification etc. **Applications (Any 2)** 1)Electronic weighing scale 2) Temperature indicator 3) Temperature controller 4) Pressure monitoring and control 5) Light intensity meter 6) Measurement of flow and thermal conductivity	**2M** **1M each**
	c)	**Draw and describe following op-amp based operation using log and antilog amplifier $V_0 = V_1 * V_2$**	**4M**
	Ans:	 **Description:-** • The two inputs to be multiplied are applied to the log amplifier to provide the outputs log V_X and log V_Y • The inputs are given to adder circuit to provide log Vx +log Vy. The two inputs are applied to antilog amplifier which provides the output **V_O= K*Vx *Vy.**	**2M** **2M**
	d)	**Design and draw low pass filter with cut off frequency 2 KHz and pass band gain of 2.**	**4M**
	Ans:	**Solution:**	**3M**

Pass band Gain (Af) is given by

$$\mathbf{A_f = 1 + R_f / R_1}$$

Here Af = 2
Therefore 2= $1+R_f/R_1$
$R_f/R_1 = 1$
i.e $R_1 = R_f$ (any value of in kΩ can be assumed)
Assume R_1 = 10kΩ, Therefore R_f=10kΩ

Assume C= 0.01 μF (any value of C< 1 μF is valid)

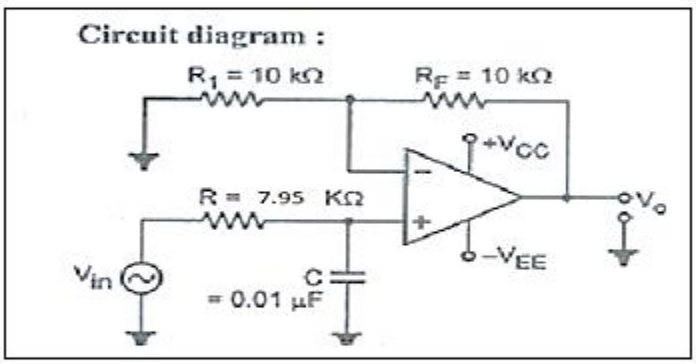
$$\mathbf{F_c = 1/ 2\pi RC.}$$

Given Fc= 2kHz

$$2x\ 10^3 = 1/ 2\pi RC$$
$$R= 1/ 2\pi \text{ x } 2x\ 10^3 \text{ x } 0.01x\ 10^{-6}$$
$$\mathbf{R= 7.95\ k\Omega}$$

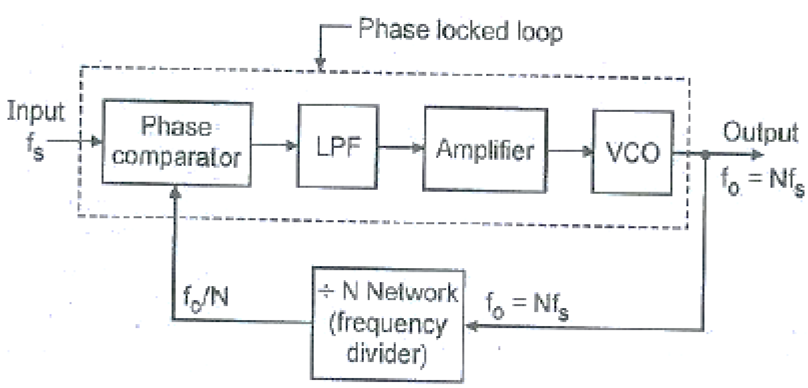
Therefore designed value for low pass filter are R= 7.95 kΩ & C = 0.01x 10^{-6} — **1M**

Designed circuit:-



e) **How the PLL can be used as multiplier?** — **4M**

Ans **Circuit Diagram:** — **2M**



Explanation: — **2M**

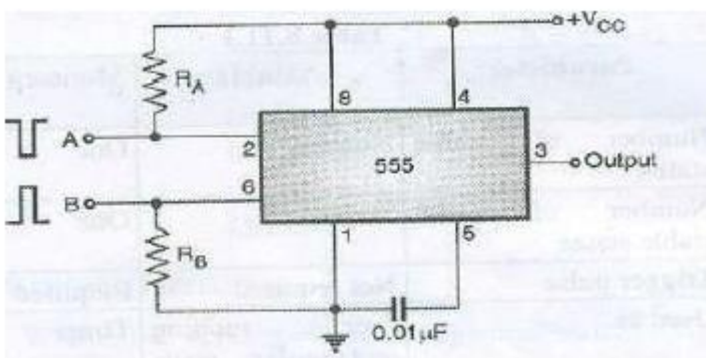
- Figure shows block diagram of a frequency multiplier using PLL.
- A divide by N network is connected externally between the VCO output and phase comparator input.

- Since the output of the divider network is locked to the input frequency fs,
- The VCO actually operates at a frequency which is N times higher than fs.
  Therefore, fo = Nfs
- The multiplying factor can be obtained by proper selection of the scaling factor N.

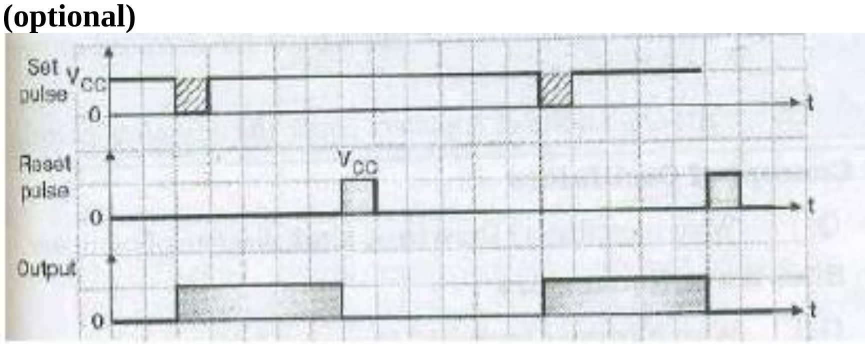
	f)	**Draw and explain bistable multivibrator using IC -555.**	**4M**

Ans:

Diagram of IC-555: **2M**



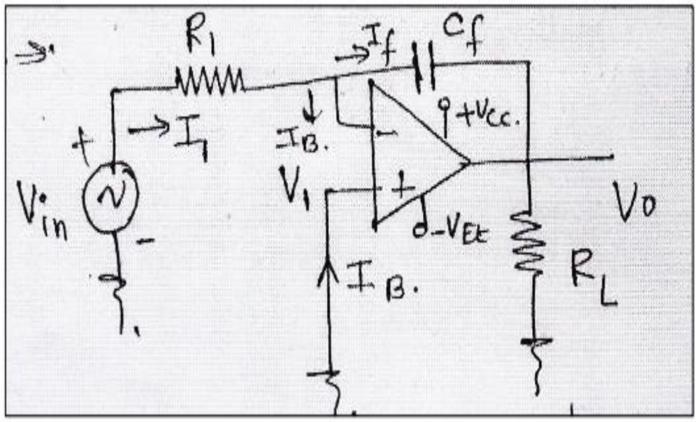
Waveform (optional)



Explanation: **2M**

- A device with two absolute stable states is possible. A Bistable multivibrator is a type of circuit which has two stable states (high and low). It stays in the same state until and unless an external trigger input is applied.
- The trigger pulse will momentarily go low and the output of the timer at pin 3 will become HIGH. The output stays HIGH because there is no input from the threshold pin and the output of the internal comparator (comparator 1) will not go high.
- The pin is internally connected to the RESET terminal of the flip-flop. When this signal goes low for a moment, the flip-flop receives the reset signal and RESETs the flip-flop.

Q.3	**A)**	**Attempt any Four of the following:**	**16M**
	a)	**Draw neat diagram of integrator and obtain expression for output voltage**	**4M**
	Ans:	**Circuit Diagram:**	**2M**



2M

Expression for output Voltage:

According to Kirchhoff's current equation,

$$I_1 = I_B + I_F$$

$$I_1 \approx I_F \ldots\ldots\ldots\ldots\ldots \text{ [} I_B \text{ is negligibly small]}$$

The relationship between current through and voltage across the capacitor is,

$$i_c = C \cdot \frac{dV_c}{dt}.$$

$$\therefore \frac{V_{in} - V_2}{R_1} = C_f \left(\frac{d}{dt} (V_2 - V_o) \right).$$

$V_1 = V_2 \approx 0$, becoze A is very large.

$$\frac{V_{in}}{R_1} = C_F \cdot \frac{d}{dt}(-V_o)$$

∴ The o/p Vtg: can be obtained by integrating both side respect to time,

$$\int_0^t \frac{V_{in}}{R_1} dt = \int_0^t C_f \cdot \frac{d}{dt} (-V_o)\, dt.$$

$$= -C_F(-V_o) + V_o.\Big|_{t=0}.$$

$$\therefore \boxed{V_o = -\frac{1}{R_1 C_f} \int_0^t V_{in}\, dt + c}. \quad \Big| \text{ c is proportional constant.}$$

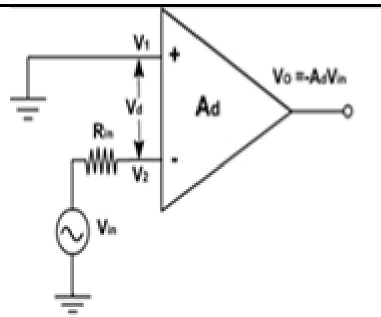
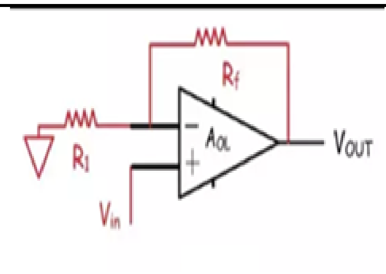
b) **Compare Open loop and Close loop configuration of op-amp on following basis:** **4M**

i) Circuit diagram
ii) Gain
iii) Bandwidth
iv) Application

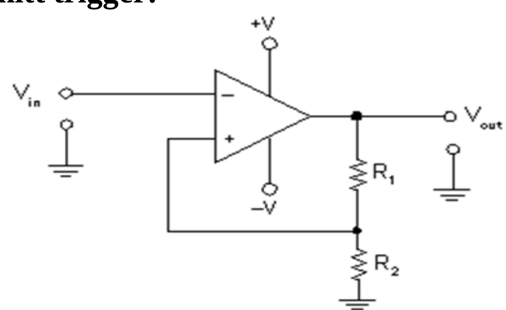
Ans:

Circuit Diagram	Open loop	Close loop

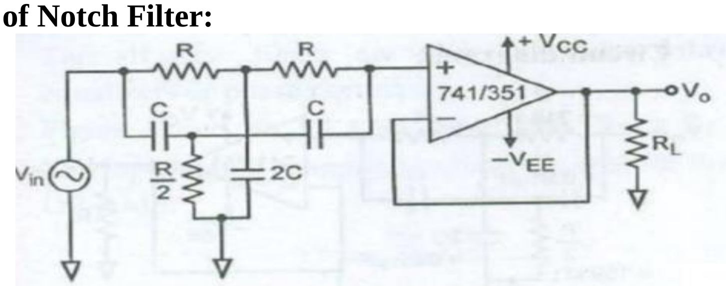
Each point 1M

		
Gain	Voltage gains is very high	Voltage gain is low as compared to open
Bandwidth	Bandwidth is low	Bandwidth is high
Application	Comparator, zero crossing detector	It is used in linear amplifier

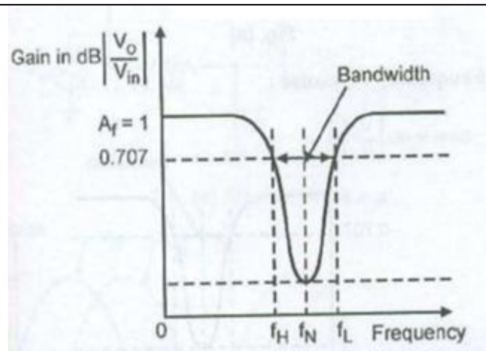
c)	**Draw circuit diagram of Schmitt trigger using op-amp.**	**4M**
Ans:	**Circuit Diagram of Schmitt trigger:**	**4M**



d)	**Draw notch filter with its frequency response**	**4M**
Ans:	**Circuit Diagram of Notch Filter:**	**2M**



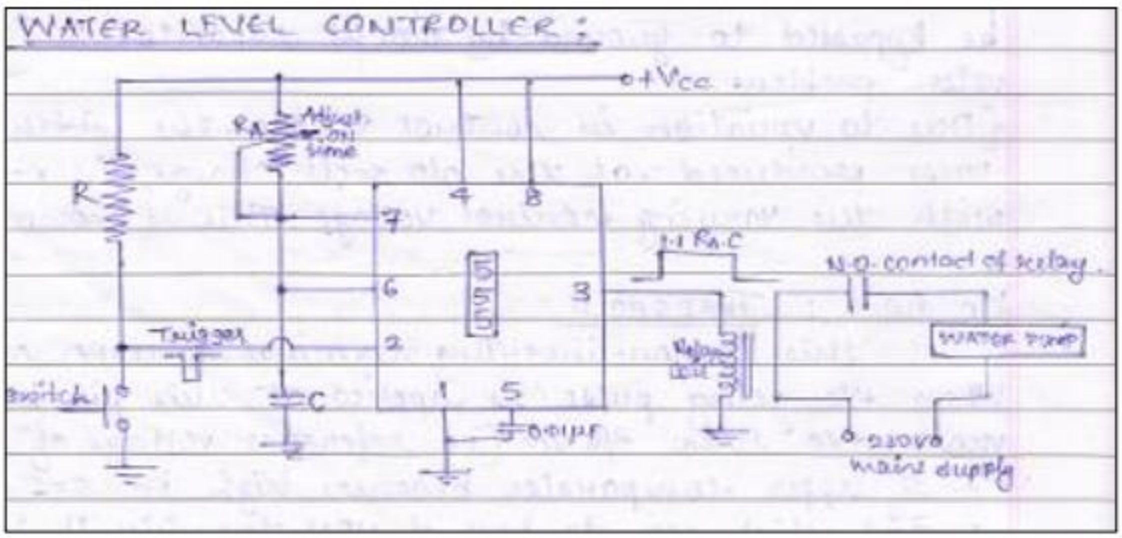
Frequency Response of Notch Filter: **2M**

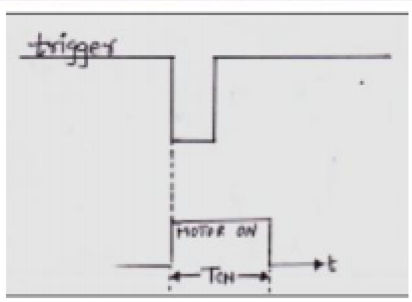


e) **Draw and describe the operation of water level controller using IC 555.** **4M**

Ans: **Water Level Controller using IC555**

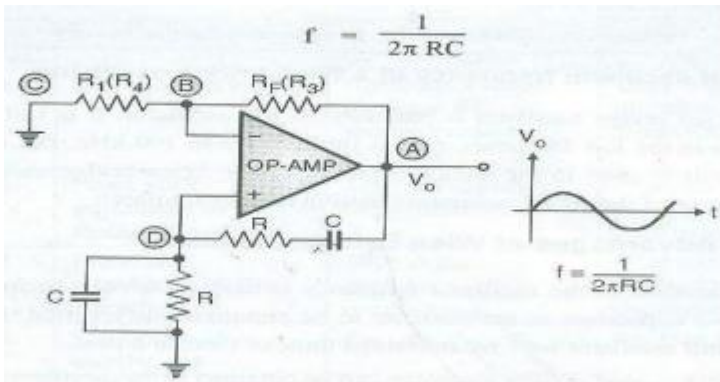
Circuit Diagram: **2M**

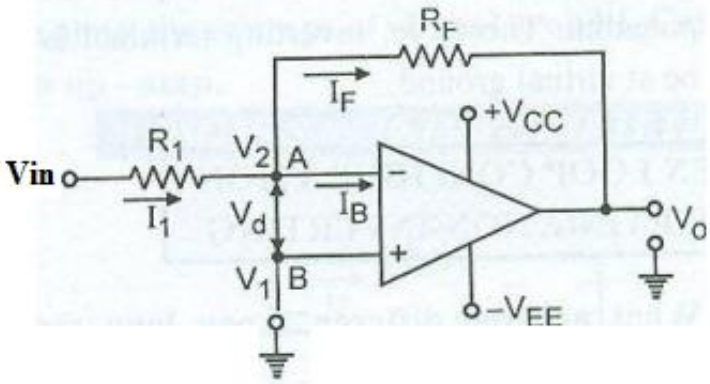




Explanation: **2M**

- In water level controller, IC 555 is used in the monostable multivibrator mode.
- As soon as switch is ON, a trigger pulse is produced & applied to pin no 2 of IC 555 & the output of IC 555 goes high.
- It will remain high for time period $\mathbf{T_{ON} = 1.1\ R_A.C}$
- The high output of IC 555 will energize the relay coil & close the normally open (N.O) contact of the relay to connect the 230 volt ac supply to the water pump motor.

		• The motor will remain ON for the ON time of monostable circuit i. e. $T_{ON}=1.1.R_A.C$	
	f)	**Draw and describe wein bridge oscillator using IC- 741.**	**4M**
	Ans:	**Circuit Diagram:** **Wien Bridge Oscillator:**  **Working:** • The OP- AMP output is applied as an input voltage to the Wien Bridge between points A and C. The output of the Wien Bridge which acts as the feedback network is applied to the OPAMP input between points D and B. • The R and C components in the frequency sensitive arms of the bridge will decide the oscillator frequency. The expression for oscillator frequency is, $F = 1/2\pi RC$ • The resistor R3 gets connected in the feedback path of OP- AMP whereas resistor R4 get connected from the inverting (-) terminal to ground. Thus the amplifier configuration is called as the non-inverting amplifier. • The gain of this configuration is given by: $A= 1+ R_3 /R_4$ • We know that at the oscillating frequency the value of feedback factor is $\beta =1/3$ and the gain should be $A \geq 3$. • Therefore, $(1+ R_3 /R_4) \geq 3$ • Therefore, $R_3 /R_4 \geq 2$ • Thus R_3 should be greater than two times the value of R_4 to ensure sustained oscillations. • The oscillator frequency can be varied by varying both the capacitors (C) simultaneously and the amplifier gain can be changed by changing the value of resistor R_3.	**2M** **2M**
Q.4		**Attempt any FOUR of the following :**	**16M**
	a)	**Draw closed loop inverting amplifier using op-amp derive expression for its gain.**	**4M**
	Ans:	**Inverting Amplifier using Op-Amp:** **Circuit Diagram:**	**2M**



2M

Derivation for gain:

(A) Derivation:

Apply KCL at node 'A', we get,

$I_1 = I_B + I_f$ —— (1)

But, $R_{in} = \infty$

$\therefore I_B = 0$

$\therefore I_1 = I_f$

$\therefore \dfrac{V_{in} - V_2}{R_1} = \dfrac{V_2 - V_o}{R_f}$

According to virtual ground condition,

$V_1 = V_2 = 0$

$\therefore \dfrac{V_{in}}{R_1} = \dfrac{-V_o}{R_f}$

$\therefore \boxed{V_o = -\left(\dfrac{R_f}{R_1}\right) V_{in}}$ —— (2)

$\therefore \boxed{A_v = \dfrac{V_o}{V_{in}} = \dfrac{-R_f}{R_1}}$ —— (3)

where, A_v = closed loop voltage gain

b) **For unity gain amplifier if Vin = +2V. What will be the output voltage? Draw the circuit diagram of unity gain amplifier.** **4M**

Ans: For unity gain amplifier, the input signal is applied at the non-inverting input of op-amp. The gain of the unity gain amplifier is 1 i.e. unity. **2M**

$$\mathbf{A_v = V_0/V_{in}}$$

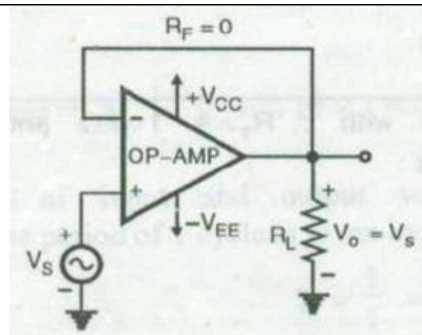
$V_0 = V_{in}$ i.e. output voltage= input voltage

Given:

Vin=+2V

Then V_0= +2V.

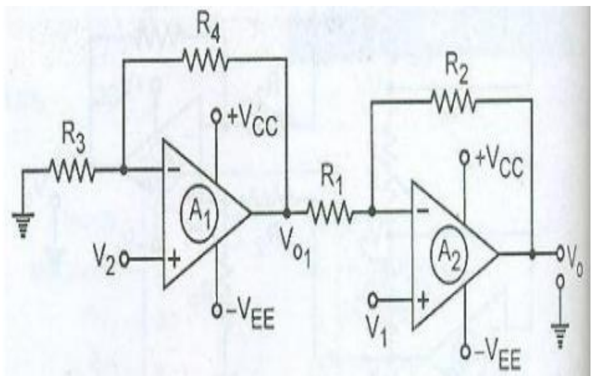
Circuit Diagram: **2M**



c) **Draw circuit and derive equation of two op-amp instrumentation amplifier.** **4M**

Ans: **Two Op-Amp Instrumentation Amplifier:** **2M**

Circuit Diagram:



Derivation: **2M**

Op amp A_1 is in non-inverting mode,

$$\therefore V_{o1} = \left(1+\frac{R_4}{R_3}\right) V_2 \quad \text{— (1)}$$

As op-amp A_2 is a differential amplifier or subtractor

$$\therefore V_o = V'_{o1} + V''_{o1}$$

$$\therefore V'_{o1} = -\frac{R_2}{R_1} \times V_{o1}$$

$$V''_{o1} = \left(1+\frac{R_2}{R_1}\right) V_1$$

$$\therefore V_o = -\frac{R_2}{R_1} V_{o1} + \left(1+\frac{R_2}{R_1}\right) V_1 \quad \text{— (2)}$$

Putting equation (1) & (2) we get,

$$V_o = -\frac{R_2}{R_1}\left(1+\frac{R_4}{R_3}\right) V_2 + \left(1+\frac{R_2}{R_1}\right) V_1$$

Assuming,

$R_4 = R_1$, $R_3 = R_2$

$$\therefore V_o = -\frac{R_2}{R_1}\left(1+\frac{R_1}{R_2}\right) V_2 + \left(1+\frac{R_2}{R_1}\right) V_1$$

$$\therefore V_o = -\left(1+\frac{R_2}{R_1}\right) V_2 + \left(1+\frac{R_2}{R_1}\right) V_1$$

$$\therefore \boxed{V_o = \left(1+\frac{R_2}{R_1}\right)(V_1 - V_2)}$$

$$\boxed{\text{Gain} = A_V = \frac{V_o}{V_1 - V_2} = 1+\frac{R_2}{R_1}}$$

d) **Draw the second order high pass filter and describe its operation.** **4M**

Ans: **Second Order High Pass Filter:**

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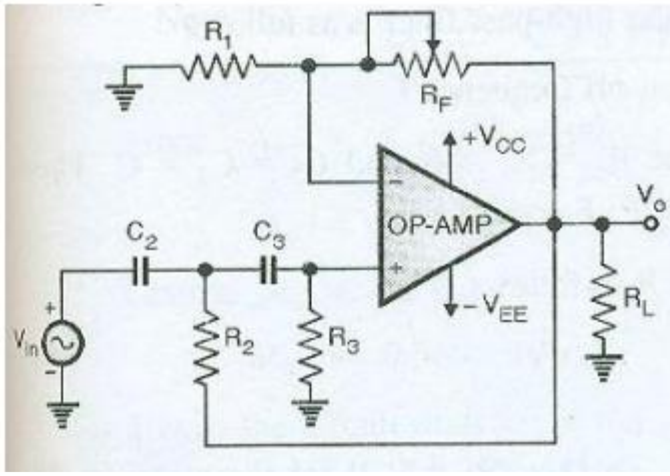
Circuit Diagram:



Description:

- The resistors R_1 and R_F will decide the gain of the high pass filter. The gain can be made variable by keeping RF variable.

The cut-off frequency f_c is determined by R_2, R_3, C_2 and C_3 as follows:

$$f_c = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

- The voltage gain magnitude is given by ,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{VF}}{\sqrt{1 + (f_c / F)^4}}$$

$$A_{VF} = 1 + \frac{R_F}{R_1} = \text{Passband gain of the filter.}$$

- The frequency response of the second order filter. It shows that the gain increases at a rate of 40 db/ decade in the attenuation band. This is doubled the rate of first order filter. This makes the frequency the frequency response sharper.
- The second order filters are important because they can be used for designing the higher order filters.

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2M

2M

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<tr><td></td><td>e)</td><td>

Draw transfer characteristics of PLL.
Define:
i) Lock range and
ii) Capture range of PLL.

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<tr><td></td><td>Ans:</td><td>

Transfer Characteristics of PLL:

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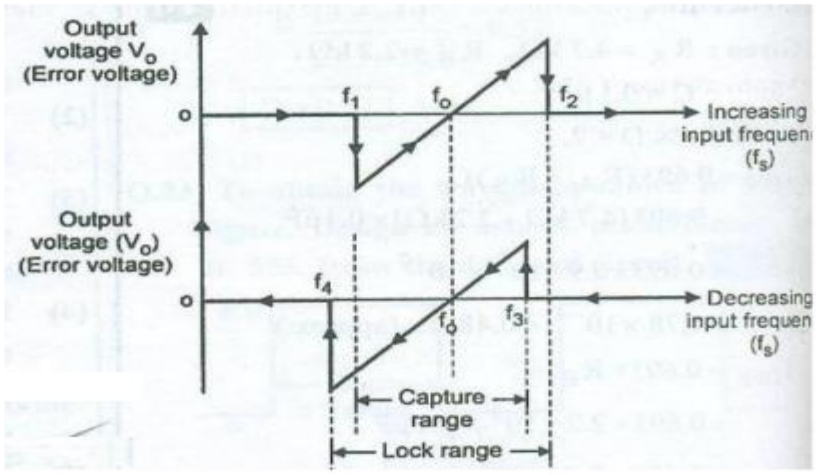
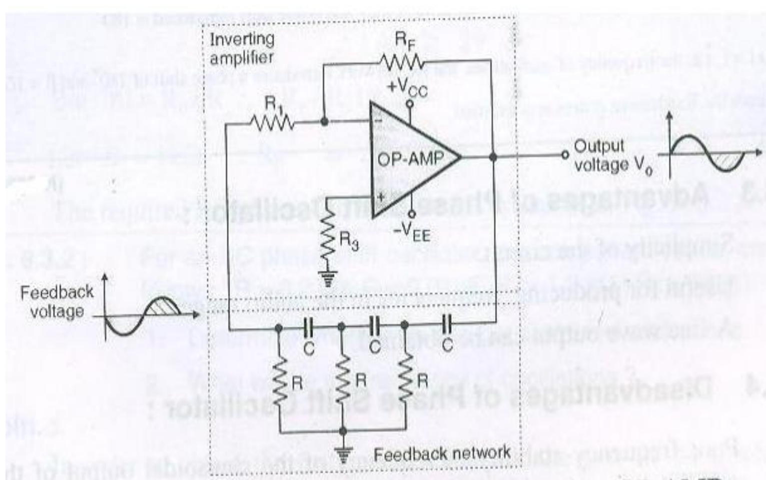
			1M
		Lock range: The range of frequencies over which the PLL can maintain the phase lock with the incoming signal Fs, is defined as the lock in range. **Lock range = F_L = 2 Δ F_L** Where $F_L = 8\ F_0 / V$	1M
		Capture range : It is defined as the range of frequencies over which the PLL can acquire lock with the input signal Fs **Capture range = 2 Δ F_C** Where $F_C = F_L / (2\pi * 3.6 * 103 * C)$	
	f)	**Draw and Explain working of phase shift oscillator using IC-741.**	4M
	Ans:	**Phase Shift Oscillator using IC-741:** **Circuit Diagram:** 	2M
		Explanation : • The Op- Amp is used as an inverting amplifier. Therefore it introduces a phase shift f180^0 between its input and output.	2M

- The output of the inverting amplifier is applied at the input of the RC phase shift network. This network attenuates the signal at its input and feeds it to the amplifier input. The level of attenuation is decided by the feedback factor β.
- The gain of the inverting amplifier is decided by the values of R_F and R_1. This gain is adjusted in such a way that the product $|A\beta|$ is slightly greater than 1.
- It can be proved that the value of feedback factor β at the frequency of oscillations is $\beta = 1/29$. For sustained oscillations, the loop gain $|A\beta| \geq 1$. Therefore, in order to make the loop gain $|A\beta| \geq 1$, the gain of the inverting amplifier A should be greater than or equal to 29.
- Gain of the inverting amplifier is given by,

$|A| = R_F / R_1$ Therefore, $R_F / R_1 \geq 29$ or $R_F \geq 29R_1$

- These values of R_F and R_1 will insure sustained oscillations.

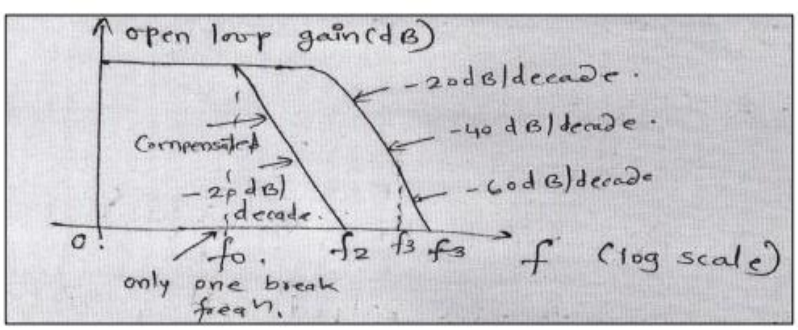
The expression for frequency of oscillations of an RC phase shift oscillator using OPAMP is given by

$$F_o = 1/ 2\pi\sqrt{6}\, RC$$

Q.5		Attempt any FOUR of the following :	16M
	a)	**With neat diagram explain the concept of frequency compensation and offset nulling**	4M
	Ans:	**Frequency compensation:**	2M

In practice all possible efforts are made to convert the multiple break frequency op-amp (uncompensated) into the single break frequency of op-amp using some technique, This technique, is called as frequency compensation.

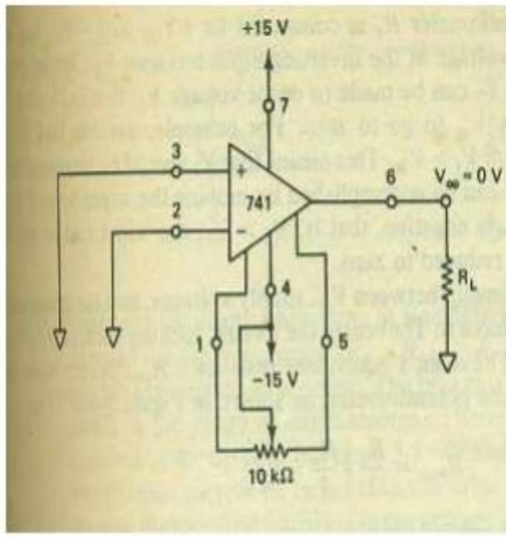
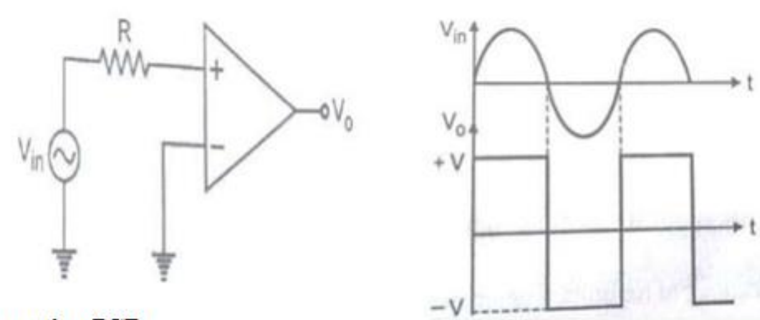
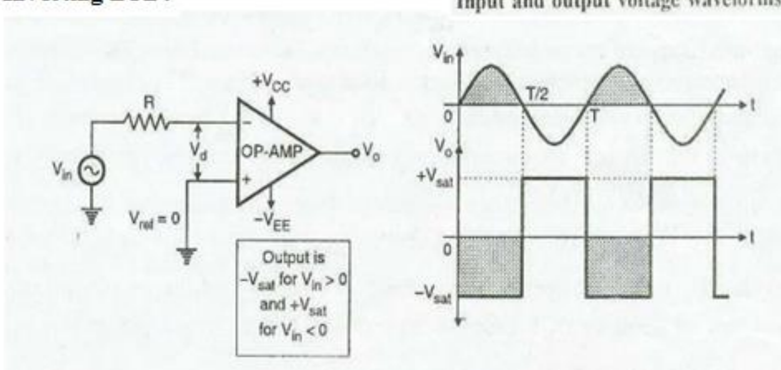
Thus the technique of modifying the loop gain frequency response of the system op-amp from multiple break frequency to the single break frequency to ensure stability is called as frequency compensation



Offset nulling: (2M)

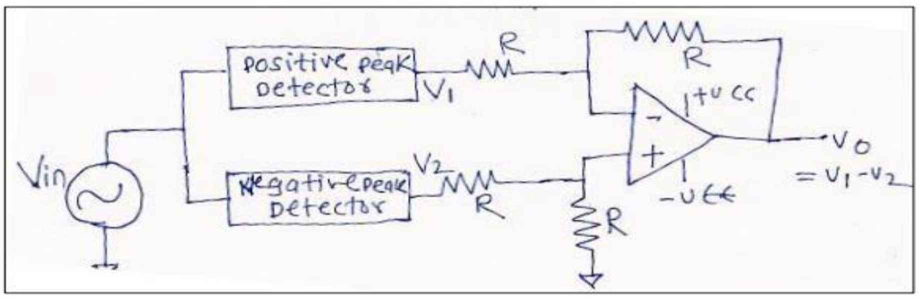
An offset voltage exists because a real op-amp can't be ideal. There will always be some unintended asymmetries due to random variation in manufacturing. In all cases, there are op-amp designs that can minimize these errors, but usually at the expense of some other parameter, like cost. It can be safely ignored in AC applications, where this offset will be ignored by the AC coupling. It becomes more important in DC applications, especially amplifiers, since this DC error will be amplified by the next stage.

An offset voltage exists because a real omp-amp can't be ideal.

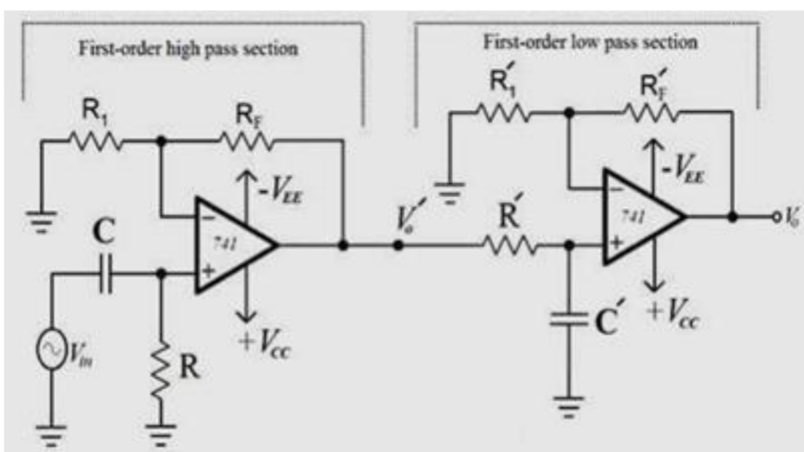
		A 10kΩ potentiometer is placed across offset null pins 1 and 5 and a wiper be connected to the negative supply pin 4. Adjustment of this pot will null the output. By varying the position of the wiper on the 10kΩ potentiometer remove the mismatch between inverting and non-inverting input terminals of the op-amp. Adjust the wiper until the output offset voltage is reduced to zero. 	
	b)	**Draw circuit diagram and input output waveform of inverting ZCD and non- inverting ZCD (Zero Crossing Detector).**	**4M**
	Ans:	**Non Inverting ZCD :-**  Input and output voltage waveforms **Inverting ZCD:-**  Input and output voltage waveforms	**4M**

	c)	**State the need of peak to peak detector and draw its circuit diagram.**	**4M**
	Ans:	**Need of peak detector**: It is used to determine or detect the highest or maximum peak value of the input signal applied. OR It is used to determine the positive or negative peak or The difference between the two peaks of the input signal.	**2M** **2M**

Circuit Diagram:



	d)	**Describe the operation of wide band pass filter with the help of circuit diagram.**	**4M**
	Ans:	**Circuit Diagram Operation of wide band pass filter**	**2M**



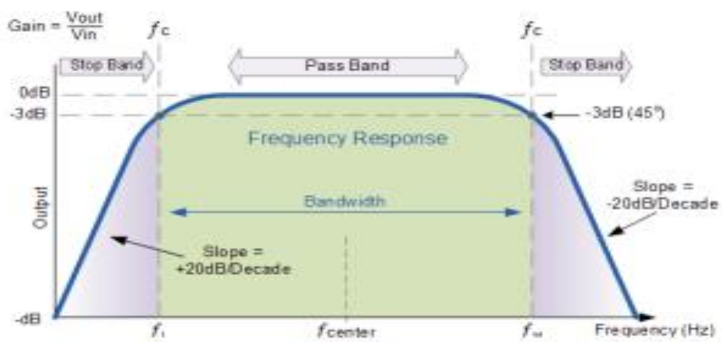
OPERATION: **2M**

- A band-pass filter passes all signals within a lower-frequency limit and an upper-frequency limit and rejects all other frequencies that are outside this specified band.
- This type of filter has a maximum gain at a resonant frequency.
- A band pass filter is the combination of high pass and low pass filter combination
- It has a pass band between two cut off frequency F_H and F_L such that $F_H > F_L$ Any input frequency outside this pass band is attenuated.
- There are two types of band pass filters wide band pass and narrow band pass.
- If the quality factor Q < 10 and Q > 10 then it would be wide band pass and narrow band pass filter respectively.

- The relationship between Q, the 3-dB bandwidth and the center frequency face is given by,

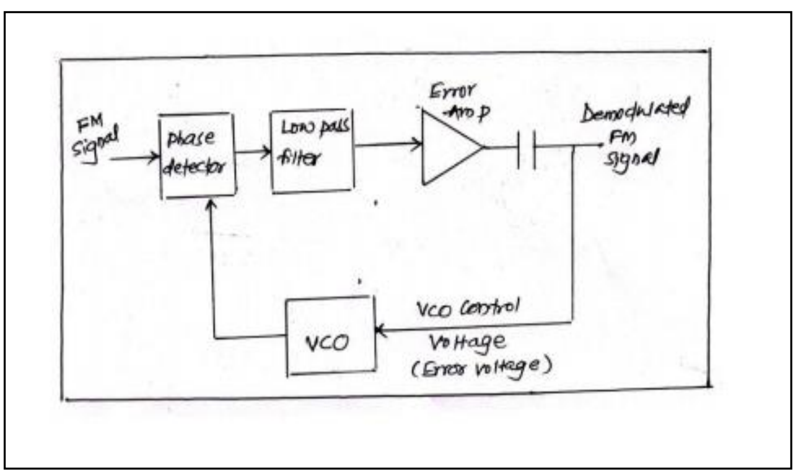
$$Q = \frac{f_C}{BW} = \frac{f_C}{f_H - f_L}$$

$$\text{Where, center frequency } f_C = \sqrt{f_H - f_L}$$



e) **Describe with the help of block diagram the operation of FM demodulator using PLL.** **4M**

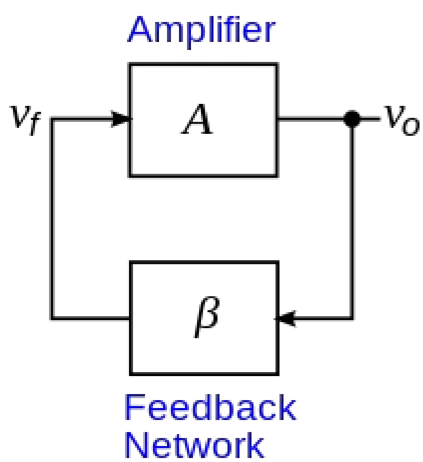
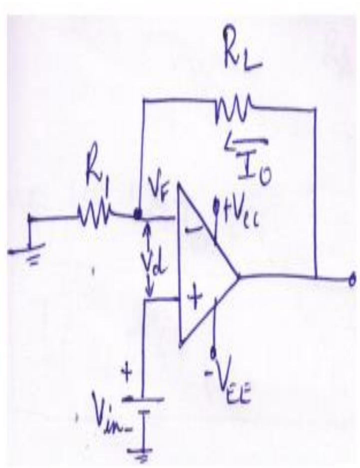
Ans: **Block Diagram:** **2M**

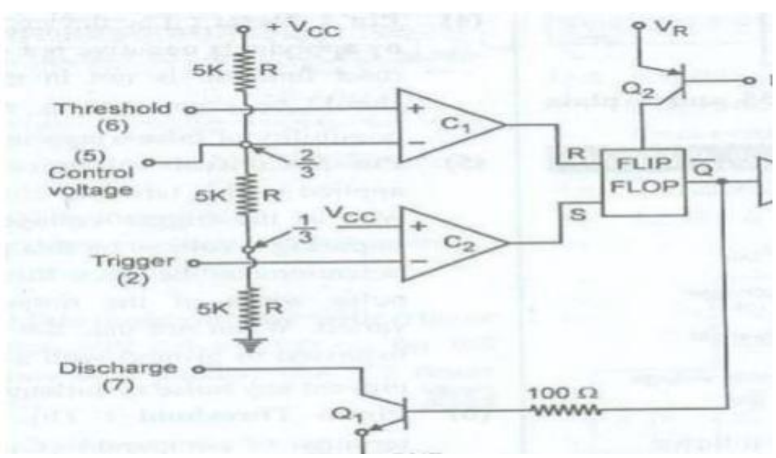


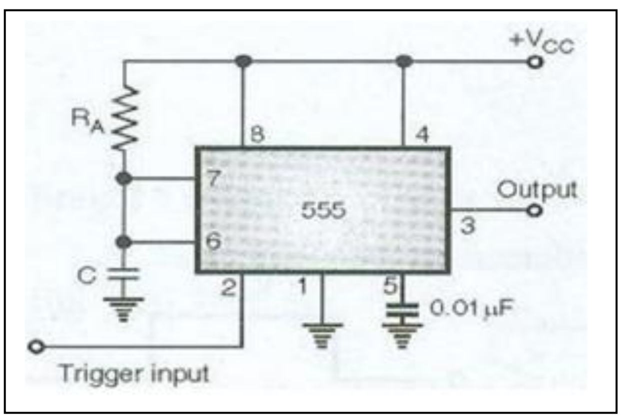
2M

Operation:

- The FM signal which is to be demodulated is applied at the input of the PLL.
- The PLL is locked to the FM.
- The error voltage produced at the output of the amplifier is proportional to the deviation of the input frequency from the center frequency of FM. Thus, The at component of the error voltage represents the modulating signal. Thus at the error amplifies output we get demodulated.
- The FM demodulator using PLL ensures a high Linearity, between the instantaneous input frequency and VCO control voltage(error amplifier output)

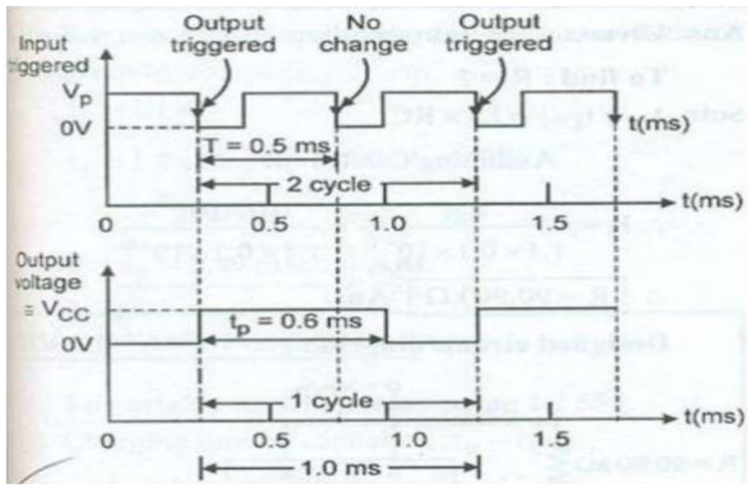
	f)	**State the principle of oscillator. Write its necessity conditions.**	**4M**
	Ans:	**Principle of oscillator:-** • An electronic oscillator is an electronic circuit that produces a periodic, oscillating electronic signal, often a sine wave or a square wave. • Oscillators convert direct current (DC) from a power supply to alternating current (AC) signal and works with positive feedback principle. **Necessity conditions:-** 1. The magnitude of the product of open loop gain of the amplifier and the magnitude of the feedback factor is unity, i.e., $\lvert\beta A\rvert=1$ where *A* is the gain of the amplifying element in the circuit and β is the feedback Network. 2. The total phase shift around the loop is 00 or integral multiples of 2π.  	**2M** **2M**
Q.6		**Attempt any FOUR of the following :**	**16TM**
	a)	**Draw and explain the circuit of V to I converter with floating load using op-amp.**	**4M**
	Ans:	**Circuit Diagram**  The load resistor R_2 is floating in, not connected to ground. The input voltage is applied to the non-inverting input terminal and the feedback voltage	**2M** **2M**

		across R_1 drives the inverting terminal. Writing KVL to the input loop, $V_{in} = V_{id} + V_F$ But $V_{id} = 0$ v since A is very large, $V_{in} = V_F$ $V_{in} = R_1 I_0$ **OR** $I_0 = \frac{Vin}{R1}$ Output current is proportional to input voltage. Input voltage is converted into an output current.	
	b)	**Explain how active filter is better than passive filter.**	**4M**
	Ans:	**Advantages of active filters over passive filters:-** **1.** Active filters have flexibility in gain and frequency adjustments. **2**. They provide pass band gain. **3.** Because of high input resistance and low output resistance, they do not have loading problems. **4.** The components required for active filters are of smaller size. **5.** They do not exhibit any insertion loss. **6.** Due to absence of inductors and easy availability of variety of cheaper op-amps active filters are cheaper. **7.** They allow for interstate isolation and control of input and output impedance.	**Any 4 Each 1M**
	c)	**Draw block diagram of IC 555. Explain the use of pin 2 and 6.**	**4M**
	Ans:	**(Block Diagram= 2M, Explanation= 2M)** **Block Diagram:**  **(Pin no 2)Trigger:-** This is the inverting terminal of comparator C2 which monitors the voltage across the external capacitor. When the voltage at this pin goes below or equal to 1/3 VCC, the output of comparator C2 goes low which in turn switches the output of the timer to high. **(Pin no 6)Threshold:-** This is non- inverting terminal of comparator C1 which monitors the	

		voltage across the external capacitor. When the voltage at this pin is greater than or equal to 2/3 VCC, the output of comparator C1 goes high which in turn switches the output of the timer low.	
	d)	**Describe the operation of phase detector and role of VCO in PLL.**	**4M**
	Ans:	**Voltage controlled oscillator(VCO):** • The control voltage V_C is applied at the input of a VCO. • The output frequency of VCO is directly proportional to the dc control voltage $V_{C.}$ The VCO frequency f_0 is compared with the input frequency f_{in} by the phase detector and it(VCO frequency) is adjusted continuously until it is equal to the input frequency f_{in} $f_0=f_{in}$ • The voltage controlled oscillator (VCO) is a free running multivibrator and operates at frequency f_0 .Which is determined by external timing capacitor and external resistor. • The operating frequency can be shifted on either side by applying a dc control voltage V_C externally. **Phase detector or phase comparator:** • The two points to a phase detector or comparator are the input voltage V_S at frequency $_S$and the feedback voltage from a voltage controlled oscillator(VCO) at the frequency $F_{0.}$ • The phase detector compares these two signals and produces a dc voltage $\mathbf{V_e}$which is proportional to the phase difference between F_{in} and $F_{0.}$ The output voltage of the phase detector is called as error voltage. This error voltage is then applied to a low pass filter.	**2M** **2M**
	e)	**How monostable multivibrator can be used as frequency divider?**	**4M**
	Ans:	**Circuit Diagram:**  **Explanation:** • The Monostable multivibrator can be used as frequency divider by adjusting the length of the timing cycle t_o with respect to time period T of the trigger input signal applied to pin 2. • To use the Monostable multivibrator as divide by 2 circuit, the timing interval t_o must be slightly larger than the time period T of the trigger input signal as shown in figure above	**2M** **2M**

- By the same concept, to use the Monostable multivibrator as divider by 3 circuit, t_o most be slightly larger than twice the period of the input trigger signal and so on.
- The frequency divider application is possible because the Monostable multivibrator cannot be triggered during the timing cycle.

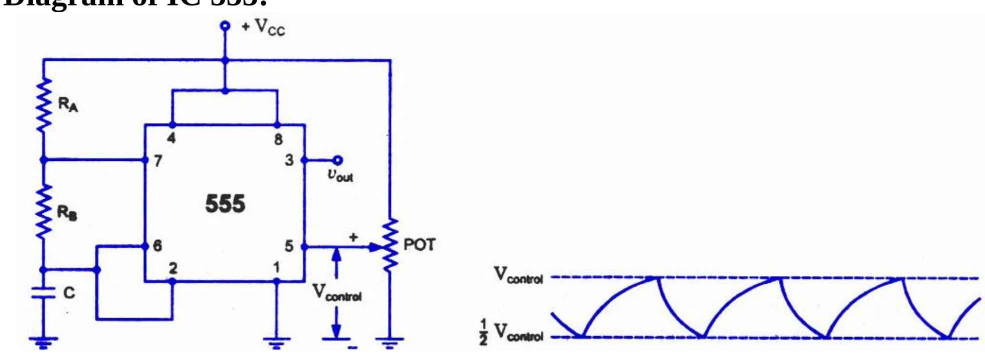
(Waveform Optional)



Waveforms as frequency divider

f) **State the working of IC 555 as a voltage controlled oscillator (VCO).** **4M**

Ans: **Circuit Diagram of IC 555:** **2M**



Working :-

- The circuit is also called as a **voltage-to-frequency converter** because the output frequency can be changed by changing the input voltage.
- pin 5 terminal is voltage control terminal and its function is to control the threshold and trigger levels. Normally, the control voltage is +2/3V_{CC} because of the internal voltage divider.
- However, an external voltage can be applied to this terminal directly or through a pot, as illustrated in figure, and by adjusting the pot, control voltage can be varied. A Voltage across the timing capacitor is varies between +$V_{control}$ and ½ $V_{control}$.
- If control voltage is increased, the capacitor takes a longer to charge and discharge; the frequency, therefore, decreases.

2M

		• Thus the frequency can be changed by changing the control voltage.	