17659

21718

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory****.*
(2) Illustrate your answers with neat sketches ***wherever*** *necessary.*
(3) Figures to the ***right*** *indicate* ***full*** *marks.*
(4) Assume suitable data, if ***necessary****.*
(5) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. A) Attempt **any three** : **12**

i) Draw the AND gate and NOR gate using CMOS.
ii) Write VHDL code for 3-bit up counter.
iii) What is instantiation in VHDL ? Write one example.
iv) Draw the diagram of Moore machine and Mealy machine. Write expression for its output.

B) Attempt **any one** : **8**

i) Write any six features of spartan-3.
ii) Draw the diagram of Cz process for water fabrication. List the steps involved in water fabrication.

2. Attempt **any four** of the following : **(4×4=16)**

a) Design a mealy sequence detector circuit for detecting sequence 101 using J-K flipflop.
b) Explain how to estimate the channel resistance of CMOS transistor.
c) Compare BJT and CMOS technology.
d) Write the syntax of entity and architecture in VHDL programming.
e) Explain the sharing of complex operators.
f) Write the VHDL code for full adder.

3. Attempt **any four** of the following : **(4×4=16)**

a) State the any four features of VHDL.
b) Design the boolean expression r = (A + B). C using CMOS logic.
c) Compare synchronous and asynchronous sequential circuits. (any four points).
d) Write the VHDL code for 3 : 8 decoder.
e) Explain efficient coding styles.
f) Compare FPGA and CPLD.

P.T.O.

Marks

4. Attempt **any four** of the following : **(4×4=16)**

a) Write two advantages and disadvantages of VHDL.

b) Define the following terms related to fabrication process.

i) Oxidation

ii) Ion-implantation

iii) Diffusion

iv) Deposition.

c) Write the VHDL code for D-flipflop.

d) Design parity generator using moore machine.

e) Compare hardware and software description language.

f) Draw FPGA's configurable logic block diagram and write the function of it.

5. Attempt **any four** of the following : **(4×4=16)**

a) State the applications of test bench and write down the typical format of test bench.

b) Design 2-bit sequential counter using mealy machine.

c) Explain n-well CMOS fabrication process with neat sketches.

d) List the datatypes used in HDL and explain.

e) Explain event scheduling.

f) Draw the design flow of ASIC and explain.

6. Attempt **any four** of the following : **(4×4=16)**

a) Write the VHDL code for 3-bit right shift register.

b) Draw HDL design flow for synthesis and explain.

c) Explain CMOS transmission gate with neat diagram.

d) Draw the architecture of XC9500 CPLD.

e) Explain event based simulator.

f) Differentiate between Xilinx and Atmel series architecture of CPLD (four points).