17659

11920

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Assume suitable data, if necessary.

(6) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. Solve any FIVE : **20**

(a) List the types of FSM. Draw labelled diagram for each.

(b) Define the following terms :

(i) Metastability

(ii) Noise margin

(iii) Fan out

(iv) Skew

(c) Explain (i) Event scheduling (ii) zero modeling.

(d) Design the NAND Gate using CMOS and write its truth table.

(e) Explain the HDL terms entity and Architecture with syntax.

(f) Compare Software and Hardware description language.

(g) Write the VHDL code to implement 2 I/P NOR gate.

2. Solve any FOUR : **16**

(a) Write a VHDL code for 3 : 8 decoder.

(b) Write a VHDL code for 16 : 1 MUX.

(c) Explain the main steps carried out in a p-well process.

(d) Draw state diagram of a sequence detector to detect a sequence of '1101'.

(e) Explain different Data Types in VHDL.

(f) Explain the silicon gate process for N-MOS transistor.

3. Solve any FOUR : **16**

(a) Write VHDL code for four bit binary to array code converter.

(b) Explain different types of sequential constructs in VHDL.

(c) State the features of VHDL (any four).

(d) Describe oxidation in CMOS fabrication.

(e) Explain resistance estimation of MOSFET.

(f) Design a CMOS logic gate for the function

$f = \overline{A \cdot B + C \cdot D}$

4. Solve any FOUR : **4 × 4 = 16**

(a) Draw and explain design flow of ASIC.

(b) Compare Moore and Melay type of state machine (any four points)

(c) Write steps for designing clocked synchronous state machine.

(d) Compare BJT with CMOS.

(e) Explain architecture of Xilinx 9500 family CPLD.

(f) Explain sharing of complex operator in HDL.

5. Solve any TWO : **16**

(a) List the steps carried out in the twin tub fabrication. Also state the advantages.

(b) Explain simulation deltas with an example.

(c) Draw and explain basic architecture of Spartan-3 FPGA series.

6. Solve any TWO : **16**

(a) Draw the functional blocks of XC4000 FPGA series and differentiate between FPGA and CPLD (any four points).

(b) Explain HDL design flow for synthesis in detail.

(c) Write test bent for 2 input AND Gate and state applications of test bench.
