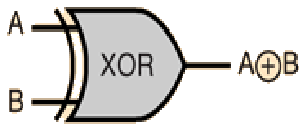
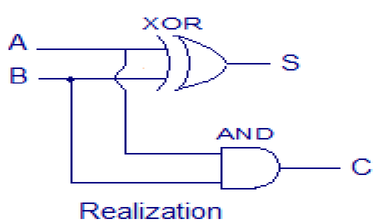
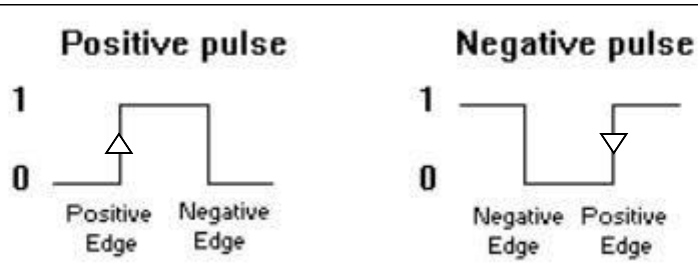
SUMMER– 18 EXAMINATION

Subject Name: Principles of Digital Techniques **Model Answer** Subject Code: **17320**

Important Instructions to examiners:

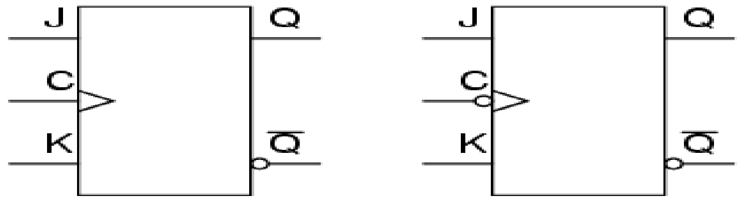
1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q. N.	Answers	Marking Scheme
1	a	**Attempt any six:**	**12-Total Marks**
	i	Convert (AC) H into binary and octal.	2M
	Ans:	1) $(AC)_H = (?)_2 = (?)_8$ $= (1010\ 1100)_2$ 2) $(AC)_H = (10\ 101\ 100)_2 = (254)_8$ 2 5 4	1M 1M
	ii	Draw symbol, Truth table and logical equation of Ex-OR gate.	2M
	Ans:	 **Symbol**	½ M ½ M

		Logical equation: Y= $A\bar{B} + \bar{A}B$ (truth table below) Truth Table	1M
	iii	Draw logic diagram of half adder and write its logical equation.	2M
	Ans:	Logic Diagram of Half adder:  Logic Equation: S= $A\bar{B} + \bar{A}B$ C= A.B	Diagram ½ M XOR(S) ½ M AND(C) Logic Equation ½ M ½ M
	iv	Draw symbol of positive edge triggered and negative.	2M
	Ans:	 OR	1 M For positive edge trigger and 1 M for negative edge trigger (Pulse or Flip Flop)

A	B	Out
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table

			
	v	Specify the function of — 1) IC 74245: 2) IC 74151:	2M
	Ans:	**1) IC 74245: Octal Bus Transceiver** a) It is octal bidirectional buffer IC b) It is used as a driver for the data bus c) Total 16 bus drivers, 8 for each direction with tristate output d) The direction of data flow is controlled by DIR pin **2) IC 74151: 8:1 Multiplexer** a) It has 8 inputs and 1 output b) 2^N =8, N=3 select lines, whose bit combination determines which combination is selected at output	1M (Minimum One function) 1M (Minimum One function)
	vi	What is Flash memory?	2M
	Ans:	1. Flash Memory is nonvolatile RAM memory 2. It can be Electrically erased and reprogrammed 3. Flash memory can be written into blocks size rather than byte. It is easy to update. 4. It is faster than EEPROM as EEPROM edit the data at Byte level. 5. As large block of data can be erased at one time (or flash)thus called as flash	(Any 4 points) ½ M each

		memory. 6. Features: High speed, low operating voltage and low power consumption 7. Applications: 1. Cellular phone 2. Digital camera's embedded controller.	
	vii	Write applications of DAC and ADC.	2M
	Ans:	1. In Process control system 2. Low power converter for remote data acquisition 3. Battery operated equipment 4. Acquisition of analog values in automotive, audio and TV application (Any suitable relevant application should be considered)	1 M(Any two)
	viii	List advantages of TTL logic family.	2M
	Ans:	1. Low propagation delay, hence TTL circuits are fast. 2. Power dissipation is independent of Frequency. 3. No latch ups. 4. TTL is compatible to other logic families. 5. High current sourcing and sinking capabilities. (Relevant advantages should be considered)	½ M each (any 4)
	b	**Attempt any TWO:**	**08-Total Marks**
	i	Perform binary subtraction using 2's complement method. $(12)_{10}$ — $(08)_{10}$	4M

	Ans:	1. Finding equivalent binary for $(12)_{10}$ and $(08)_{10}$ $(12)_{10} = (1100)_2$ $(08)_{10} = (1000)_2$ 2. Taking 1's complement of $(1000)_2$ 1's complement of 1000 => 0 1 1 1 + 1 2's complement 1 0 0 0 3. Adding $(12)_{10}$ and 2's complement of $(08)_{10}$ 1 1 0 0 + 1 0 0 0 carry → $\boxed{1}$ 0 1 0 0 4. If carry comes discard carry 5. Answer is positive and in real form $=(0100)_2 = (04)_{10}$	1M 1M 1M 1M
	ii	Convert following expression into canonical SOP form Y = A + BC + ABC	4M
	Ans:	Y = A + BC + ABC $= A.1.1 + BC.1 + ABC$ Multiplying each sum by missing term $= A(B+\bar{B})(C+\bar{C}) + BC(A+\bar{A}) + ABC$ As $(B+\bar{B}) = 1$	1M For each step

		$= ABC + A\bar{B}C + AB\bar{C} + ABC + A\bar{B}\bar{C} + \bar{A}BC + ABC$ discarding similar terms (A+A=A) Thus the canonical form of given expression is $Y = ABC + A\bar{B}C + AB\bar{C} + A\bar{B}\bar{C} + \bar{A}BC$	
	iii	Draw excitation table for RS Flip-flop and JK flip-flop.	4M
	Ans:	See tables below	2M for each table

SR Flip-flop

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Excitation table for SR Flip Flop

JK flip-flop

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Excitation table for JK Flip Flop

Q. No.	Sub Q. N.	Answers	Marking Scheme
2		**Attempt any FOUR:**	**16-Total Marks**
	a	Compare TTL, ECL and CMOS logic family on following points: (i) Basic gates (ii) Component used (iii) Propagation delay (iv) Power dissipation	4M
	Ans:	See table below	1M EACH

Parameter	TTL	ECL	CMOS
Basic gates	NAND	OR-NOR	NOR-NAND
Component used	Transistors	Difference amplifiers	CMOS

Propagation delay	10ns	2ns	70-105ns
Power dissipation	10mW	40-55mW	1.01mW

b Design half subtractor using truth table and k-map. **4M**

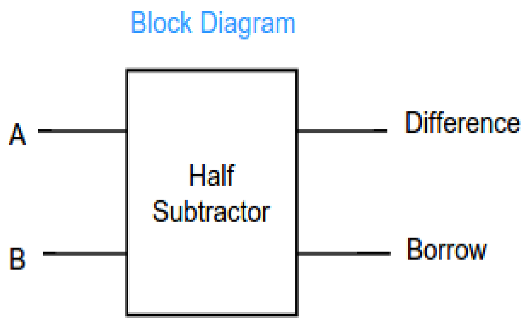
Ans:

T.T. 1M

k- MAP 1M

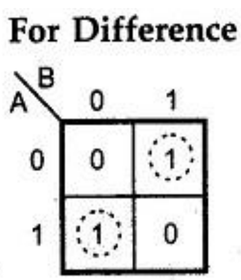
Expression – 1M

Logical circuit - 1M

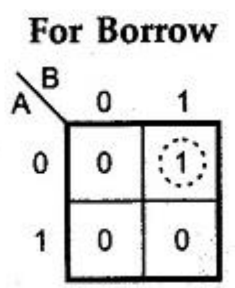


A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

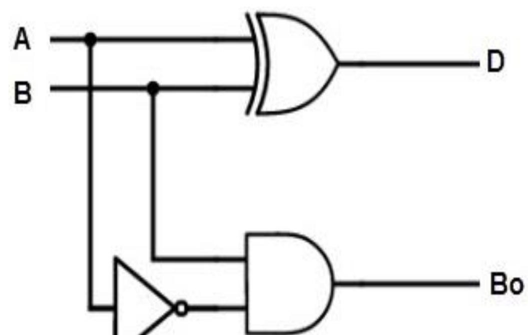
Truth Table



Difference = $A\bar{B} + \bar{A}B$
= $A \oplus B$



Borrow = $\bar{A}B$



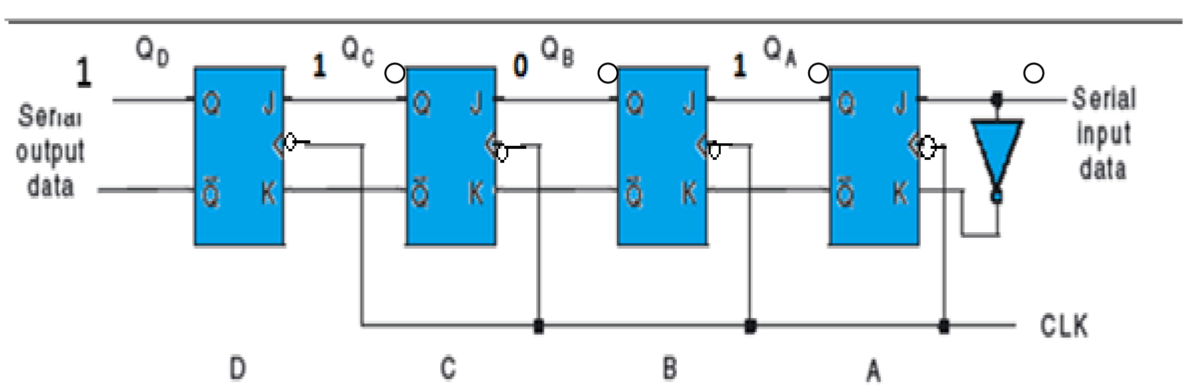
Logic Circuit of Half Subtractor

c Draw 4 bit left shift SISO registor, truth table and waveforms for data 1011. **4M**

Ans:

1. Logical Diagram

1M- Logical diagram



1M-

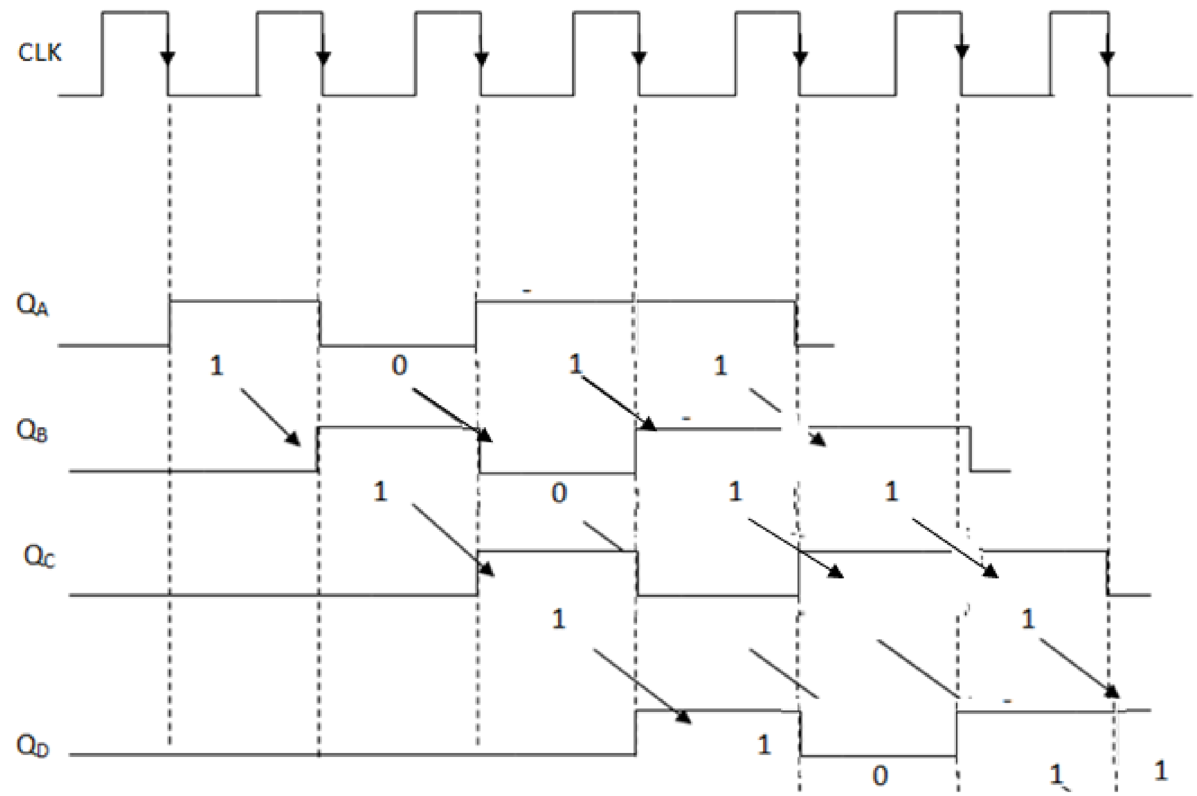
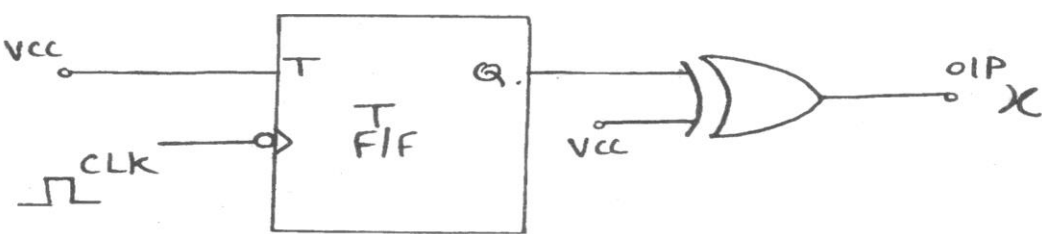
Truth Table

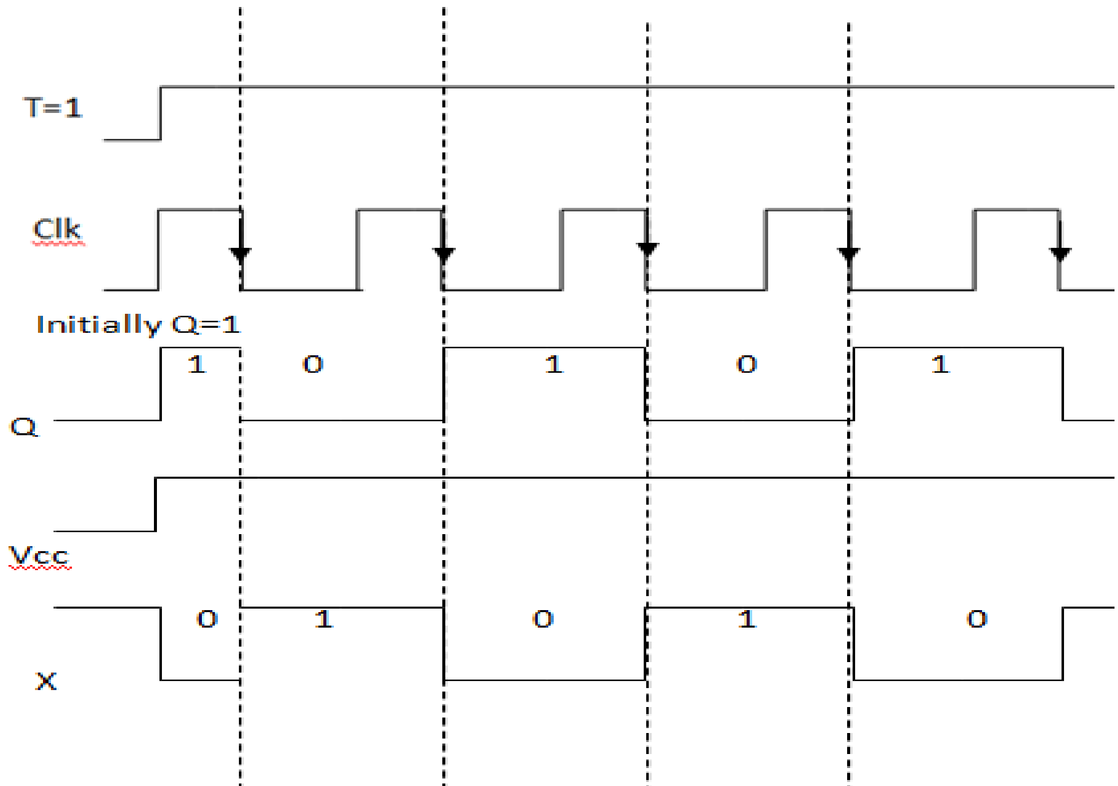
2. Truth Table

Timing Pulse	Serial output at Q_D	Q_D	Q_C	Q_B	Q_A	Serial Input
Initial value	0	0	0	0	0	
After 1st clock pulse	0	0	0	0	1	1
After 2nd clock pulse	0	0	0	1	1	1
After 3rd clock pulse	0	0	1	1	0	0
After 4th clock pulse	1	1	1	0	1	1
After 5th clock pulse	1	1	0	1	0	0
After 6th clock pulse	0	0	1	0	0	0
After 7th clock pulse	1	1	0	0	0	0

2M- waveform

3. Waveform:

			
	d	Study the following circuit and draw waveforms for Q and x. consider last value of Q = 1.  **last Value of Q = 1.** **Fig. No. 1**	4M
	Ans:	Waveforms:	1M for synchronised T, clk, Vcc

		 $x = Q.\overline{Vcc} + \bar{Q}.Vcc$ As Vcc=1, Output of Ex-OR gate will be When Q=0, Vcc=1 ➔X=1 Q=1, Vcc=1,➔ X=0	wave 1M For waveform of Q 2M for waveform of X
	e	Differentiate between weighted resistor method DAC and R-2R ladder DAC. (any four points)	4M
	Ans:	see table below	1M each point

Sr. No	**Weighted Resistor DAC**	**R-2R Ladder Type DAC**
1	Simple Construction	Slightly Complicated
2	Wide range of resistors are required	Resistors pf two values are required
3	One resistor per bit	Two resistors per bit
4	Not easy to expand for more number of bits	Easy to expand for more number of bits

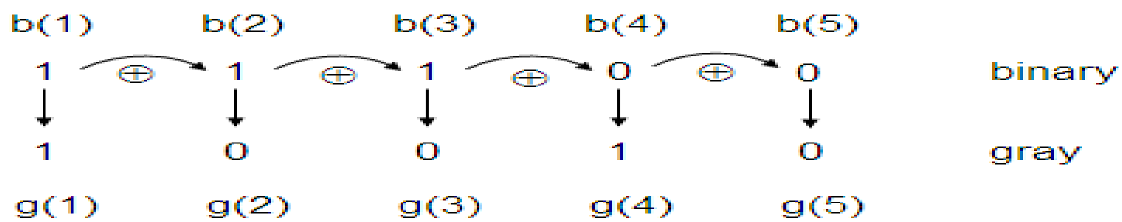
	f	Find out Gray code and excess-3 code of given numbers. (i) $(28)_{10}$ (ii) $(64)_{10}$	4M

Ans:

1. Converting into Gray code

$(28)_{10}$ => $(11100)_2$ ➔ $(10010)_{GRAY}$

1M For each conversion



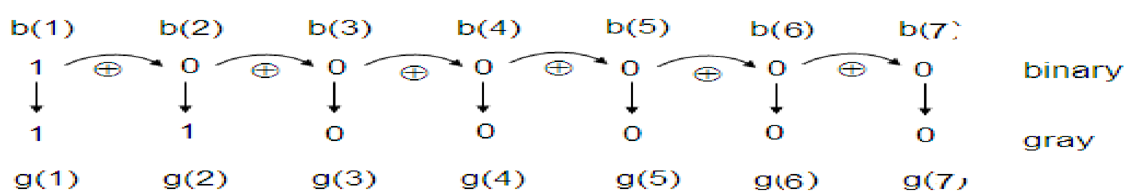
Converting into Excess-3

$(28)_{10}$ => $(0010\ 1000)_{BCD}$ ➔ $(0101\ 1011)_{XS-3}$

	0 0 1 0	1 0 0 0
+	0 0 1 1	0 0 1 1
	0 1 0 1	1 0 1 1

2. Converting into Gray code

$(64)_{10}$ => $(1000000)_2$ ➔ $(1100000)_{GRAY}$

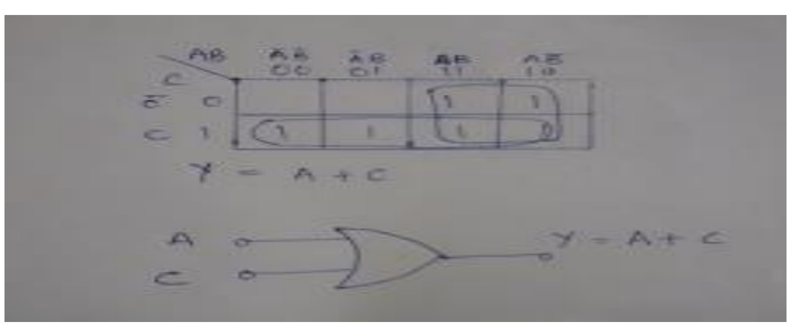


Converting into Excess-3

$(64)_{10}$ => $(0110\ \ 0100)_{BCD}$ ➔ $(1001\ \ 0111)_{XS-3}$

0 1 1 0 | 0 1 0 0

		+ 0 0 1 1 0 0 1 1 ———————— 1 0 0 1 0 1 1 1	

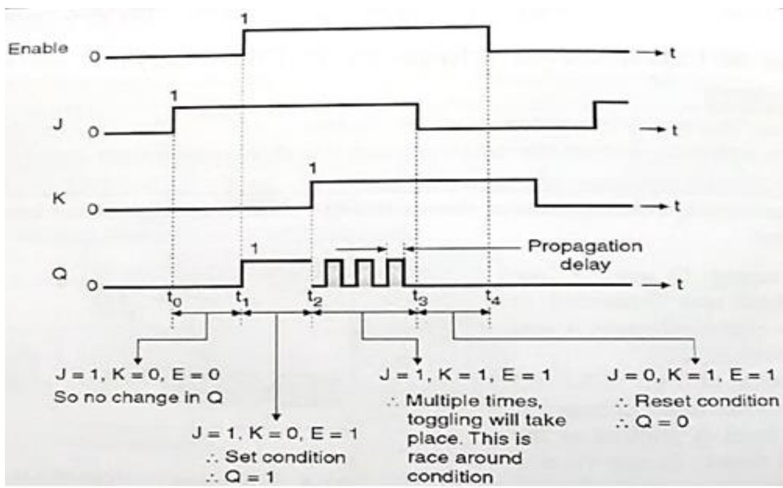
Q. No.	Sub Q. N.	Answers	Marking Scheme
3		**Attempt any FOUR:**	**16-Total Marks**
	a	Minimize the following expression using k-map and realize it using basic logic gates. Y=∑ m (1, 3, 4, 5, 6, 7)	4M
	Ans:	 	2 M – K-map & 2M - Realization

	Q	Question / Answer	Marks
	b	What is race around condition? How it can be avoided?	4M

Ans:

Race around condition: (2M)

- Race around condition occurs in J K Flip-flop only when J=K=1 and clock/enable is high (logic 1) as shown below-



Waveform showing Race around condition.

- In JK Flip-flop when J=K=1 and when clock goes high, output should toggle (change to opposite state), but due to multiple feedback output changes/toggles many times till the clock/enable is high.
- Thus toggling takes place more than once, called as racing or race around condition.

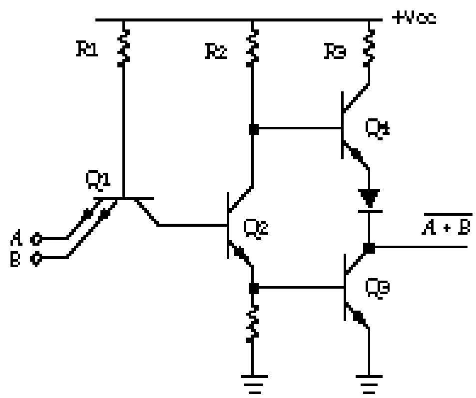
(2M)

Steps to avoid racing condition in JK Flip flop:

1. If the Clock On or High time is less than the propagation delay of the flip flop then racing can be avoided. This is done by using edge triggering rather than level triggering.
2. If the flip flop is made to toggle over one clock period then racing can be avoided. This introduced the concept of Master Slave JK flip flop.

	Q	Question / Answer	Marks
	c	Draw and explain the operation of 2 input totem pole TTL NAND gate with circuit diagram.	4M
	Ans:	• Circuit diagram for TTL gate with totem- pole output is as shown.	2M - Circuit Diagram & 2M-

Explanation



- Transistor Q1 is multi - emitter transistor, the output transistors Q3 and Q4 form a totem-Pole connection, with a totem- pole output stage, either the upper or lower transistor is on.
- When Q3 is on the o/p is high and when Q4 is on the O/P is low.
- If A or B is low, the base of Q1 is pulled down to approximately 0.7 V. This reduces the base voltage of Q2 to almost zero. Therefore Q2 cuts off. With Q2 open Q4 is off and the Q3 base is pulled high. The emitter of Q3 is only 0.7 V below the base and thus the Y output is pulled up to a high voltage.

Inputs		Y Output
A	B	
0	0	1
0	1	1
1	0	1

		• On the other hand when A and B both high, the emitter diodes of Q1 stop conducting and collector diode goes into forward conduction. This forces Q2 to turn on. In turn Q4 goes on and Q3 turn off, producing a low output as show in truth table. Without Diode D1, Q3 will conduct slightly. | 1 | 1 | 0 |	
	d	(i) Perform BCD addition. **(983)₁₀** + (274)₁₀ (ii) State the rules of BCD additions	4M
	Ans:	(i) BCD Addition:	2M

Decimal		BCD
983		1001 1000 0011
274	+	0010 0111 0100
		1011 1111 0111
		0110 0110 0000
Carry	1	0010 0101 0111
	1	2 5 7 (Final Answer)

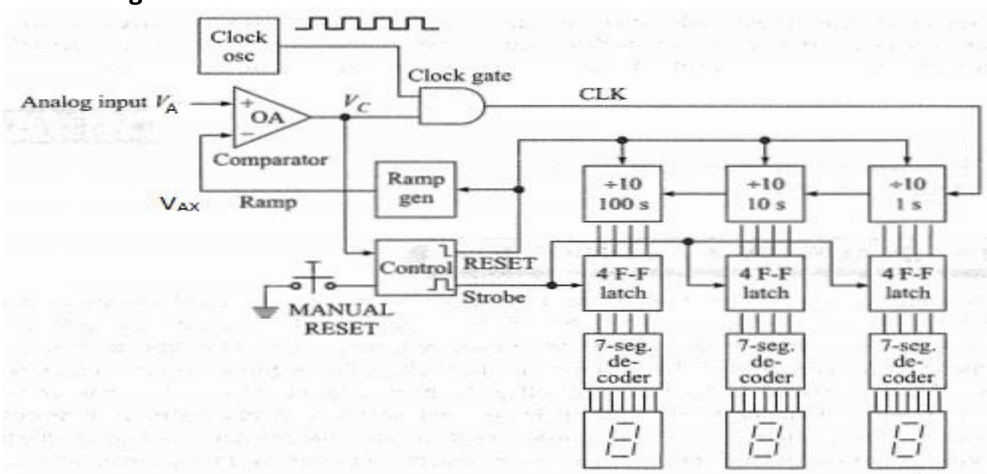
(ii) Rules of BCD Addition: 2M

1. If sum is less than or equal to 9 with carry equal to 0, then the sum is in proper BCD form and requires no correction.
2. If sum is greater than 9 but carry equal to 0, then it's an invalid BCD. Then we have to add decimal 6 or BCD 0110 to get the correct BCD.
3. If sum is less than or equal to 9 but carry equal to 1, then too it's an invalid BCD. Then we have to add decimal 6 or BCD 0110 to the sum to get the correct BCD.

	e	Draw and explain working of single slope ADC.	4M

Ans: **Circuit Diagram:**

2M - Circuit Diagram & 2M- Explanation



Operation:

- Manual RESET, will reset ramp generator as well as counter.VA has to be positive. RAMP begins at 0V.
- As VAX < VA, VC = 1 (HIGH). This will enable CLOCK gate allowing the CLK input, to be applied to the counter.
- As counter receives clock pulses, it will count up; and the RAMP continues upward.
- RAMP voltage rises till it reaches to VA input voltage.
- At this point, time t1, output V_O = 0 (LOW) and it will disable CLOCK gate and counter cease to advance.
- The negative transition of V_O, simultaneously generates a strobe signal in the CONTROL box that shifts the contents of the three decade counters into the three 4 FF latch circuit.
- Shortly after that, a reset pulse is generated (time t2), by the CONTROL box that resets the RAMP and clears the decade counter to all 0's (ZEROS) and another conversion cycle begins.

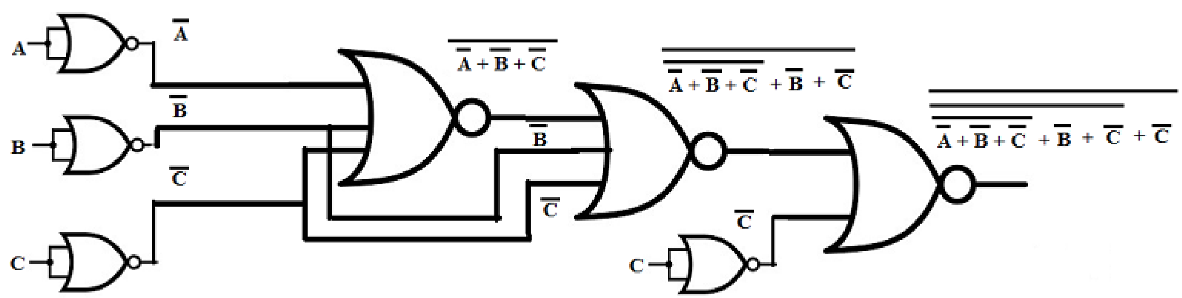
		• In the meantime the contents of the previous conversion are contained in the latches and are displayed on the seven segment display.	
	f	Differentiate between (i) Static RAM and dynamic RAM (ii) Volatile and Non-Volatile memory	4M
	Ans:	(i) Static RAM and dynamic RAM	2M each (Any 2 points)

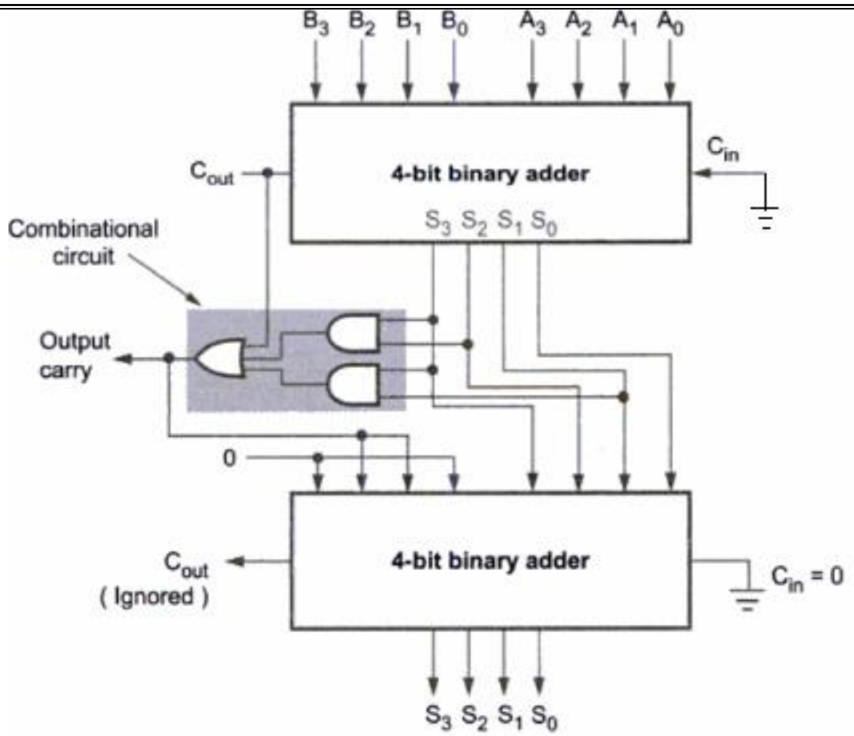
Parameter	Static RAM	Dynamic RAM
Circuit Configuration	Each SRAM cell is a flip flop	Each cell is one MOSFET & a capacitor
Bits stored	In the form of voltage	In the form of charges
No. of components per cell	More	Less
Storage capacity	Less	More

(ii) Volatile and Non-Volatile memory

Parameter	Volatile memory	Non-Volatile memory
Definition	Information is if power is turned off	Information is not lost if power is turned off
Classification	All RAMs	ROMs, EPROM, magnetic memories
Effect of power	Stored information is retained only as long as power is on	No effect of power on stored information
Applications	For temporary storage	For permanent storage of information.

Q. No.	Sub Q. N.	Answers	Marking Scheme
4		**Attempt any FOUR:**	**16-Total Marks**
	a	(i) Add binary numbers. $(10110.110)_2 + (1001.1)_2$ (ii) Multiply $(1110)_2 \times (101)_2$	4M
	Ans:	(i) $(10110.110)_2 + (1001.1)_2 = (100000.01)_2$ $\begin{array}{r} 10110.11 \\ +\ \ 1001.1 \\ \hline 100000.01 \\ \hline \end{array}$ (ii) $(1110)_2 \times (101)_2 = ()_2$ $\begin{array}{r} 1110 \\ \times\ \ 101 \\ \hline 1110 \\ +\ 0000- \\ +\ 1110-- \\ \hline 1000110 \\ \hline \end{array}$	2M 2M
	b	Realize the following expression using only NOR gate. $Y = (ABC + \bar{B} + \bar{C}).C$	4M

	Ans:	$Y = \overline{\overline{(\overline{\overline{\bar{A}BC}} + \bar{B} + \bar{C}) \cdot C}}$ $= \overline{\overline{(\overline{\bar{A} + \bar{B} + \bar{C}} + \bar{B} + \bar{C}) \cdot C}}$ $= \overline{\overline{(\overline{\bar{A} + \bar{B} + \bar{C}} + \bar{B} + \bar{C})} + \bar{C}}$	2M
			2M
	c	Draw and explain working of single digit BCD adder using IC 7483.	4M

	Ans:	 • BCD Adder adds two BCD numbers and gives result in BCD form the output sum cannot exceed 09. • As shown in the Fig, the two BCD numbers, together with input carry, are first added in the top 4-bit binary adder to produce a binary sum. • When the output carry is equal to zero (i.e. when sum <= 9 and Cout = 0) nothing (zero) is added to the binary sum. • When it is equal to one (i.e. when sum > 9 or Cout = 1), binary 0110 is added to the binary sum through the bottom 4-bit binary adder. • The output carry generated from the bottom binary adder can be ignored, since it supplies information already available at the output carry terminal.	2M - Circuit Diagram & 2M- Explanation
	d	Design a 3 bit synchronous up counter and draw it.	4M
	Ans:	Step1: Construct JK state table with corresponding excitation table:	1.5 M - Step 1 1.5 M - Step 2

Output State Transitions		Flip-flop inputs		
Present State Q2 Q1 Q0	Next state Q2 Q1 Q0	J2 K2	J1 K1	J0 K0
0 0 0	0 0 1	0 X	0 X	1 X
0 0 1	0 1 0	0 X	1 X	X 1
0 1 0	0 1 1	0 X	X 0	1 X
0 1 1	1 0 0	1 X	X 1	X 1
1 0 0	1 0 1	X 0	0 X	1 X
1 0 1	1 1 0	X 0	1 X	X 1
1 1 0	1 1 1	X 0	X 0	1 X
1 1 1	0 0 0	X 1	X 1	X 1

State Table and Corresponding Excitation Table (d=don't care)

1M – Step 3

Step 2:

Build Karnaugh Map or Kmap for each JK inputs:

Q2Q1 \ Q0	0	1
00	0	0
01	0	1
11	X	X
10	X	X

J2 map

Q2Q1 \ Q0	0	1
00	0	1
01	X	X
11	X	X
10	0	1

J1 map

Q2Q1 \ Q0	0	1
00	1	X
01	1	X
11	1	X
10	1	X

J0 map

Q2Q1 \ Q0	0	1
00	X	X
01	X	X
11	0	1
10	0	0

K2 map

Q2Q1 \ Q0	0	1
00	X	X
01	0	1
11	0	1
10	X	X

K1 map

Q2Q1 \ Q0	0	1
00	X	1
01	X	1
11	X	1
10	X	1

K0 map

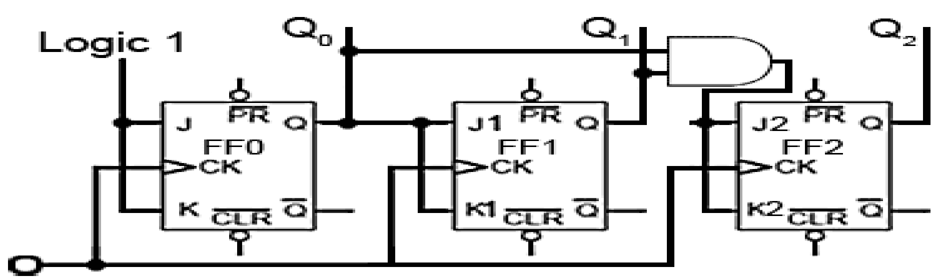
J0 = K0 = 1

J1 = K1 = Q0

J2 = K2 = Q1 * Q2

Step 3:

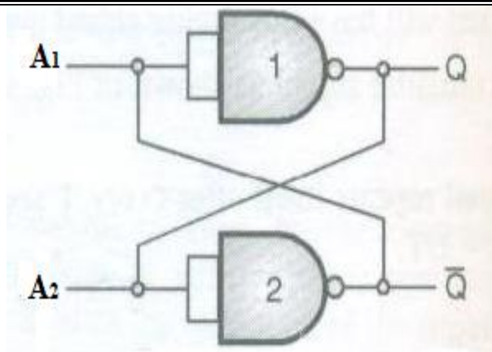
Draw the complete design as below:



Note : It can also be designed using T Flip Flop.

e	Draw single digit memory cell using NAND gates and explain working with truth table.	4M

Ans:



A1	Q	A2 = Q	$\bar{Q}$ = A2
0	1	1	0
1	0	0	1

Circuit Diagram   Truth Table

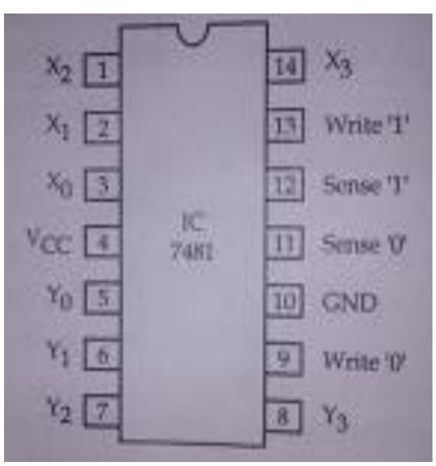
Operation:

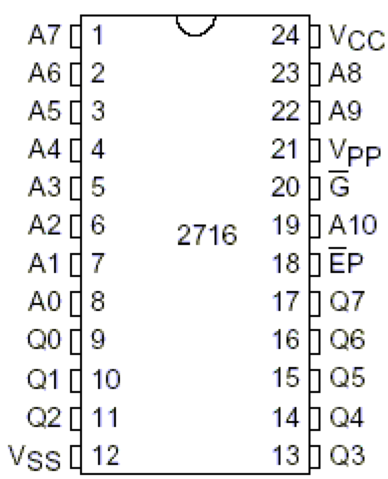
- Assume that the output of gate 1 i.e. Q = 1. Hence A_2 = 1.
- As A_2 = 1, output of gate 2 i.e. $\bar{Q}$ = 0 which makes A1 = 0.
- Hence Q continues to be equal to 1.
- Similarly we can demonstrate that if we start with Q = 0,then we obtain Q = 0 and .
  $\bar{Q}$ = 1.

f Identify function of IC 7481 and IC 2716 and draw its pin diagram. **4M**

Ans: Function of IC 7481 and IC 2716:

IC 7481 - Bipolar RAM In 4 x 4 Matrix   IC 2716 – 16 KB EPROM





Each Function 1M

Pin Diagram 1M

Q. No.	Sub Q. N.	Answers	Marking Scheme
5		**Attempt any FOUR:**	**16-Total Marks**
	a	Compare single slope ADC and dual slope ADC (any four points).	4M

Ans:

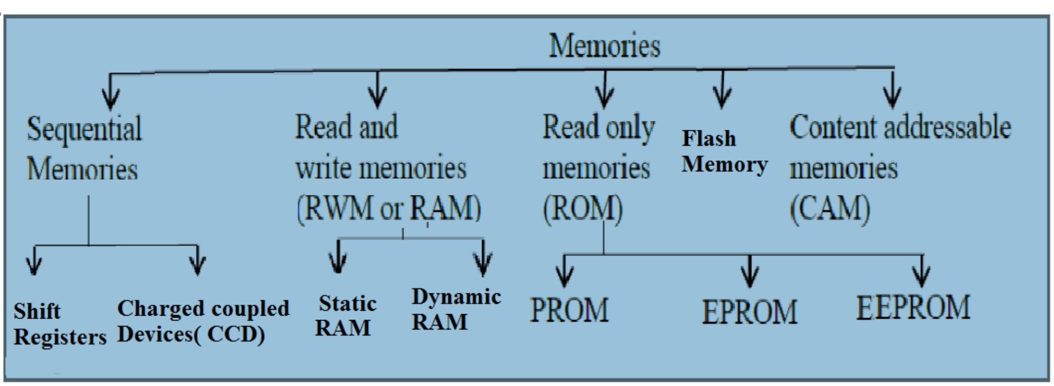
(any four points- 1 Mk for each Point).

Sr. No.	Single slope ADC	dual slope ADC
1	Single-slope ADCs are appropriate for very high accuracy of high-resolution measurements where the input signal bandwidth is relatively low	Dual slope ADCs provides increased range, the increased accuracy and resolution.
2	Less cost	Costly
3	The name implies that single-slope ADC use only one ramp cycle to measure each input signal	Dual-Slope ADC operate on the principle of integrating the unknown input and then comparing the integration times with a reference cycle.
4	Conversion result is dependent on the tolerances of the R & C values	Conversion result is insensitive to errors in the component values
5	Poor noise immunity	Good noise immunity
6	Speed more	Speed less
7	Simple circuitry	Complicated circuitry

b How are memories classified ? Explain any two types of memories. 4M

Ans:

Classification 2M Explanation (any 2-1 Mk each)



1) RAM :

- Random access memory is also called as read-write memory.
- In this type of memories, the memory locations are organized in such a way that the
  access time required for any location is same.
- Data stored at any location can be changed during the operation of the system.

2) Static RAM

- This type of memory can be implemented by bipolar as well as MOS technology.
- It is possible to store data as long as power is applied to the chip.
- The basic cell in SRAM is a flip-flop

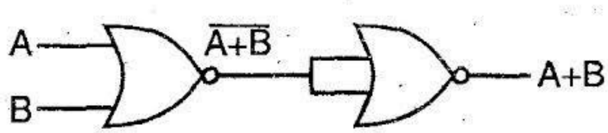
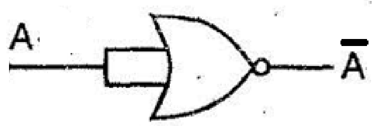
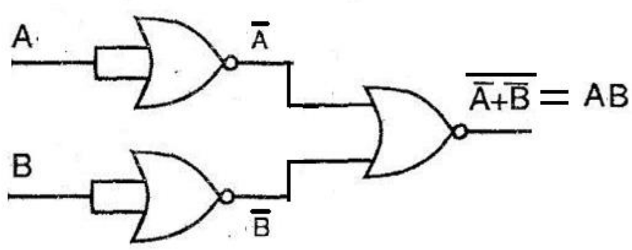
3) Dynamic RAM

- In dynamic RAM, the data is stored in the form of charge on the capacitor.
- Its formed using MOSFET and capacitor.
- It needs to be refreshed after every few milliseconds.

4) Flash Memory:-

- Flash memory is non-volatile RAM memory that can be electrically erased and reprogrammed.
- Flash memory can be written to in block size rather than byte, it is easier to update it.
- Due to this, the flash memories are faster than EEPROMS which erase and

		write new data of byte level. • This type of memory has been named as 'flash memory' because a large block of memory could be erased at one time, i.e. in a single action or 'flash'. • Important features are high speed, low operating voltages, low power consumption. • Typical application areas are digital camera`s embedded controllers, cellular phones etc. **5) Programmable Read Only Memories (PROM):-** • PROM is electrically programmable i.e. the data pattern is defined after final packaging rather than when the device is fabricated. • The programming is done with an equipment referred to as PROM programmer. • The PROM are one time programmable. Once programmed, the information stored is permanent. **6) Erasable Programmable Read Only Memories (EPROM):-** • In these memories, data can be written in any number of times i.e. they are reprogrammable. • Reprogrammable ROMs are possible only in MOS technology. For erasing the contents of the memory, one of the following two methods are employed: a) Exposing the chip to ultraviolet radiation for about 30minutes (UVEPROM) b) Erasing electrically by applying voltage of proper polarity & amplitude. Electricity erasable Prom is also referred to as E^2PROM or EEPROM or EAROM (Electrically alterable ROM)	
	c	Why NAND and NOR gates are called as universal gates. Derive basic gates using NOR gates only.	4M

	Ans:	NAND and NOR gates are called as universal gates because 1. It is possible to implement any Boolean expression with the help of only NAND or only NOR gate. 2. Hence a user can build any combinational circuit of any complexity with the help of only NAND or NOR gates . OR Gate  NOT Gate (1 mk)  AND Gate (1 mk)  	Reason :1 M 1M 1M 1M
	d	Write a truth table for given circuit if A B changes from 00 to 11.	4M

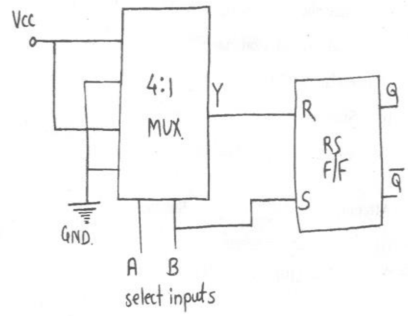


Fig. No. 2

Ans:

A	B=S	Y=R	Q	$\overline{Q}$
0	0	I_0 =1	0	1
0	1	I_1=0	1	0
1	0	I_2=1	0	1
1	1	I_3=0	1	0

Correct Truth table (4 Mks)

e Draw binary to gray code converter and write its truth table. 4M

Ans: Truth Table for 4 bit Binary to Gray code converter

Binary Input				Gray Output			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

2M

K-MAP FOR G3:

B3B2 \ B1B0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

G3=B3

K-MAP FOR G2:

B3B2 \ B1B0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

Equation for G2= $\overline{B3}$B2 + B3 $\overline{B2}$= B3 XOR B2

K-MAP FOR G1:

B3B2 \ B1B0	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1

Equation for G1= $\overline{B1}$B2 + B1 $\overline{B2}$= B1 XOR B2

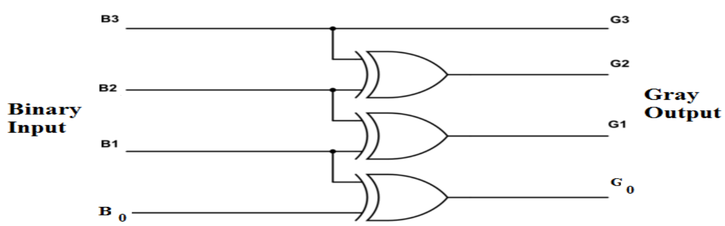
K-MAP FOR G0:

B3B2 \ B1B0	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

Equation for G0= $\overline{B1}$ B0 + B1 $\overline{B0}$= B1 XOR B0

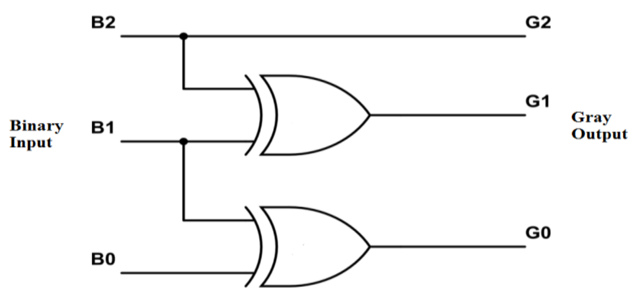
2M(even if K Map is not drawn)

Diagram for 4 bit Binary to Gray code converter



OR

Diagram for 3 bit Binary to Gray code converter (2 Mks)

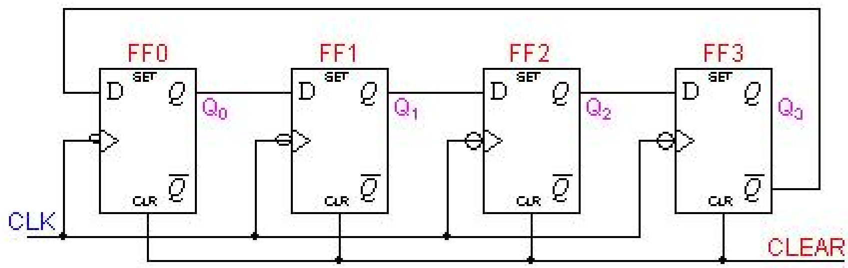


Truth Table for 3 bit Binary to Gray code converter (2 Mks)

Binary Input			Gray Output		
B_2	B_1	B_0	G_2	G_1	G_0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1

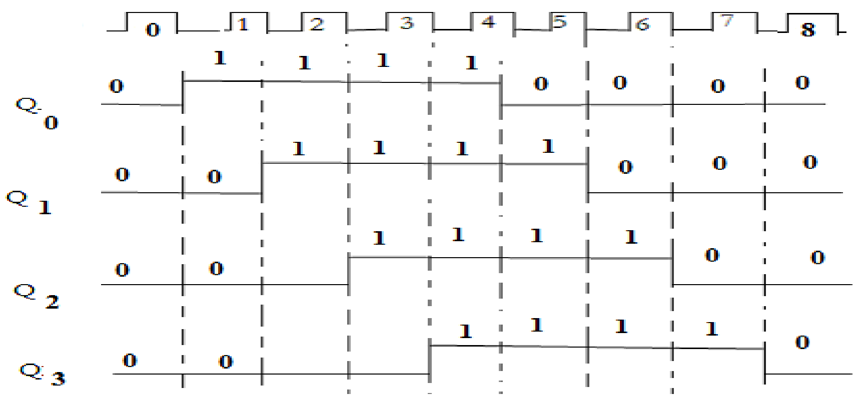
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

f	Draw 4 - bit twisted ring counter and explain working with truth table and	4M

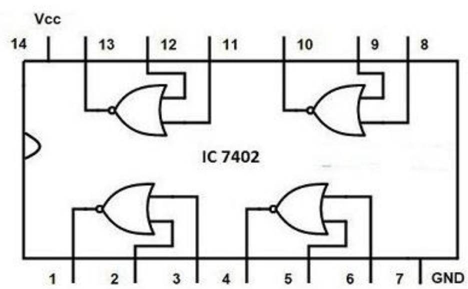
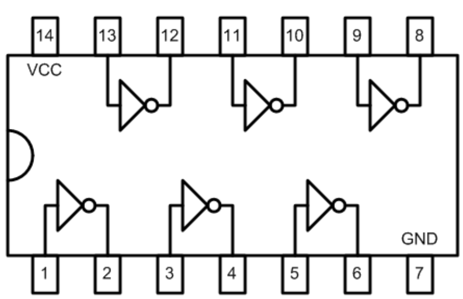
		waveforms.	
	Ans:	 **Twisted Ring Counter** also known as Johnson Counter is another basic application of shift registers with a feedback. Here the feedback is given from the inverted output of the last flip flop to the input of the first flip-flop. • Figure above shows a 4-bit Johnson counter. • It consists of four flip-flops FF0, FF1, FF2 and FF3. Here the inverted output of the last flip-flop FF3 is given as feedback to the input of the first flip-flop FF0. • Here, at first four logic zeros will be passed to the flip-flops. • When clock pulses are given "1000", "1100", "1110", "1111", "0111", "0011", "0001", "0000" outputs will be obtained and the sequence will repeat for the next clock pulses. • There are 8 different states of output . In general , the number of states of Johnson Counter is twice the number of flip flops used.	**Diagram:1M** **Explanation: 1M**

Clock	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

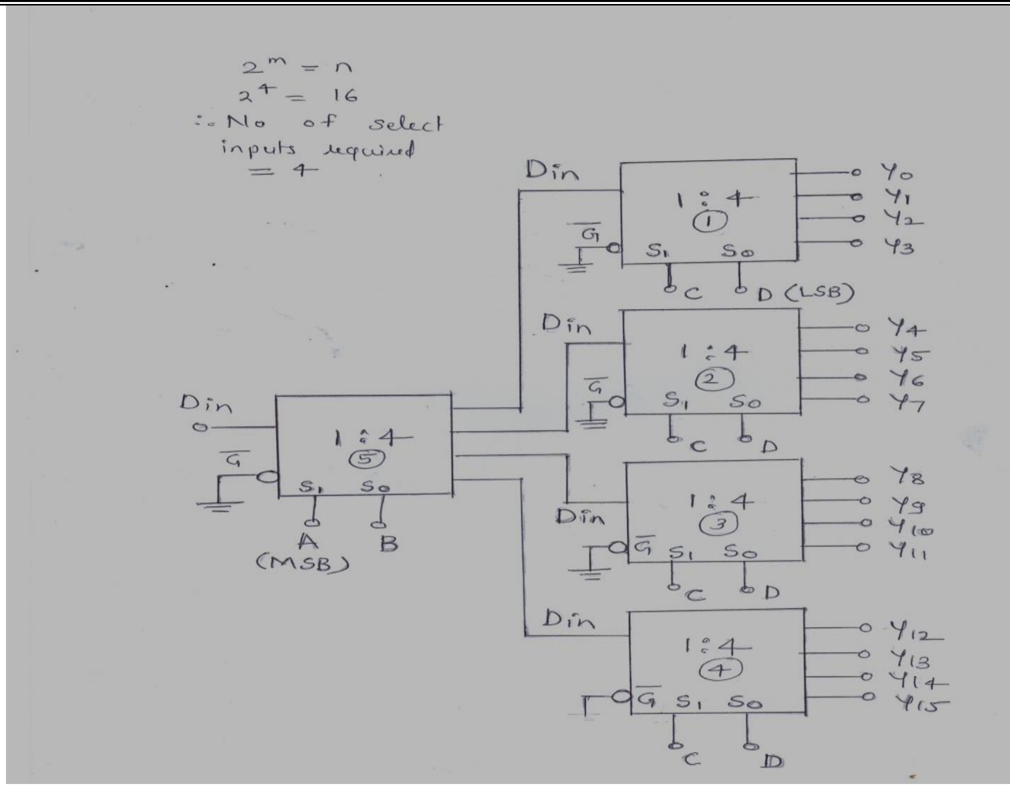
Truth Table: 1M



Waveform: 1M

Q. No.	Sub Q. N.	Answers	Marking Scheme
6		**Attempt any FOUR:**	**16-Total Marks**
	A	Draw the pinout configuration for (i) IC 7402 (ii) IC 7404	4M
	Ans:	Pin Diagram of IC 7402  Pin Diagram of IC 7404  	2M 2M
	B	Implement 1:16 Demux using 1:4 Demux write a truth table.	4M

Ans:



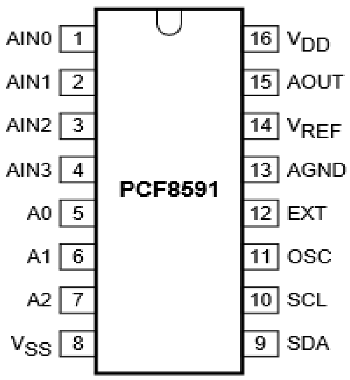
Circuit diagram -2M

Select inputs				outputs															
A	B	C	D	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}
0	0	0	0	Din	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	Din	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	Din	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	Din	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	Din	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	Din	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	Din	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	Din	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	Din	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	Din	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	Din	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	Din	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Din	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Din	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Din	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Din

Truth table – 2M

c Draw pin diagram of IC PCF 8591 and list four features. 4M

Ans: Pin diagram



Pin diagram (DIP16).

SYMBOL	PIN	DESCRIPTION
AINO	1	analog inputs (A/D converter)
AIN1	2	
AIN2	3	
AIN3	4	
A0	5	hardware address
A1	6	
A2	7	
V_{SS}	8	negative supply voltage
SDA	9	I^2C-bus data input/output
SCL	10	I^2C-bus clock input
OSC	11	oscillator input/output
EXT	12	external/internal switch for oscillator input
AGND	13	analog ground
V_{REF}	14	voltage reference input
AOUT	15	analog output (D/A converter)
V_{DD}	16	positive supply voltage

Pin diagram: 2M (consider even if description not given)

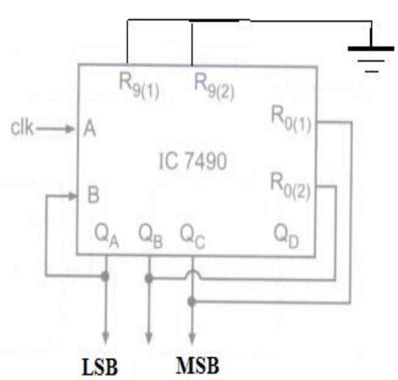
Features

1. Single power supply
2. Operating supply voltage 2.5 V to 6 V
3. Low standby current
4. Serial input/output via I^2C-bus
5. Address by 3 hardware address pins
6. Sampling rate given by I^2C-bus speed
7. 4 analog inputs programmable as single-ended or
8. differential inputs
9. Auto-incremented channel selection
10. Analog voltage range from VSS to VDD
11. On-chip track and hold circuit
12. 8-bit successive approximation A/D conversion
13. Multiplying DAC with one analog output

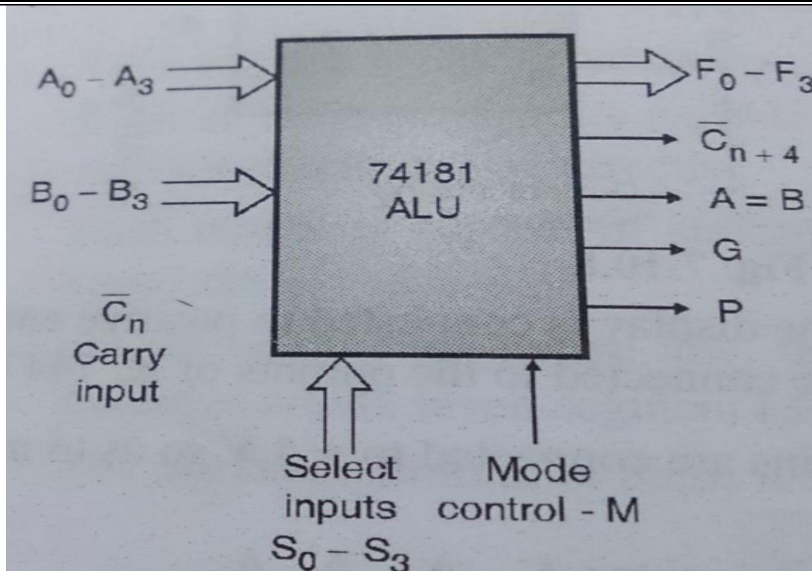
Any 4 features ½ M each

	d	Design and draw MOD-6 counter using IC 7490.	4M
	Ans:	Clock is given to clock input A. Output Q_A is connected to clock input B. To reset the counter after counting the first six states from 0 to 5, the counter outputs Qc and QB should be connected to the reset inputs. Truth table	Design 2 M diagram 2M

Clock	Output		
	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	0	0	0



	e	Draw block diagram of ALU 74181 and explain.	4M

	Ans:		**Diagram 2M**
		Explanation- IC 74181 is a high speed, 24 pin IC DIL package. Widely used combinational logic, capable of performing the arithmetic as well as logical operations. It is the heart of microprocessor. A and B are the two 4 bit input variables, F is the 4 bit output variable, S are the 4 bit select lines that decides various (either arithmetic or logical) operations M= mode control that decides whether ALU will perform arithmetic or logical operations If M= 1, 16 Logical operations (AND,OR ,NOR etc operations ,depending upon the 4 bit combination of select lines) If M=0, 16 Arithmetic operations (addition, subtraction, division etc operations ,depending upon the 4 bit combination of select lines) A=B ,Comparator equality output G and P are the carry generate and carry propagate outputs used for cascading of ALUs	**Explanation 2 mks**
	f	Calculate output voltage for 4 bit binary weighted resistor DAC for binary inputs and V_{ref} = 5V. (i) 1 0 1 0 (i i) 1 1 0 0	4M

Ans: Considering MSB resistor is 2R, $R_F = R$

Output voltage for 4 bit (D C B A) binary weighted resistor DAC is given by

$$Vo = \frac{RF}{R} Vref \left(\frac{b_{n-1}}{2^1} + \frac{b_{n-1}}{2^2} + \frac{b_{n-1}}{2^3} + \frac{b_{n-1}}{2^4}\right)$$

(i) 1 0 1 0 = D C B A

$$Vo = Vref \left(\frac{1}{2^1} + \frac{0}{2^2} + \frac{1}{2^3} + \frac{0}{2^4}\right)$$

=3.125V

(i i) 1 1 0 0 = D C B A

$$Vo = Vref \left(\frac{1}{2^1} + \frac{1}{2^2} + \frac{0}{2^3} + \frac{0}{2^4}\right)$$

=3.75V

(OR)

Considering V(0) = 0V and V(1) = V_{ref} = 5V

MSB resistor is 2R, $R_f = R$

output voltage for 4 bit (D C B A) binary weighted resistor DAC is given by

$$V_0 = \left[\frac{V_D}{2} + \frac{V_C}{4} + \frac{V_B}{8} + \frac{V_A}{16}\right]$$

Where D= MSB bit & A= LSB bit

(i i i) 1 0 1 0 = D C B A

$$V_0 = \left[\frac{5}{2} + \frac{0}{4} + \frac{5}{8} + \frac{0}{16}\right]$$

$V_0 = 3.125$ V

		Note :- Mark should be given even if MSB resistor is taken as R and calculated using formula, $V_o = V_D + \frac{V_C}{2} + \frac{V_B}{4} + \frac{V_A}{8}$	