

### SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

Subject Code:

17534

### Important Instructions to examiners:

- 1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
- 2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
- 3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
- 4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
- 5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
- 6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
- 7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q. N.			Answers		Marking Scheme
1	а	Atter	npt any THREE:			12- Total Marks
	i	Comp	oare between mi	croprocessor and microcontro	ller (any four points).	4M
	Ans:					1Mark each
		Sr. No	Parameter	Microprocessor	Microcontroller	
		1	No. of instructions used	Many instructions to read/write data to/ from external memory.	Few instruction to read/ write data to/ from external memory	
		2	Memory	Do not have inbuilt RAM or ROM.	Inbuilt RAM /or ROM	
		3	Registers	Microprocessor contains general purpose registers, Stack pointer register, Program counter register	Microcontroller contains general purpose registers, Stack pointer register, Program counter register additional to that it contains Special Function Registers (SFRs) for Timer, Interrupt and serial communication	



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				etc.	
	4	Timer	Do not have inbuilt Timer.	Inbuilt Timer	
	5	I/O ports	I/O ports are not available requires extra device like 8155 or 8255.	I/O ports are available	
	6	Serial port	Do not have inbuilt serial port, requires extra devices like 8250 or 8251.	Inbuilt serial port	
	7	Multifunction pins	Less Multifunction pins on IC.	Many multifunction pins on the IC	
	8	Boolean Operation	Boolean operation is not possible directly.	Boolean Operation i.e. operation on individual bit is possible directly	
	9	Applications	General purpose, Computers and Personal Uses.	Single purpose(dedicated application), Automobile companies, embedded systems, remote control devices.	
ii	Draw	v neat labelled block	diagram of Von-neumann	and Harvard architecture.	4M
Ans:		CPU <	ata ddress	lata	2М
	Harv	ard Architecture			



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	SMOD	-	-	-	GF1	GF0	PD	IDI			
SMOI	Dauble be		IC Times	1 in more da	b		SUOD -	1 db - ba		in daarki a	
5/101				modes 1,	to generate b 2, or 3.	iud rate and	SMOD -	- i, ine ba	ud rate	is double	
-	Not imple	emented, re	served for	future use	•						11
-	•			future use							
—	•			future use	•						
GF1	General p	-									
GF0 PD	General p	-		hit activat	es Power Do	wa operatio	n in tha Q	005100			
PD	Power Do	own on. S	tung uns	on activat	to rower Do	wii operatio	n in the e	ocondri.			
IDL	Idle Mode	e bit. Settir	g this bit a	ctivates Id	le Mode oper	ation in the	80C51BH.				
IDLE MC	DE										
In the Id	le mode,	the inte	ernal clo	ck signa	l is gated	off to the	CPU, b	ut not to	the l	nterrup	pt,
Timer, a	nd Serial	Port fui	nctions.								
The CPU	status is	preserv	ed in its	s entiret	y, the Sta	ck Pointe	r, Progra	am Cour	nter, F	rogram	n
Status W	/ord, Acc	umulate	or, and a	all other	registers	maintain	their da	ita durir	g Idle	. The	
port pin:	s hold the	e logical	state th	ney had	at the tim	e idle mo	de was	activate	d. ALE	Eand	
PSEN ho	ld at logi	c high le	vels.								
There ar	e two wa	ays to te	rminate	the idle	e mode.						
i) Activa	tion of ar	ny enabl	ed inter	rupt wil	l cause PC	ON.O to	be clear	ed and i	dle m	ode is	
terminat	ted.										
ii) Hard v	ware rese	et: that	s signal	at RST p	oin clears	DEAL bit	IN PCOI	N registe	er dire	ctly. At	t   1N
this time	e, CPU res	sumes t	ne prog	ram exe	cution fro	m where	it left o	ff.			
POWER	DOWNN	/IODE									
An instru	uction the	at sets F	CON.1	causes t	hat to be <sup>.</sup>	he last ir:	structio	on execu	ted b	efore	
aning int	the be	WOR LION	wn mad	o ln +ho	Dowor D	own mod	o tho o	n chin a	coillat	oric	



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	stopped. With the clock frozen, all functions are stopped, but the on-chip RAM and	
	Special Function Register are maintained held. The port pins output the values held by	
	their respective SFRS. ALE and PSEN are held low.	
	Termination from power down mode: an exit from this mode is hardware reset.	
	Reset defines all SFRs but doesn't change on chip RAM	1M
iv	Write the operation of the following instructions of 8051.	4M
	1) CJNE A, direct, rel	
	2) DAA	
	3) DJNZ Rn, rel.	
	4) SWAP A	
Ans:		
	1) CJNE A, direct, rel	1M for
	Compare the contents of the accumulator with the 8 bit data in memory address	each instructio
	mentioned in the instruction and if they are not equal then jump to the relative address	with
	mentioned in the instruction.	example
	Example: CJNE A, 04H, UP	
	Compare the contents of the accumulator with the contents of 04H memory and if they	
	are not equal then jump to the line of instruction where UP label is mentioned.	
	2) DA A (Decimal Adjust After Addition).	
	When two BCD numbers are added, the answer is a non-BCD number. To get the result in	
	BCD, we use DA A instruction after the addition.	
	DA A works as follows.	
	• If lower nibble is greater than 9 or auxiliary carry is 1, 6 is added to lower nibble.	
	<ul> <li>If upper nibble is greater than 9 or carry is 1, 6 is added to upper nibble.</li> </ul>	
	Eg 1: MOV A,#23H	
	MOV R1,#55H	



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	ADD A, R1 // [A]=78 H	
	DA A // [A]=78 no changes in the accumulator after da a	
	<b>Eg 2</b> : MOV A,#53H	
	MOV R1,#58H	
	ADD A,R1 // [A]=ABh	
	DA A // [A]=11, C=1 . ANSWER IS 111. Accumulator data is changed after DA A	
	3) DJNZ Rn, rel.(Decrement and jump if not zero)	
	In this instruction a byte present in register Rn is decremented, and if the result is not	
	zero it will jump to the relative address mentioned in the instruction.	
	Example: DJNZ R3, HERE	
	Decrements the contents of the register R3, and if it is not equal to zero then jump to the	
	line of instruction where HERE label is mentioned.	
	4) SWAP A	
	Description: This instruction exchanges bits 0-3 of the Accumulator with bits 4-7 of the	
	Accumulator. This instruction is identical to executing "RR A" or "RL A" four times.	
	No of bytes: 1 byte	
	Addressing mode: register specific	
	Example: MOV A, #59H ; A= 59H	
	SWAP A ; A= 95H	
v	With control word register, explain Bit Set reset (BSR) mode of 8255.	4M
Ans:		



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			1	1	0	PC <sub>6</sub>			
			1	1	1	PC <sub>7</sub>			
	• Bit I	$D_0$ is used to	o set/res	et the sel	lected pin of	Port C.			
	As an example, if it is needed that $PC_5$ be set, then in the control word,								
	<ol> <li>Since it is BSR mode, D<sub>7</sub> = '0'.</li> <li>Since D<sub>4</sub>, D<sub>5</sub>, D<sub>6</sub> are not used, assume them to be '0'.</li> <li>PC<sub>5</sub> has to be selected, hence, D<sub>3</sub> = '1', D<sub>2</sub> = '0', D<sub>1</sub> = '1'.</li> <li>PC<sub>5</sub> has to be set, hence, D0 = '1'.</li> </ol>								
	Thus, as per the above values, OB (Hex) will be loaded into the Control Word Register (CWR).								
	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D4	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	
	0	0	0	0	1	0	1	1	
b	Attempt ar	ny ONE:							6- Total Marks
i		AM location				verage of ten Is store result			6M
Ans:									
	ORG 0000H								
	MOV R1, #0A ;R1 stores the count of total 8 bit numbers								6M for correct
	MOV B, #0A ;B is used as divisor for average								
	МС	DV B, #0A DV R0, #30H DV A, #00H	I		R0 acts as po Clear A	inter to the da	ata		



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		INC RO	; Increment the pointer	
		DJNZ R1,BACK	; repeat addition until R1=0	
		DIV AB	; divide sum to get average	
			; quotient is in A and remainder in B	
		MOV 60H,A	;Ignore remainder and store average result in 60h	
	HERE:	SJMP HERE	; wait	
		END		
ii	Sketch Interfa	8051 microcontroller ice LEDs to port 0 uppe	ge. Please check the logic and understanding of students. interfacing diagram to interface 4 LEDs and 4 switches. er nibble and switch to port 1. Write an ALP for 8051 to operate LEDs as per switch status.	6M
Ans:				
		ca ny		
				3М
	Progra			3М
	Progra	m: ORG 0000H MOV P1, #0F0F		3M



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17534 Subject Code: ; Key pressed branch from Port 0 CJNE A, #0F0H, CHECK1 SJMP START ; Branch to start CHECK1: ACALL DELAY ; Call delay 3M MOV A, P1 ; Read data from port 0 CPL A ; Complement A MOV PO, A ; Send data to LED AJMP START ; Jump to start DELAY: MOV R6,#20H ; Delay program NEXT1: MOV R7, #0FFH NEXT2: DJNZ R7, NEXT2 DJNZ R6, NEXT1 RET END

NOTE: Program may change. Please check the logic and understanding of students.



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Q. No.	Sub	Answers	Marking Scheme
NO.	Q. N.		Scheme
2		Attempt any FOUR:	16- Total Marks
	а	Draw pin diagram of 8051 microcontroller.	4M
	Ans:	4 M for correct diagram	
		P1.0       1       40       Vcc         P1.1       2       39       P0.0 (AD0)         P1.2       3       38       P0.1 (AD1)         P1.3       4       8051       37       P0.2 (AD2)         P1.4       5       36       P0.3 (AD3)         P1.5       6       35       P0.4 (AD4)         P1.6       7       34       P0.5 (AD5)         P1.7       8       33       P0.6 (AD6)         RST       9       32       P0.7 (AD7)         (RXD) P3.0       10       31       EAVPP         (TXD) P3.1       11       30       ALE/PROG         (INTT) P3.3       13       28       P2.7 (A15)         (TO P3.4       14       27       P2.6 (A14)         (T1) P3.5       15       26       P2.5 (A13)         (WF) P3.6       16       25       P2.4 (A12)         (RD) P3.7       17       24       P2.3 (A11)         XTAL2       18       23       P2.2 (A10)         XTAL1       19       22       P2.1 (A9)         GND       20       21       P2.0 (A8)	4M
	b	Which pins of 8051 microcontroller are used for external memory interfacing with 8051? State their functions.	4M
	Ans:		
	_	The following pins of 8051 are used for external memory interfacing:	1M each
		i) PSEN/:PSEN stands for —program store enable.∥ In an 8031-based system in which an	
		external ROM holds the program code, this pin is connected to the OE pin of the ROM.	
		In other words, to access external ROM containing program code, the 8031/51 uses the	
		PSEN signal. When the EA pin is connected to GND, the 8031/51 fetches opcode from	



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	machine cycles before it is allowed to go low.	
	3. In order for the RESET input to be effective, it must have a minimum duration of two machine cycles. In other words, the high pulse must be high for a minimum of two	
	values in the registers to be lost. It will set program counter to all 0s.	
	2. This is often referred to as a power-on reset. Activating a power-on reset will cause all	
	high pulse to this pin, the microcontroller will reset and terminate all activities.	
	1. Pin 9 is the RESET pin. It is an input and is active high (normally low). Upon applying a	
~113.	Function of RESET:	explanatio
c Ans:	Draw and explain reset circuit used for 8051 microcontroller.	4M 2M –
	iv) RD(P3.7) and WR(P3.6): External data memory read and external data memory write.	
	pin should not be floated. (Should be connected to ground).	
	all the instructions are fetched from the external memory. During normal operation, this	
	address the instructions are fetched from external program memory. If this pin is low,	
	executes instruction from the internal program memory till address OFFFH, beyond this	
	iii) <i>EA</i> : EA stands for External access pin and it is active low. When it is held high,	
	chip.	
	used for demultiplexing the address and data by connecting to the G pin of the 74LS373	
	latching the low byte of address during accesses to external memory. The ALE pin is	
	ii) ALE: ALE stands for address latch enable. It is an output pin and is active high for	
	on- chip ROM contains program code.	
	is connected to VCC, these chips do not activate the PSEN pin. This indicates that the	



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	M	10 uF 30 pF 11.0592 MHz 19 2 K 1 X2 30 pF 18 9 RST	2M – Diagram						
	- Tuesday, 149y.14, 2015	Robotics Club, YOR, WRC							
d	Draw the format of PS	W register of $8051\mu$ C and state the function of each flag.	4M						
Ans:	CY AC	F0 RS1 RS0 OV P							
	CY PSW.7	Carry Flag.	2M –						
	AC PSW.6	Auxiliary carry flag.	format						
	F0 PSW.5	Available to the user for general purpose.							
	RS1 PSW.4	Register bank selector bit 1.							
	RS0 PSW.3	Register bank selector bit 0.							
	OV PSW.2	Overflow flag.							
	PSW.1	User- definable bit.							
	P PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to							
		indicate and Odd/ even number of 1 bit in the accumulator.							
	1. CY: Carry flag.								
	1. This flag is set whenever there is a carry out from the D7 bit.								
	2. The flag bit is affected	ed after an 8 bit addition or subtraction.							
	3. It can also be set to	1 or 0 directly by an instruction such as SETB C and CLR C where							
	SETB C stands for set bit carry and CLR C for clear carry.								
	SETEC Statius for set t								
	2. AC: Auxiliary carry f	lag							



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<b>A</b> 113.	<b>i. Stack pointer:</b> The 8-bit stack pointer (SP) register is used to hold an internal RAM	
Ans:		
	iv) Accumulator	
	iii) Program counter	
	ii) DPTR	
	i) Stack pointer	
9	Explain the function of following registers of 8051µC.	4M
	register contains an odd number of 1's, then P=1, P=0 if A has an even number of 1's.	
	1. The parity flag reflects the number of 1s in the A (accumulator) register only. If the A	
	6. P: Parity flag	
	signed arithmetic operations.	
	errors in unsigned arithmetic operations. The overflow flag is only used to detect errors in	
	high-order bit to overflow into the sign bit. In general, the carry flag is used to detect	
	This flag is set whenever the result of a signed number operation is too large, causing the	
	5. OV: Overflow flag	
	1 0 Bank2 (10H-17H) 1 1 Bank3 (18H-1FH)	
	0 1 Bank 1 (08H-0FH)	
	0 0 Bank 0 (00H- 07H)	
	RS1 RS0 Space in RAM	
	of four registers banks in internal RAM.	
	table. By writing zeroes and ones to these bits, a group of registers R0- R7 can be used out	
	1. These two bits are used to select one of the four register banks n internal RAM in the	2M - functions
	4. RS0, RS1: Register bank selects bits	
	<b>3. F0:.</b> Available to the user for general purposes	
	arithmetic.	



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		1
	ii. DPTR : The DPTR register is made up of two registers named as DPH & DPL which are	
	used to access any memory address that may be internal & external code access &	
	external data access. The DPTR is under the program control & can also be specified as 16-	
	bit pointer as DPTR or by individual 8- bits as DPH & DPL. DPTR does have a single address	
	but the DPH is assigned the address as 82 H.	
	iii. Program counter: The program counter (PC) is a 16-bit register. It is used to hold	
	address of a byte in memory. Program instruction bytes are fetched from locations in	
	memory that are addressed by PC. Program ROM may be on chip at addresses 0000H to	
	OFFF H, external to the chip for addresses that exceeds OFFF h or totally external for all	
	addresses from 0000H to FFFF H. The PC is incremented automatically after every	
	instruction byte is fetched. The PC is the only register that does not have any address.	
	iv. Accumulator: It is also called as register A. It is an 8- bit register. The CPU of 8051 is	
	accumulator based hence it is used to hold the source operand and result of arithmetic	
	operations like addition, subtraction, multiplication, division. However it is source as well	
	as destination for logical operations and data movement instructions. It can be used as a	
	look up table pointer. It is also used in RAM expansion. It is specially used for rotate, parity	
	computation, testing for zero etc. It is bit accessible.	
f	What is bus? Describe the function of address, data and control bus.	4M
Ans:	A Bus is a set of physical connection used for communication between CPU and	
	peripherals.	1M
	There are three types of buses Address Bus, Data Bus and Control Bus	
	(1) Address Bus	
	• The address bus is unidirectional over which the microcontroller sends an address	
	code to the memory or input/output. The size of the address bus is specified by the	
	number of bits it can handle.	
	• The more bits there are in the address bus, the more memory locations a	
	microcontroller can access. A 16-bit address bus is capable of addressing (64k)	
	addresses.	
	• The more bits there are in the address bus, the more memory locations a microcontroller can access. A 16-bit address bus is capable of addressing (64k)	



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(2) Da
•
(3) Co
•



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3		Attempt any FOUR:	16- Total Marks
	а	Explain the following directives with example. i) ORG ii) DB iii) EQU (iv) END	4M
	Ans:	ORG:-ORG stands for Origin Syntax: ORG Address The ORG directive is used to indicate the beginning of the address. The number that comes after ORG can be either in hex or in decimal. If the number is not followed by H, it is decimal and the assembler will convert it to hex. Some assemblers use — .ORG (notice the dot) instead of —ORG for the origin directive. DB:- (Define Byte) Syntax: Label: DB Byte Where byte is an 8-bit number represented in either binary, Hex, decimal or ASCII form. There should be at least one space between label & DB. The colon (:) must present after label. This directive can be used at the beginning of program. The label will be used in program instead of actual byte. There should be at least one space between DB & a byte. EQU: Equate It is used to define constant without occupying a memory location.	1M each



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	Syntax: Label EQU Numeric value	
	By means of this directive, a numeric value is replaced by a symbol.	
	For e.g. MAXIMUM EQU 99 After this directive every appearance of the label —MAXIMUM in	
	the program, the assembler will interpret as number 99 (MAXIMUM=99).	
	END:	
	This directive must be at the end of every program meaning that in the source code anything	
	after the END directive is ignored by the assembler.	
	This indicates to the assembler the end of the source file.	
	Once it encounters this directive, the assembler will stop interpreting program into machine	
	code.	
	e.g. END ; End of the program.	
b	State any four addressing mode of 8051 $\mu C$ and explain each with example.	4M
Ans:	There are a number of addressing modes available to the 8051 instruction set, as follows:	1M
	1. Immediate Addressing mode	each
	2. Register Addressing mode	(½ M - explana
	3. Direct Addressing mode	tion,
	4 Register Indirect addressing mode	½ M -
	5. Relative Addressing mode	exampl
	6. Absolute addressing mode	e)
	7. Long Addressing mode	
	7. Long Addressing mode	
	<ul><li>7. Long Addressing mode</li><li>8. Indexed Addressing mode</li></ul>	
	<ul> <li>7. Long Addressing mode</li> <li>8. Indexed Addressing mode</li> <li>1) Immediate Addressing mode:</li> </ul>	
	<ul> <li>7. Long Addressing mode</li> <li>8. Indexed Addressing mode</li> <li>1) Immediate Addressing mode:</li> <li>Immediate addressing simply means that the operand (which immediately follows the</li> </ul>	
	<ul> <li>7. Long Addressing mode</li> <li>8. Indexed Addressing mode</li> <li>1) Immediate Addressing mode:</li> <li>Immediate addressing simply means that the operand (which immediately follows the Instruction op. code) is the data value to be used.</li> </ul>	



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immediate addressing mode is to be used.	
2 ) Register Addressing Mode:	
One of the eight general-registers, R0 to R7, can be specified as the instruction Operand. The	ē
assembly language documentation refers to a register generically as Rn.	
An example instruction using register addressing is :	
ADD A, R5 ; Add the contents of register R5 to contents of A (accumulator) , store sum in A.	
Here the contents of R5 are added to the accumulator and sum stored in A. One advantage	of
register addressing is that the instructions tend to be short, single byte instructions.	
3) Direct Addressing Mode:	
Direct addressing means that the data value is obtained directly from the memory location	
specified in the operand.	
For example consider the instruction:	
MOV R0, 40H; Save contents of RAM location 40H in R0.	
The instruction reads the data from Internal RAM address 40H and stores this in theR0. Direct	ct
addressing can be used to access Internal RAM, including the SFR registers.	
4) Register Indirect Addressing Mode:	
Indirect addressing provides a powerful addressing capability, which needs to be appreciated	d.
An example instruction, which uses indirect addressing, is as follows:	
MOV A, @R0; move contents of RAM location whose address is held by R0 into A	
The @ symbol indicates that indirect addressing mode is used. If the data is inside the CPU,	
only registers R0 & R1 are used for this purpose.	
5) Relative Addressing Mode:	
This is a special addressing mode used with certain jump instructions. The relative address,	
often referred to as an offset, is an 8-bit signed number, which is automatically added to the	:
PC to make the address of the next instruction. The 8-bit signed offset value gives an addres	S
range of + 127 to -128 locations.	
Consider the following example:	
SJMP LABEL_X	
An advantage of relative addressing is that the program code is easy to relocate in memory i	n



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	that the addressing is relative to the position in memory.	
	6) Absolute addressing Mode:	
	Absolute addressing within the 8051 is used only by the AJMP (Absolute Jump) and ACALL	
	(Absolute Call) instructions.	
	7) Long Addressing Mode:	
	The long addressing mode within the 8051 is used with the instructions LJMP and LCALL. The	
	address specifies a full 16 bit destination address so that a jump or a call can be made to a	
	location within a 64KByte code memory space (216 = 64K).	
	An example instruction is:	
	LJMP 5000h; full 16 bit address is specified in operand.	
	8) Indexed Addressing Mode:	
	With indexed addressing a separate register, either the program counter, PC, or the data	
	pointer DTPR, is used as a base address and the accumulator is used as an offset address. The	
	effective address is formed by adding the value from the base address to the value from the	
	offset address. Indexed addressing in the 8051 is used with the JMP or MOVC instructions.	
	Look up tables are easy to implement with the help of index addressing.	
	Consider the example instruction:	
	MOVC A, @A+DPTR	
	MOVC is a move instruction, which moves data from the external code memory space. The	
	address operand in this example is formed by adding the content of the DPTR register to the	
	accumulator value. Here the DPTR value is referred to as the base address and the	
	accumulator value us referred to as the index address.	
:	Draw the software development cycle. State the function of editor, assembler and	4M
	cross compiler.	



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		Assembler: An assembler is programs that translate assembly language program to the	
		correct binary code for each instruction i. e .machine code and generate the file called as	
		Object file with extension . obj and list file with extension .lst extension. Some examples of	
		assembler are ASEM51, Keil A51, AX51, Intel ASM-51etc.	
		<b>Editor:</b> An editor is a program which helps you to construct your assembly language program	
		in right format so that the assembler will translate it correctly to machine language. So, you	
		can type your program using editor. This form of our program is called as source program and	
		extension of program must be .asm or .src depending on which assembler is used. The DOS	
		based editor such as EDIT, WordStar, and Norton Editor etc. can be used to type your	
		program.	
		Cross Compiler:	
		A cross compiler is used to create executable code for a platform other than the one on which	
		the compiler is run. Cross compiling is compiling something for different CPU type than the	
		one you are running on. A cross compiler is used to produce executable (or objects) for a	
		platform other than the local host.	
·	d	Write an ALP for 16 bit multiplication. Assume numbers to be stored in External	4M
		RAM.	
	Ans:	ORG 0000H	4M
		LCALL TRANSFER_IN	
		LCALL MUL_16	
		LCALL TRANSFER_OUT	
		TRANSFER_IN:	
		MOV DPTR, #ADD_FIRSTBYTE	
		MOV R0, #04H	
		MOV R1, #04H	



# SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

Subject Code:

	MOV @R0, A		
	INC R0		
	INC DPTR		
	DJNZ R1,HERI	E	
	RET		
	MUL_16:		
	;Multiply R5 b	y R7	
	MOV A,R5	;Move the R5 into the Accumulator	
	MOV 0F0H,R7	';Move R7 into F0H	
	MUL AB	;Multiply the two values	
	MOV R2,0F0H	;Move B (the high-byte) into R2	
	MOV R3,A	;Move A (the low-byte) into R3	
	;Multiply R5 b	y R6	
	MOV A,R5	;Move R5 back into the Accumulator	
	MOV 0F0H,R6	;Move R6 into B	
	MUL AB	;Multiply the two values	
	ADD A,R2	;Add the lower byte into value in R2	
	MOV R2,A	;Move the resulting value back into R2	
	MOV A,0F0H	;Move the high-byte into the accumulator	
	ADDC A,#00h	;Add zero (plus the carry, if any)	
	MOV R1,A	;Move the resulting answer into R1	
	MOV A <i>,</i> #00h	;Load the accumulator with zero	
	ADDC A,#00h	;Add zero (plus the carry, if any)	
	MOV R0, A	;Move the resulting answer to R0.	



# SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

Subject Code:

;Multiply R4 by R7	7	
MOV A,R4	;Move R4 into the Accumulator	
MOV 0F0H,R7	;Move R7 into B	
MUL AB	;Multiply the two values	
ADD A,R2	;Add the low-byte into value in R2	
MOV R2,A	;Move the resulting value back into R2	
MOV A,0F0H	;Move the high-byte into the accumulator	
ADDC A,R1	;Add the current value of R1 (plus carry)	
MOV R1,A	;Move the resulting answer into R1.	
MOV A,#00h	;Load the accumulator with zero	
ADDC A,R0	;Add the current value of R0 (plus carry)	
MOV R0,A	;Move the resulting answer to R1.	
;Multiply R4 by R6	5	
MOV A,R4	;Move R4 back into the Accumulator	
MOV 0F0H,R6	;Move R6 into	
MUL AB	;Multiply the two values	
ADD A,R1	;Add the low-byte into the value in R1	
MOV R1,A	;Move the resulting value back into R1	
MOV A,0F0H	;Move the high-byte into the accumulator	
ADDC A,R0	;Add it to the value already in R0 + carry	
MOV R0,A	;Move the resulting answer back to R0	
RET	;Return(answer is now in R0, R1, R2,R3)	
;Answer stored in	r0(msb),r1,r2,r3(lsb)	
TRANSFER_OUT:		
MOV DPTR, #ADD	ANSBYTE	



# SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

Subject Code:

	SETB PSW.3			
	MOV R0, #00H			
	MOV R1, #04H			
	THERE: MOV A, @R0			
	MOVX @DPTR, A			
	INC RO			
	INC DPTR			
	DJNZ R1,THERE			
	BACK: SJMP BACK			
	;			
	; (Marks can be given for any oth	ner relevant logic)		
e			priorities.	4M
	(Marks can be given for any oth		priorities.	
	(Marks can be given for any oth		priorities.	
	(Marks can be given for any oth List interrupt of 8051 μC with t Interrupt Source External Interrupt 0 –	heir vector addresses and		2M- li
	(Marks can be given for any oth List interrupt of 8051 μC with t Interrupt Source External Interrupt 0 – INT0	heir vector addresses and Vector address 0003H	Interrupt priority 1	2M- li 1M vecto
e Ans:	(Marks can be given for any oth List interrupt of 8051 μC with t Interrupt Source External Interrupt 0 – INT0 Timer 0 Interrupt	heir vector addresses and Vector address 0003H 000BH	Interrupt priority       1       2	2M- li
	(Marks can be given for any oth List interrupt of 8051 μC with t Interrupt Source External Interrupt 0 – INT0 Timer 0 Interrupt External Interrupt 1 –	heir vector addresses and Vector address 0003H	Interrupt priority 1	2M- li 1M vector addre
	(Marks can be given for any oth List interrupt of 8051 μC with t Interrupt Source External Interrupt 0 – INT0 Timer 0 Interrupt	heir vector addresses and Vector address 0003H 000BH	Interrupt priority       1       2	2M- li 1M vector addre , 1M



# SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

17534

Q N o	Sub Q. N.	Answers	Markin g Schem e
4	а	Attempt any THREE:	12- Total Marks
	i	Classify the instruction set of microcontroller 8051. List one example of each.	4M
	Ans:	Instruction set can be classified as:	2M-
		1. Data transfer instructions	classifi cation,
		2. Arithmetic instructions	2M examp
		3. Logical Instructions	le
		4. Control transfer instructions	
		5. Bit manipulation instructions	
		Data Transfer Instructions:	
		MOV A, Rn: The contents of registers Rn (R0-R7) is moved to Accumulator.	
		(for any other data transfer instructions marks can be given)	
		Arithmetic Instructions:	
		ADD A, Byte: Add the contents of Accumulator with byte and the result is stored in Accumulator.	
		(for any other arithmetic instructions marks can be given)	
		Logical Instructions:	
		RR A: Rotate the contents of Accumulator to right.	
		(for any other logical instructions marks can be given)	
		Control Transfer Instructions:	
		JNC ADDR: If carry flag CY=0, jump to the given relative address.	
		(for any other control transfer instructions marks can be given)	
		Bit Manipulation Instructions:	



# SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

Subject Code:

	(for any othe	r bit manipulation	instructions marks	can be given)			
	Draw and de	escribe IE register	r of 8051 μC.				4M
ns:							2M - form
	IE: INTE	RRUPT ENABL	E REGISTER. B	IT ADDRESS	ABLE.		20.4
	If the bit is	0. the corresponding	interrupt is disabled. I	If the bit is 1, the	corresponding int	errupt is enabled	2M desc
	EA	- ET2		EX1 ET0	EXO	cirupi is cimordi.	ptio
	- here					COMPANY STREET, MARCHINE	ption
	EA I	IE.7 Disables all in source is indiv	terrupts. If $EA = 0$ , n vidually enabled or dis	abled by setting or	clearing its enab	EA = 1, each interrupt le bit.	
	- 1		ited, reserved for futur		Construction of the second	CANS I HAD I	
	ET2 1	IE.5 Enable or disa	able the Timer 2 overfl	low or capture inte	rrupt (8052 only)	A sheming or loss of the	
	ES 1	IE.4 Enable or disa	ible the serial port inte	rrupt.			
	ETI I	IE.3 Enable or disa	ible the Timer 1 overfl	low interrupt.			
	EX1 I		ible External Interrupt				
	ETO I		ble the Timer 0 overfl				
	EX0 1	E.0 Enable or disa	ble External Interrupt	0.			
	With the he	lp of neat diagrar	n, describe the ti	mer modes of	8051 μC.		4M
ns:							1M
							each
	M1	M0	MODE	DESCRIPT	TION		
1		0	0	13-bit time			
	0			16-bit time	r		
	0	1	1				
	0 1	0	2	8-bit auto-1	reload		
	0				reload		
	0 1 1 Operating mod	0 1	2	8-bit auto-1 Split mode	eload		
	0 1 1 Operating mod	0 1 des of Timer: The timer	2 3	8-bit auto-1 Split mode	eload		
	0 1 1 Operating mod byM1 and M0	0 1 des of Timer: The timer ) bit in TMOD register. Mode 0	2 3	8-bit auto-1 Split mode	eload		
	0 1 1 Operating mod byM1 and M0	0 1 des of Timer: The timer ) bit in TMOD register.	2 3	8-bit auto-r Split mode the four modes that a	eload		
	0 1 1 Operating mod byM1 and M0	0 1 des of Timer: The timer ) bit in TMOD register. Mode 0 Timer	2 3 The may operate in any of t	8-bit auto-1 Split mode	eload		



### **SUMMER-18 EXAMINATION**





### SUMMER- 18 EXAMINATION

Subject Name: Micro controller Model Answer

Subject Code:

	Time=1/1MHz=1µs	
	Given frequency =10KHz,	
	Time Period (T)= 1/10kHz= 0.1ms,	
	Ton=Toff=T/2,	
	Delay= 0.1ms/2= 0.05ms	
	0.05ms/1µs=50	
	Therefore count to be loaded in TH0 and TL0 can be calculated as 65536- 50=65486d=FFCEH	
	Program:	
	MOV TMOD,#01H	
	UP: SETB P1.7	
	ACALL DELAY	
	CLR P1.7	
	ACALL DELAY	
	SJMP UP	
	DELAY: MOV TH0,#0FFH	
	MOV TL0,# 0CEH	
	SETB TRO	
	JNB TF0,\$	
	CLR TFO	
	CLR TRO	
	RET	
	END	
-		



# SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

Subject Code:

В	Attempt any ONE:		6- Tota Mar
I	•	C to find smallest numbers from the array of 10 numbers stored in n 3000 H to onwards. Store result at 6000 H. (assume suitable data)	6M
Ans:	Program:		6M
	CLR PSW.3	; Select Bank 0 PSW.3	
	MOV R1, 0AH	; Initialize byte counter	
	MOV DPTR, # 3000H	; Initialize memory pointer	
	DEC R1	; Decrement byte counter by 1	
	MOVX A, @DPTR	; Load number in accumulator	
	MOV 40 H, A	; Store number in memory location	
	UP: INC DPTR	; Increment memory pointer by 1	
	MOVXA, @DTPR	; Read next number	
	CJNE A, 40 H, DN	; if number≠ next number, and then go to DN	
	DN: JNC NEXT	; If next number > number then go to NEXT	
	MOV 40H, A	; Else replace n ext number with number	
	NEXT: DJNZ R1, UP	; Decrement byte counter by 1, if byte counter≠ 0 then go to UP	
	MOV DPTR,#6000H	; Increment memory pointer by 1	
	MOV A, 40H		
	MOVX@ DPTR, A	; Store result t external memory location	
	LOOP: AJMP LOOP	; Stop	
li		gram of stepper motor with 8051 microcontroller. Write an assembly ate the stepper motor continuously in anti-clockwise direction. <sup>9</sup> /step.	6M
Ans:			6M



### **SUMMER- 18 EXAMINATION**

Subject Name: Micro controller

Model Answer

Subject Code:

17534



### **PROGRAM:**

Bit pattern for code for Half Stepping (0.9<sup>0</sup>) Stepper Motor for Anticlockwise rotation

A	В	С	D	CODE
0	0	1	1	03H
0	0	1	0	02H
0	1	1	0	06H
0	1	0	0	04H
1	1	0	0	0CH
1	0	0	0	08H
1	0	0	1	09H
0	0	0	1	01H
0	0	1	1	03H

### ORG 0000H

REP: MOV DPTR, #COD



### **SUMMER- 18 EXAMINATION**

17534 **Model Answer** Subject Code: Subject Name: Micro controller MOV R2, #08H UP: MOV A, #00H MOVC A, @A+DPTR MOV P1, A ACALL DELAY INC DPTR DJNZ R2, UP SJMP REP DELAY: MOV R3, #0FFH AGAIN: MOV R4,#0FFH DJNZ R4,\$ DJNZ R3, AGAIN COD: DB 03H,02H,06H,04H,0CH,08H, 09H,01H HERE : SJMP HERE Draw interfacing diagram of 2K byte EPROM and 2K byte RAM to 8051 µC. Draw memory map. lii 6M 3M Ans: interfa cing, 3M memo ry mappi ng



### **SUMMER- 18 EXAMINATION**

Subject Name: Micro controller

Model Answer

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# SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

17534

Q. No.	Sub Q. N.	Answers	Marking Scheme
5		Attempt any FOUR:	16- Total Marks
	а	List the I/o ports of 8051 microcontroller and describe alternate function of port 0.	4M
	Ans:	<ul> <li>There are four ports available with 8051 microcontroller as,</li> <li>1. Port 0</li> <li>2. Port 1</li> <li>3. Port 2</li> <li>4. Port 3</li> <li>1. Port 0: It can be used as <ul> <li>a) Simple input/output</li> <li>b) Bidirectional low order address / data bus (AD0 - AD7) for external memory.</li> </ul> </li> </ul>	Listing: 2M, Alternate function: 2M
	b	State operating modes of serial port of IC 8051 microcontroller.	4M
	Ans:	Mode 0 – 8 bit shift Register In this mode, the serial port works like a shift register and the data transmission works synchronously with a clock frequency of fosc /12. Serial data is received and transmitted through RXD. 8 bits are transmitted/ received at a time. Pin TXD outputs the shift clock pulses of frequency fosc /12, which is connected to the external circuitry for synchronization In Mode 0, the baud rate is fixed at Fosc. / 12.	1M for each mode
		2 Mode 1: 8-bit UART 10 bits are transmitted through TXD or received through RXD. The 10 bits consist of one start bit (which is usually '0'), 8 data bits (LSB is sent first/received first), and a stop bit (which is usually '1'). Once received, the stop bit goes into RB8 in the special function register SCON. The baud rate is variable. Baud Rate = $2^{\text{SMOD}}$ X Oscillator Frequency	
		32 12 X [256 - ( TH1 ) ]	
		Mode 2 : 9-bit UART.	
		In this mode 11 bits are transmitted through TXD or received through RXD.The various bits are as follows: a start bit (usually '0'), 8 data bits (LSB first), a programmable 9 th (TB8 or RB8)bit and a stop bit (usually '1'). While transmitting, the 9 th data bit (TB8 in SCON) can be assigned the value '0' or '1'. For example, if the information of parity is to be transmitted, the parity bit (P) in PSW could be moved into TB8.On reception of the data, the 9 th bit goes into RB8 in 'SCON', while the stop bit is ignored.	



# SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

Subject Code:

	Baud Rate = $\frac{2^{\text{SMOD}}}{64}$ X (Oscillator Frequency)	
	4. Mode 3: 9-Bit UART with Variable Baud Rate	
	In this mode 11 bits are transmitted through TXD or received through RXD. The various bits are: a start bit (usually '0'), 8 data bits (LSB first), a programmable 9 th bit and a stop bit (usually '1'). Mode-3 is same as mode-2, except the fact that the baud rate in mode-3 is variable (i.e., just as in mode-1).	
	Baud Rate = $\frac{2^{\text{SMOD}}}{32} \times \frac{\text{Oscillator Frequency}}{12 \times [256 - (\text{TH1})]}$	
c	Explain SBUF register used with serial-communication with 8051 microcontroller.	4M
Ans:	Serial Buffer register, SBUF is physically two separate registers at the same address. (99H). One is Write-only transmit register and other is Read-only receive register. The byte to be transmitted on the serial port is "written" into SBUF & Serial transmission starts immediately. The byte received from the serial port will be stored	4 <b>M</b>
	in SBUF once the last bit is received.	
d		4M
d Ans:	in SBUF once the last bit is received.	Format:
	in SBUF once the last bit is received. Draw the format of TMOD and state the function of each bit.	
	in SBUF once the last bit is received. Draw the format of TMOD and state the function of each bit. TMOD: TIMER/COUNTER MODE CONTROL REGISTER.	Format:
	in SBUF once the last bit is received. Draw the format of TMOD and state the function of each bit. TMOD: TIMER/COUNTER MODE CONTROL REGISTER. GATE C/T M1 M0 GATE C/T M1 M0	Format: 2M
	in SBUF once the last bit is received. Draw the format of TMOD and state the function of each bit. TMOD: TIMER/COUNTER MODE CONTROL REGISTER. GATE $C/T$ M1 M0 GATE $C/T$ M1 M0 Timer 0 • GATE : When TR <sub>x</sub> (in TCON) is set and GATE=1 , TIMER/COUNTER will run only while INT <sub>x</sub> pin is high( hardware control), when GATE=0 , TIMER/COUNTER will run only while TR <sub>x</sub> =1 regardless of state of INTX pin	Format:
	in SBUF once the last bit is received. Draw the format of TMOD and state the function of each bit. TMOD: TIMER/COUNTER MODE CONTROL REGISTER. GATE C/T M1 M0 GATE C/T M1 M0 Timer 1 Timer 0 • GATE : When TR <sub>X</sub> (in TCON) is set and GATE=1 , TIMER/COUNTER will run only while INT <sub>X</sub> pin is high( hardware control), when GATE=0 , TIMER/COUNTER will run only while TR <sub>X</sub> =1 regardless of state of INTX pin (software control)	Format: 2M Functior



### SUMMER- 18 EXAMINATION

Subject Name: Micro controller

Model Answer

Subject Code:

		M1	<b>M0</b>	MODE	DE	SCRIP	ΓΙΟΝ			
		0	0	0	13-bit timer/counter					
		0	1	1	16 bit tin	ner/coun	ter			
		1     0     2     8 bit auto-reload								
		1	1	3	Split mo	de				
e D	raw and expl	ain the for	rmat of	IP register o	f 8051 mic	rocontro	oller.			41
Ans:	The IP	Register	: INTE	RRUPT PF	RIRIOTY	REGIST	<u>TER</u>			21
	r				DT1	D)/4		51/0	7	
		-	-	- PS	PT1	PX1	PT0	PX0		
		-	-	- PS	PII	PX1	PIO	PXU		
	]	Bit	- Name	- PS			P10	PX0		
			- Name	- PS	Desci	ription	P10	PX0	_	
		IP.7		- PS	Desci	ription erved	P10	PX0		21
			-	- PS	Desci Rese Rese	ription	P10	PX0		21
		IP.7 IP.6	-	- PS	Desci Rese Rese	ription erved erved erved	P10	PX0		21
		IP.7 IP.6 IP.5	- - - PS		Desci Rese Rese Rese	ription erved erved erved riority				21
		IP.7 IP.6 IP.5 IP.4	- - PS PT1	Serial Port Ir	Desci Rese Rese Rese nterrupt prior	ription erved erved erved riority rity (TF1)	)	PX0		21
		IP.7 IP.6 IP.5 IP.4 IP.3	- - PS PT1 PX1	Serial Port In Timer 1 Inte	Desci Rese Rese Rese nterrupt prior errupt 1 pr	ription erved erved riority rity (TF1)	) NT1)	PX0		21
		IP.7 IP.6 IP.5 IP.4 IP.3 IP.2	- - PS PT1 PX1 PT0	Serial Port In Timer 1 Inte External Inte	Desci Rese Rese nterrupt prior errupt 1 pr rrupt prior	ription erved erved riority rity (TF1) riority (IN rity (TF0)	) \\T1)	PX0		21



# SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

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Q. No.	Sub Q. N.	Answers	Marking Scheme
6		Attempt any FOUR:	16- Total Marks
	a	Write ALP for 8051 microcontroller to transmit message 'WELCOME' serially at baud rate 9600, 8 bit data, I stop bit. Assume crystal frequency is 11.0592 MHz.	4M
	Ans:	MOV SCON,#50H ;8-bit, 1 stop, REN enabled (MODE 1) MOV TMDD,#20H ;timer 1,mode 2(autoreload) MOV TH1,#0FDH ;9600 baud rate SETB TR1 ;start timer 1 MOV A,#"W" ;transfer "W" ACALL TRANS MOV A,#"E" ;transfer "E" ACALL TRANS MOV A,#"L" ;transfer "L" ACALL TRANS MOV A,#"C" ;transfer "C" ACALL TRANS MOV A,#"C" ;transfer "C" ACALL TRANS MOV A,#"O" ;transfer "O" ACALL TRANS MOV A,#"W" ;transfer "M" ACALL TRANS MOV A,#"E" ;transfer "E" ACALL TRANS AGAIN:SIMP AGAIN TRANS:MOV SBUF,A ;load SBUF HERE :JNB TI,HERE ;wait for the last bit CLR TI ;get ready for next byte RET	Correct program: 4 marks
	b	What is the role of SMOD bit in serial communication? Write instruction to set SMOD bit.	4M
	Ans:	SMOD bit Doubles the serial communication Baud rate, When set to 1 in modes 1, 2, or 3.	2M



# SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

Subject Code:

	PCON Register:											
		MSB LSB										
		SMOD	_	_	-	GF1	GF0	PD	IDL		2M	
	Instruction to set S	SMOD bit	is <b>MO</b>	V PC	ON, #8	0H.					2111	
C	Describe the fund	ction of fo	ollowi	ng har	ndshak	ing sig	nals o	of 825!	5.		4M	
	i) IBF											
	ii) STB											
	iii) ACK											
	iv) OBF											
Ans:	i) IBF:										Each	
	This is active high output signal generated by 8255 to peripheral. A high on this output indicates that data has been loaded into input latch.											
	ii) STB											
	This is active low input signal to 8255.A low on this input loads data into the input latch. This signal is generated by the peripheral to indicate that data is available on input ports lines.											
	iii) ACK											
	A low on this input informs the 8255 that the data from port A or port B is accepted by the output peripheral In essence peripheral device generates ACK signal indicating that data is accepted from the output port											
	iv) OBF											
										cified port. This		



# SUMMER- 18 EXAMINATION Model Answer

Subject Name: Micro controller

Subject Code:

d	Draw form	nat of SFR S	CON and	explain ea	ch bit of same.				4M
Ans:	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	2M
	SM0 SM1	Serial Po Serial Po	al Port Mode Bit 0,						
	SIVIT	Senal Po SM0	SM1	Mode	Description	Baud	Rate		
		0 0 1 1	0 1 0 1	0 1 2 3	shift register 8-bit UART 9-bit UART 9-bit UART	fosc/′ variat f <sub>OSC</sub> /( variat	ole 64 or f <sub>OSC</sub> /3	32	
	3, is rec <b>REN</b> : Rre	if SM2 is s 0. In Mode ceived. In M eceive enabl	et to 1 t 1, if SM Iode 0 SM le bit. Wh	han RI will 2 = 1 then 1 /12 should b	nication feature i not be activated RI will not be act e 0 f = 1, reception is c	if the reco ivated if a	eived 9th d a valid stop	ate bit(RB8) b bit was not	2М
	<ul> <li>reception is disabled.</li> <li><b>TB8</b>: Transfer bit 8 The 9<sup>th</sup> data bit that will be transmitted in modes 2 and 3.</li> <li><b>RB8</b>: Receive bit 8. The 9<sup>th</sup> data bit that was received in modes 2 and 3.In mode 1, this bit is the stop bit that was received.</li> <li><b>TI</b>: Transmit interrupt flag. set by hardware at end of 8<sup>th</sup> bit in mode 0 and at the beginning</li> </ul>							e beginning	
	of the stop bit in other modes, in serial transmission. Must be cleared by software <b>RI</b> : Receive interrupt flag . set by hardware at end of 8 <sup>th</sup> bit in mode 0 and half way through the stop bit time in other modes in serial reception. Must be cleared by software								
e	Describe s	election fac	ctors of m	icrocontro	ller.				4M
Ans:	of microco	0	either 8,	16 or 32 bi	s a microcontroll t. As the word le	-		•	Any four selection factors:
	voltage, V	-	logy etc.	-	rious factors like operated embed				1 mark each
					of an embedded on the application		epends upo	on the clock	
	frequency. 4. Instruct RISC.	The clock f tion Set: O	requency n the bas	depends up is of instru		n. rollers are	e classified	as CISC &	



### **SUMMER- 18 EXAMINATION**

Subject Name: Micro controller

Model Answer

Subject Code:

17534

RISC improves speed of the system for the particular applications.

**5. Internal resources:** The internal resources are ROM, RAM, EEPROM, FLASH ROM, UART, TIMER, watch dog timer, PWM, ADC, DAC, network interface, wireless interface etc. It depends upon the application for which microcontroller is going to be used.

**6. I/O capabilities:** The capability of microcontroller to handle external devices depend upon the number of I/O ports, size and characteristics of each I/O port provided. There may be serial port or parallel ports.

7. Architecture type: Architecture decides complexity and hence cost of the chip. Depending upon application suitable architecture should be selected. Harvard architecture is commonly used.