**Important Instructions to examiners:**

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

**Q1. a) Attempt any THREE of the following:** **12M**

**i. State the necessity of adder and subtractor circuit in PAL-D decoder.**

**Ans} (02 M Diagram,02M Explanation)**

**Explanation:**

- A delay line and adding and subtracting circuits are interposed between the chrominance amplifier and demodulators.
- The object of delay line is to delay the chrominance signal by almost one line period of 64us.
- The chrominance amplifier feeds the chrominance signal to the adder, the subtracter and the delay line.
- The delay line in turn feeds its output to both the adder and subtrater circuit.
- The adder and the subtacter circuits, therefore, receive the two signals simultaneously. These may be referred to any given time as the direct line and delay line signals.
- The adder yields a signal consisting of U information only but with twice amplitude (2U)
- Similarly , the subtraction circuit produces a signal consisting only of V information, with an amplitude twice that of the 'V' modulation product.

**Diagram:**

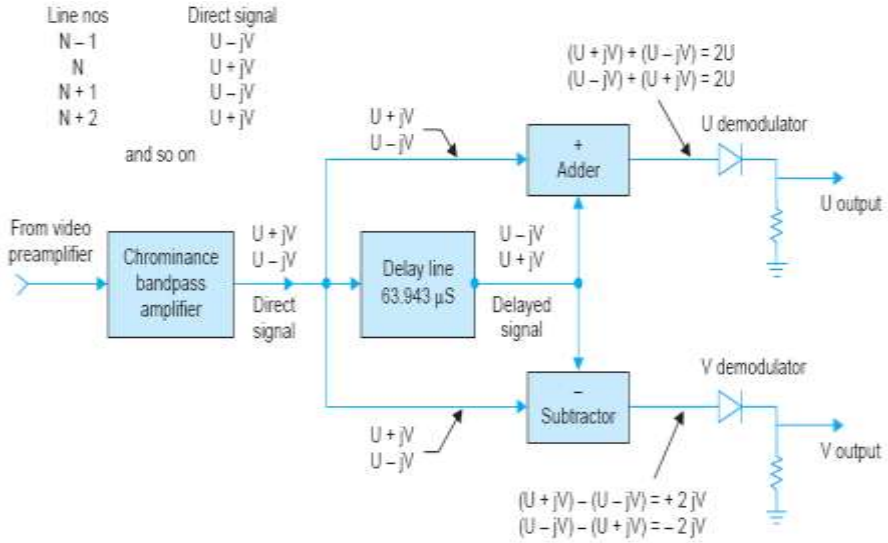



**Figure: Block diagram of PAL-Decoder**

**ii) Draw block diagram of sync. Separator and describe its working.**

**Ans} (02M Diagram, 02M Explanation)**

**Note:-( Any other relevant block diagram should be considered and marks should be given accordingly )**

**Diagram:**

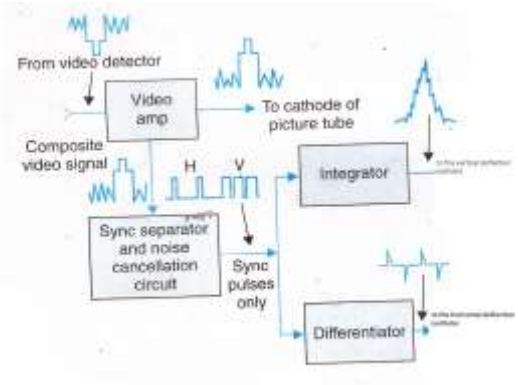



**Figure: Block diagram of sync. Separator**

**Explanation:**

- The sync pulses include horizontal, vertical and equalizing pulses. There are separated from the video signal by the sync separator.
- The clipped line (horizontal) and field (vertical) pulses are processed by appropriate line-pulse and field –pulse circuitry. The sync output thus obtained is fed to the horizontal and vertical deflection oscillators to the time the scanning frequencies.
- As a result , picture information is in correct position on the raster.
- The sequence of the operation is illustrated in figure.
- The problem of taking off the sync pulses from the video waveform is a comparatively simple one, since the action consists of merely biasing the device use in the circuit, in such a way, that only the top potions of the video signal cause current flow in the device.
- This is readily achieved by self-biasing the tube or transistor use in the circuit.

**iii) Justify the use of microcontroller in TV receiver.**

**Ans} (01M each for each use)**

**Note:-( Any other justification use relevant should be considered)**

**Explanation:**

The main thrust of all microcontroller is based control system is channel selection and fine tuning.For this, frequency synthesizer is used which enables crystal accuracy of the local oscillator frequency for all channels. Several facilities that become available in microcontroller controlled system include.

- Auto seek programming
- Manual programming
- Digital ‘LED’ display of the selected channel
- Operation with or without remote control
- AFT control and
- Audio mute during channel hunting.
- For above reasons microcontroller in TV receiver is used.

**iv) Draw construction of SAW filter. Why pre-amplifier is needed before the SAW filter.**

**Ans}(02M Diagram,02 Reason)**

**Diagram:**

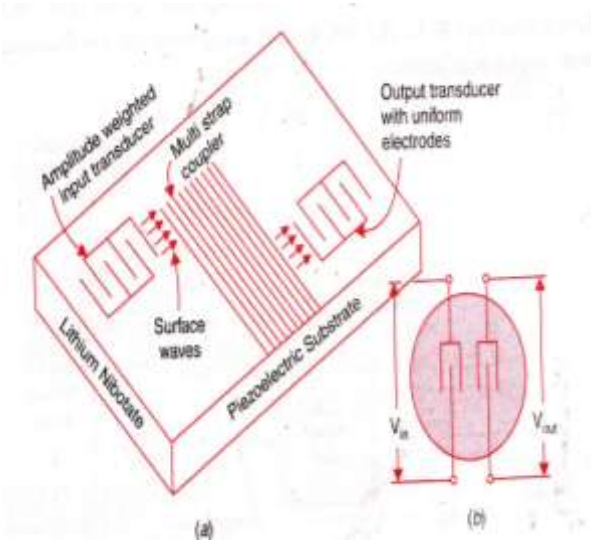



**Figure: Construction diagram of SAW filter**

**Reason for Why pre-amplifier is needed before the SAW filter :-**

- The bandwidth and frequency characteristics of a SAW filter depend on the geometric structure of the input transducer array because the extent of attenuation to desired bands of frequencies.
- A short length of coaxial cable feeds tuner output into a wide-band pre-amplifier that precede the SAW filter .
- IT is necessary to provide this amplifier to compensate for the large uniform attention of the signal that occurs in the SAW filter.
- Practically all the gain and selectivity of the receiver is provided by IF section.
- The use of SAW filter along with it has very much simplified tedious tuning of several trap circuits that formed part of earlier IF subsystems

**b) Attempt any ONE of the following:** **06M**

**i) Draw ckt. Diagram of ident and color killer ckt. And describe its operation.**

**Ans}(03M Diagram,03M Explanation)**

**Color killer control:**

- The color killer circuit is shown in Fig. The forward bias of Q5, the last stage of band pass amplifier depends on the state of the color killer circuit.
- When a color signal is being received, the 7.8 KHz (switching rate of the (R – Y) signal) component is available at the APC (automatic phase control) circuit of the reference subcarrier oscillator.
- It is applied via C1 to the base of tuned amplifier Q6. The amplified 7.8 KHz signal is ac coupled to Q7. Diode D3 conducts on negative half cycles charges the capacitor C2 with the polarity marked across it.
- The discharge current from this capacitor provides forward bias to Q7, the emitter follower. Such an action results in a square wave signal at the output of Q7. It is coupled back via a 680 ohm resistor to the tuned circuit in the collector of Q6.
- This provides positive feedback and thus improves the quality factor of the tuned circuit. The colour killer diode D4 rectifies the square-wave output from the emitter of Q7.

**Diagram:**

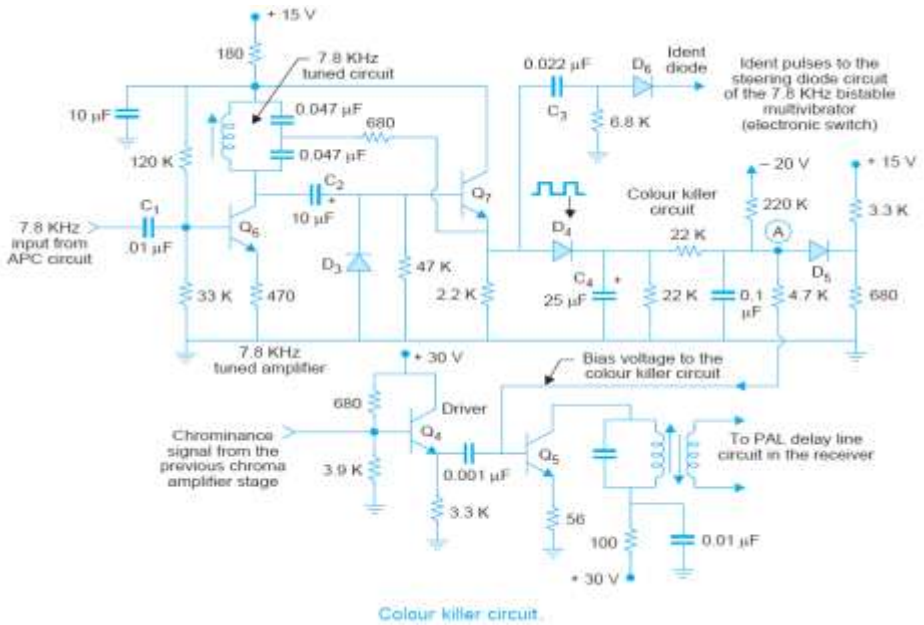



**Figure: Circuit diagram of Color Killer**

- The associated RC filter circuit provides a positive dc voltage at point 'A' and this serves a source of forward bias to the chrominance amplifier Q5. Diode D5 is switched on by this bias and so clamps the voltage produced at 'A' by the potential divider (3.3 K and 680 ohm) across the + 15 V line.
- When a monochrome transmission is received there is no 7.8 KHz input to the colour killer diode D4 and no positive voltage is developed at its cathode (point A).
- Both D5 and the base emitter junction of Q5 are now back biased by the – 20 V potential returned at 'A' via the 220 K resistor. The chrominance signal channel, therefore, remains interrupted.

**OR**

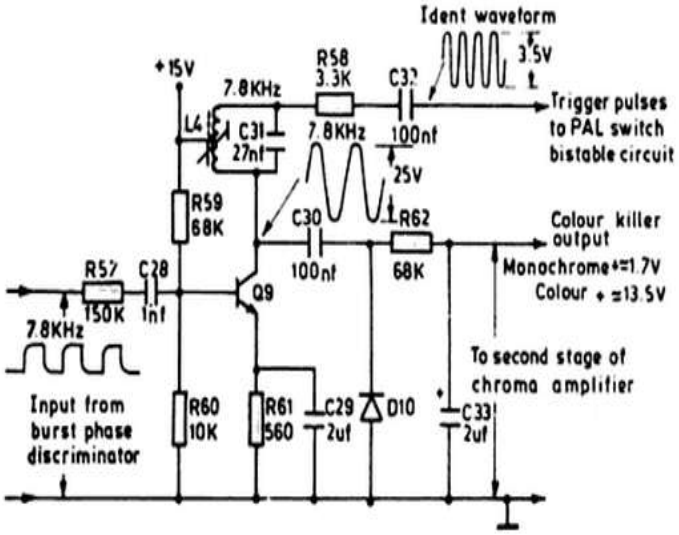



**Figure: Burst phase IDENT amplifier & color –Killer generation circuit.**

- The dc operating voltage to Q9 is supplied via center tap on L4. Such a connection causes L4 to function as a tuned autotransformer & enables a waveform of about 25V peak-to-peak to be developed at the collector of Q9.
- This is fed via C30 to diode D10 which functions as a HWR. The components R62 & c33 form a LPF which provides a steady dc level of about 13.5V as the output. This is the color killer voltage which is used to control conduction of the second stage of Chroma signal amplifier.
- When a black and white picture is being received, there is no output from the burst discriminator & hence, no input to burst phase indent amplifier.

- Under this condition the color killer output fails to less than 2V which is not enough to forward bias transistor of the Chroma amplifier. Thus the second Chroma amplifier stage is inhibited.
- This prevents application of any signal to the Chroma delay line & to the U & V demodulators. Thus any stray coloring signals are prevented from reaching RGB amplifier & hence, no colour noise appears on the black & white picture during monochrome receptions.

**ii) Draw the construction of Trinitron picture tube and describe its working.**

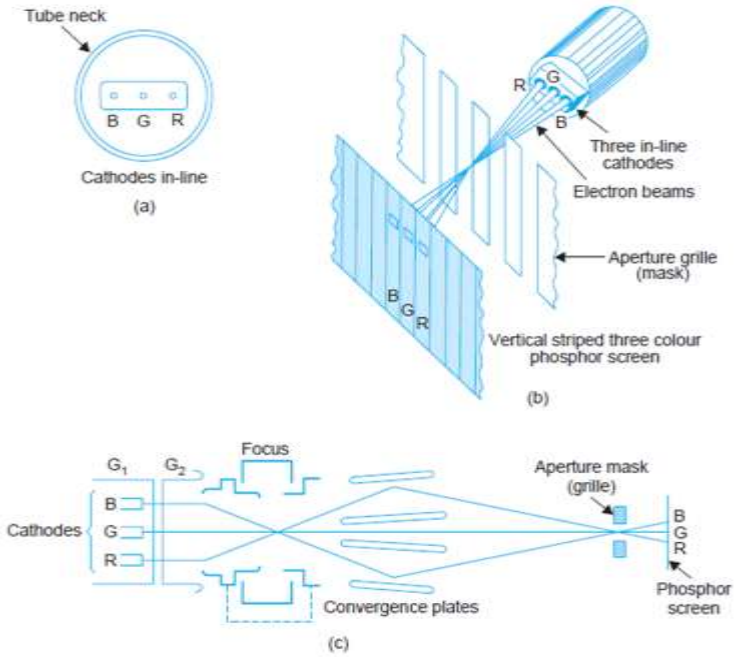
**Ans}(03M Diagram,03M Explanation)**

**Explanation**

**Trinitron:**

- The Trinitron or three in-line cathodes color picture tube was developed by 'SONY' Corporation of Japan around 1970. It employs a single gun having three in-line cathodes. This simplifies constructional problems since only one electron gun assembly is to be accommodated.
- The three phosphor triads are arranged in vertical strips as in the P.I.L. tube. Each strip is only a few thousandth of a centimeter wide. A metal aperture grille like mask is provided very close to the screen.

**Diagram:**




(a) gun structure(b) electron beams, vertical-striped three colour phosphor screen
(c) constructional, focus and convergence details

**Figure: Constructional Diagram of Trinitron**

- It has one vertical slot for each phosphor triad. The grille is easy to manufacture and has greater electron transparency as compared to both delta-gun and P.I.L. tubes. The beam and mask structure, together with constructional and focusing details of the Trinitron are shown in Fig.
- The three beams are bent by an electrostatic lens system and appear to emerge from the same point in the lens assembly. Since the beams have a common focus plane a sharper image is obtained with good focus over the entire picture area. All this simplifies convergence problems and fewer adjustments are necessary.

**Q2.Attempt any FOUR of the following:** **16M**

**a) Draw the block diagram of SMPS. State the function of each block.**

**Ans}(02M Diagram,02 Explanation)**

**Explanation:**

SMPS is the non dissipative regulator which operates by chopping the regulated DC supply voltage, at high frequency 15,625KHZ by using switching transistors. And when filtered by high voltage rectifier and capacitors.

**Diagram:**

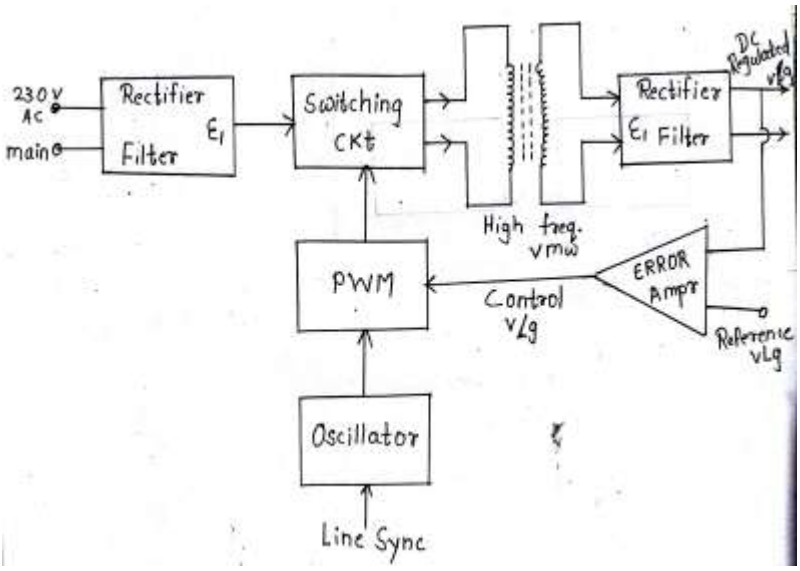


**Figure: Block diagram of SMPS**

**Working:-**

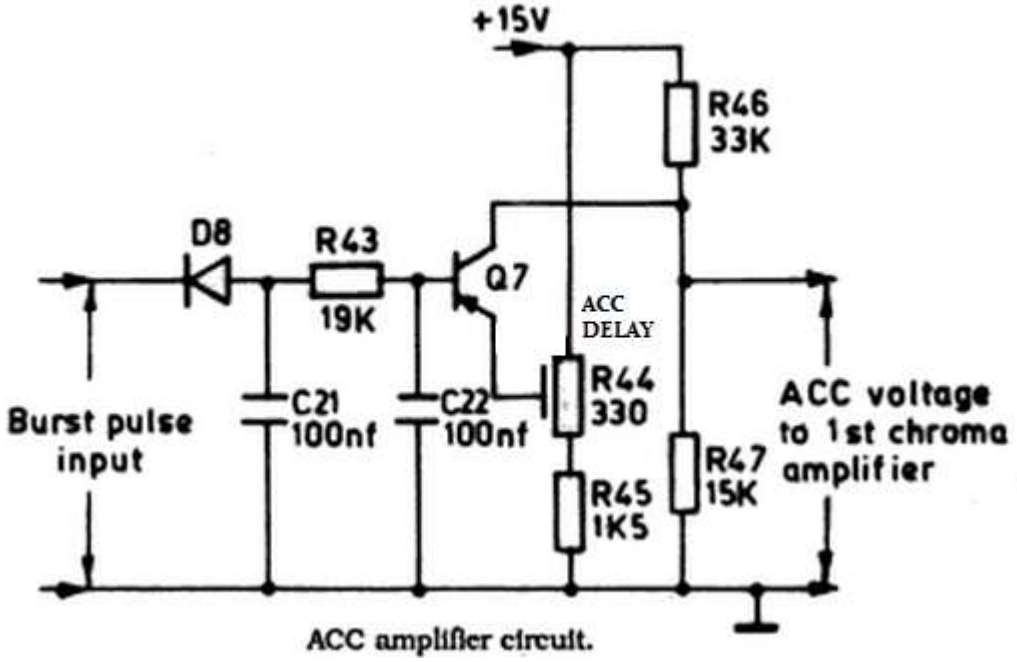
1. The unregulated DC voltage is applied to the switching circuit .
2. The switching circuit consist of a transistor driven by pulse width modulation(PWM). It chops the input DC voltage at the high frequency.
3. The chop DC voltage is applied to the rectifier circuit through the high frequency transformer.
4. The transformer may be step up or step down or coupling transformer.
5. The amplifier samples the input voltage & controls the pulse width of the PWM.
6. The PWM in turn controls the switching time of transistor & proportionally varies the output voltage.

**b) Draw ckt. Diagram of ACC amplifier and describe its working.**

**Ans} (02M Diagram,02 Explanation)**

**ACC Amplifier:**

- The amplified burst signal that become available at the output of gated burst amplifier is also fed to diode D8 of the automatic colour control amplifier circuit as shown in fig.




ACC amplifier circuit.

- The diode together with filter (C21, R43, and C22) acts as a HWR-cum-filter to develop a negative going dc voltage at the base of Q7, which is proportional to the strength of received signal.
- As stated C21, R43 & C22 from a LPF to smooth any 4.43MHz variations present in the rectified signal. The output voltage at the collector of transistor Q7 is a positive voltage which increases or decreases with the strength of Chroma signal.
- This positive voltage is typically 7V under normal signal strength conditions. The resistor R44 provides an adjustable reverse bias for Q7 to delay its conduction until the Chroma signal exceeds a given threshold.
- The potentiometer formed by resistors R46 & R47 is used to obtain correct steady bias for the first Chroma amplifier. It is also necessary for making the collector of transistor Q7, negative w.r.t. its emitter.

**c) Illustrate the operation of forward SMPS with neat circuit diagram**.

**Ans}(02M Diagram,02 Explanation)**

**Diagram:**

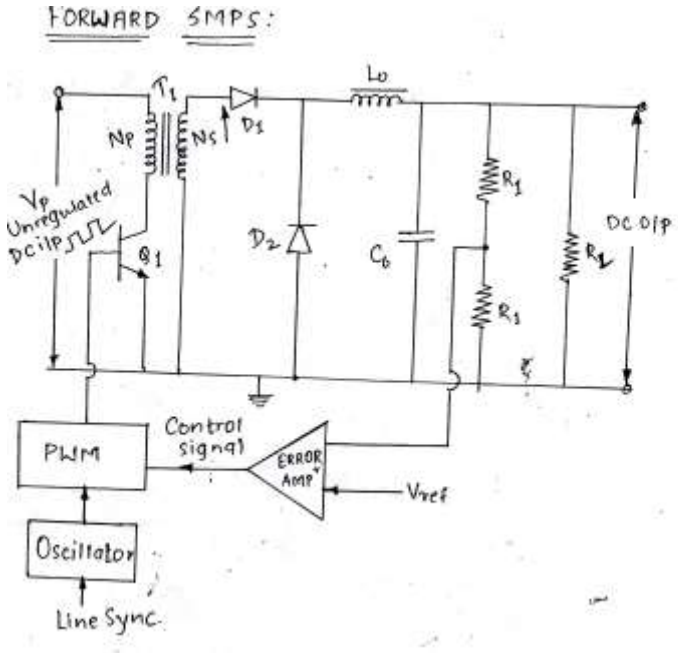



**Figure : Circuit diagram of Forward SMPS**

**operation:**

- Unregulated DC input voltage is taken from main supply by simple diode rectifier and connected to the series circuit of primary winding of Transformer T1 and switching transistor Q1.
- The conduction of Q1 is controlled by varying width of pulse fed at its base from a pulse width modulation(PWM).
- PWM is driven by error amplifier and oscillator.
- The oscillator generates a rectangular pulse of constant duration & am[plifier whose frequency is synchronized to the horizontal oscillator.
- The error amplifier controls the pulse width of pulse width modulation by applyin controlled voltafe .It compares reference voltage and error signal obtained from resistor voltage divider of R1,R2 to generate the control signal.
- When the transistor Q1 is ON. Input voltage is applied to the primary winding of transformer T1or rising current in Np produce polarity voltage. At the upper end Ns.
- Thus , diode D1 conducts during ON period of transistor Q1 to store energy in L0 & C0 & also feed load current . Diode D2 stays reverse biased during this interval.
- As soon as transistor Q1 turns 'OFF' the decreasing currents in Np induces a voltage across ns i.e of opposite polarity.
- Diode D1 is thus reverse biased & no transfer of energy to the load circuit takes place.
- However, the energy stored in L0 and C0 is transferred to the node circuit
- Since the diode D1 conducts & store energy when Q1 is on , its is called as forward SMPS.

**d) State the purpose of remote control system in TV. State its advantages and disadvantages.**

**Ans}(02M for Purpose,01M Advantage and 01M disadvantage)**

**Note:-( Any other relevant advantages and disadvantages should be considered)**

**Explanation:**

Based on the design of the remote control unit and type and make of the receiver, it is possible to control as many as five different functions. These include volume-up and on-off, volume-down, channel selection, color-up, color-down etc. Though a variety of remote control television system are in use.

**Advantages:**

- Audio muting option is available.
- TV can be programmed by remote control system.
- User can make their own set of selected channels**.**

**Disadvantages:**

- It requires line of site.
- Range of IR sensor is less compared to any other wireless communication components.
- Latest Tv do not have power on/OFF button on the Tv so if remote is faulty Tv cannot be stay off condition means it goes in standby mode which ultimately cause loss of power.
-

**e) State the features of plasma TV (any four).**

**Ans}(01M each for each features)**

**Explanation:**

**Features of plasma TV:**

- There is no flicker as all the phosphor excited pixels react at the same time during one frame of scanning.
- There is also no back light and no protection of any kind.
- As , such the light emitting phosphors result in bright pictures with rich colors and wide viewing angle.
- Though plasma screens are thin, they are heavy and consume lot of power.
- These are also fragile and often need professional help to install them.
- Capable of producing deeper blacks allowing for superior contrast ratio.
- Wider viewing angles than those of LCD.
- Less visible motion blur.
- Superior uniformity.

- Unaffected by clouding from the polishing process.
- Less expensive for the buyer per square inch than LCD

**f) Draw the block diagram of remote control transmitter and receiver.**

**Ans} (02M for transmitter,02M Receiver)**

**Diagram:**

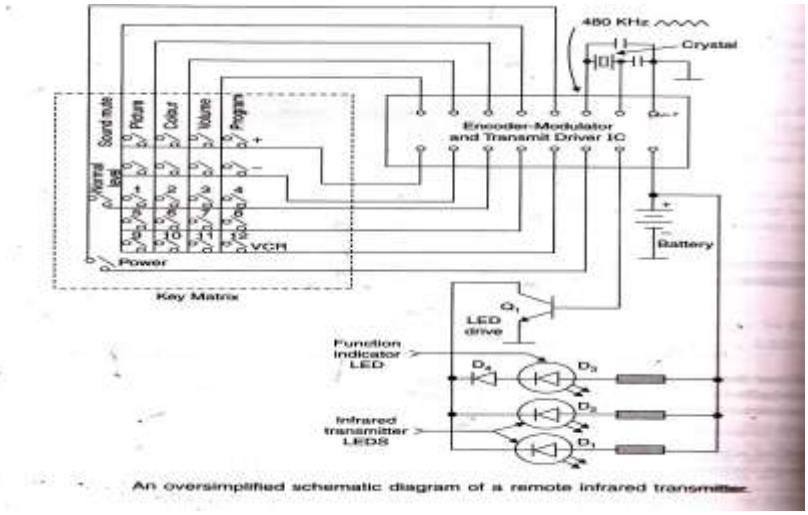



**Figure: Oversimplified schematic diagram of a remote infrared transmitter.**

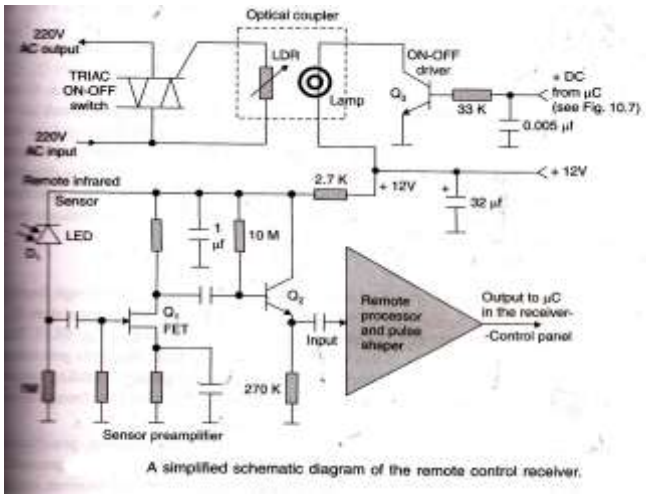


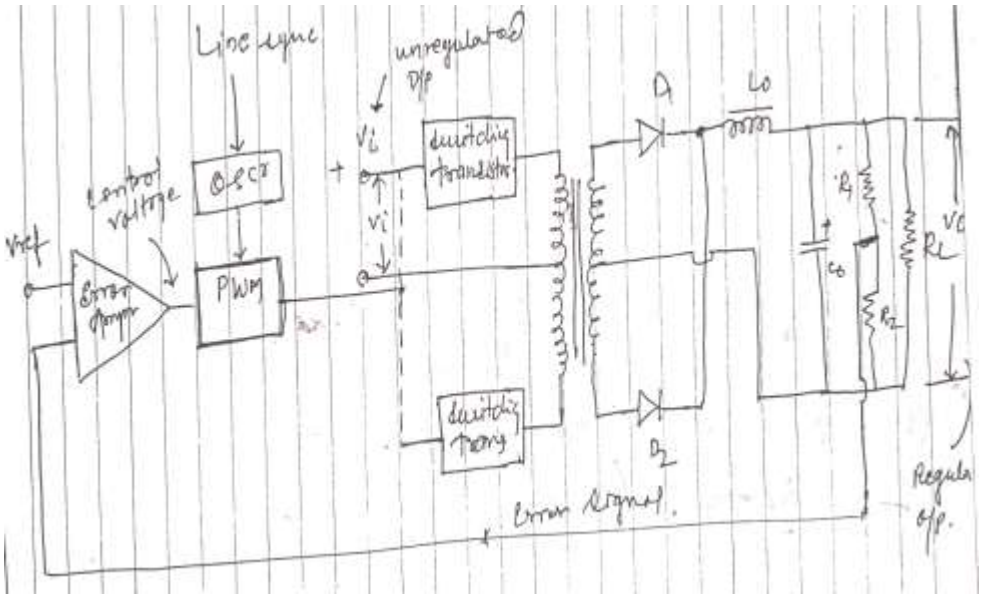

**Figure: A simplified schematic diagram of remote control receiver.**

**Q.3 Attempt any FOUR of the following: 16M**

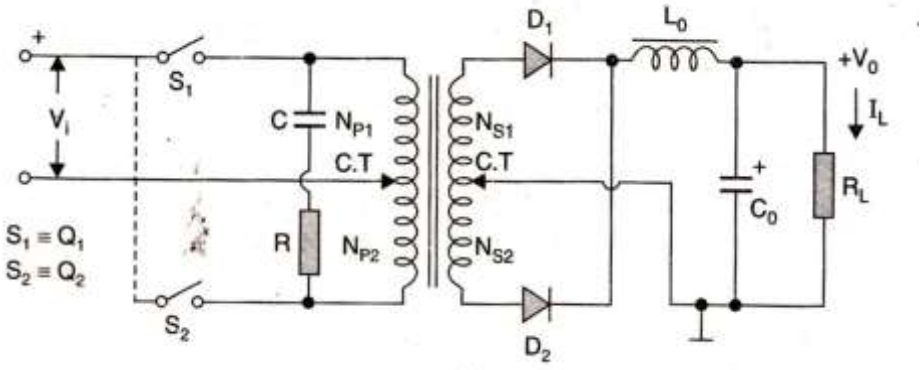
**a) Draw the block diagram of push-pull SMPS and state the function of each block.**

**(Diagram- 2Marks, Function of each block- 2 Marks)**

Ans: **Block Diagram:**




**OR**




**Explanation:**

- **Switches S1 and S2** represents two transistors that are necessary for transfer of energy from unregulated source Vi to the load circuit. The two transistor conduct alternately by opposite polarity pulses from the pulse width modulator.
- Thus **D1 and D2 conduct alternately** as in a conventional full-wave rectifier circuit.
- The **choke $L_0$** and filter **capacitor $C_0$** store energy to maintain steady voltage across the load.

- The **feedback circuit** operates in the same manner to actuate the PWM in such a way that conduction periods of switching transistors vary in accordance with variation in load current thus maintains output voltage constant at $V_0$.

**b) Draw the block diagram of microcontroller based TV.**

**(4 Mark for Correct diagram, Any other relevant diagram should also be given marks)**

Ans: **Diagram:**

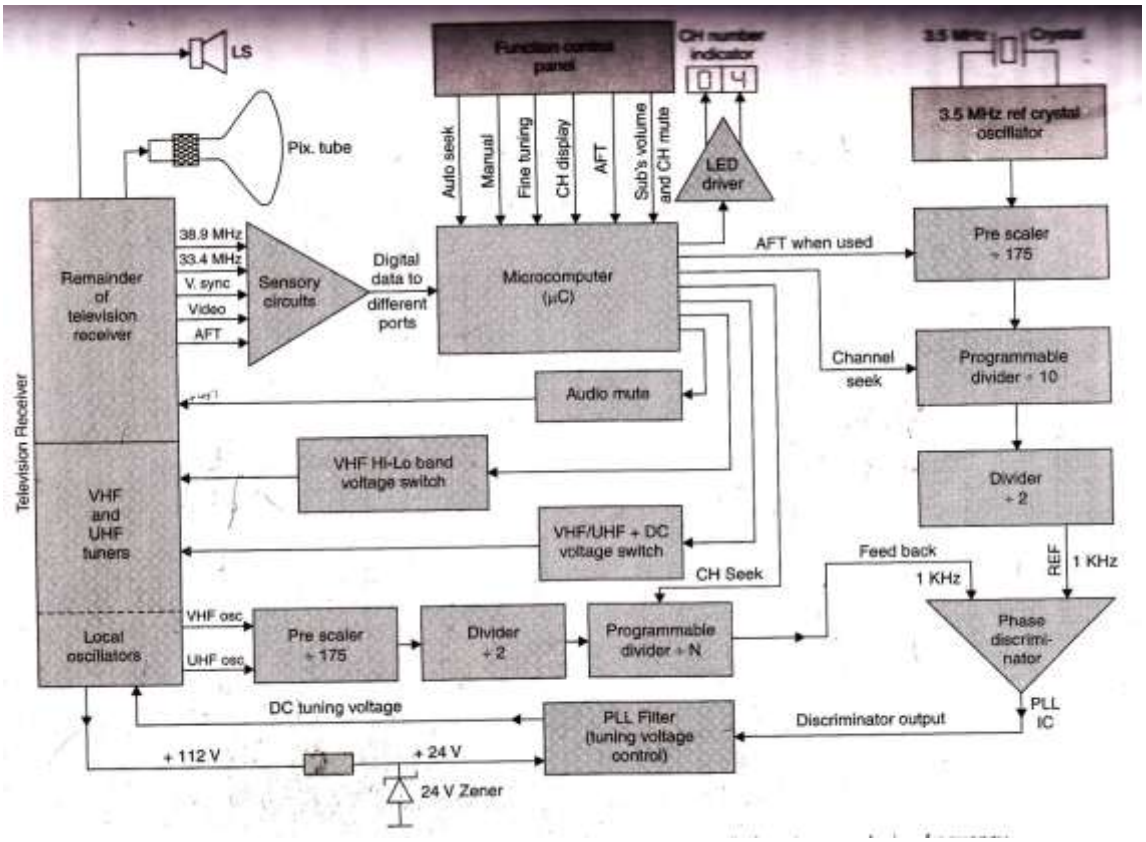



**Figure: Block diagram of microcontroller based TV**

**c) Draw the block diagram of VIF stage in colour TV receiver and draw its response curve.**

**(Block Diagram-2 Mark, Response Curve- 2Mark)**

**Ans: Diagram:**

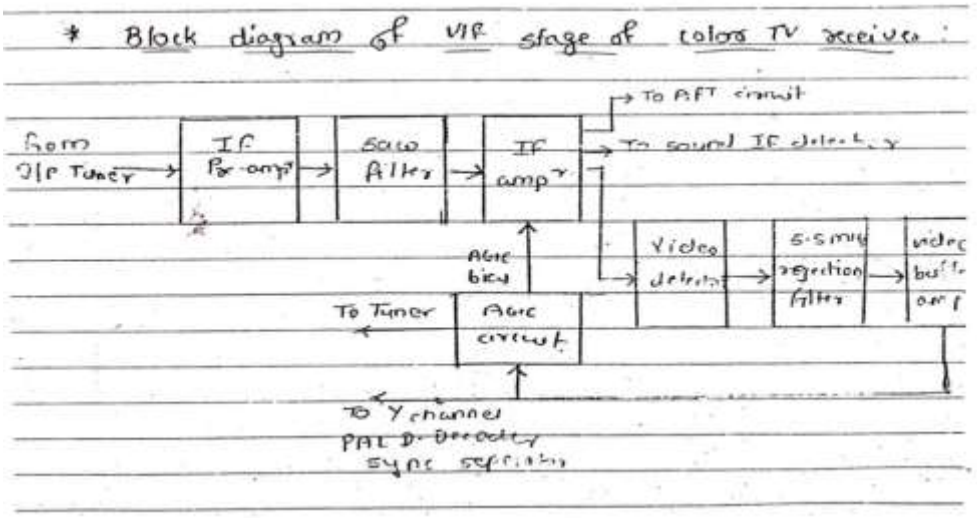



**Figure: Block diagram of VIF stage of color Tv receiver**

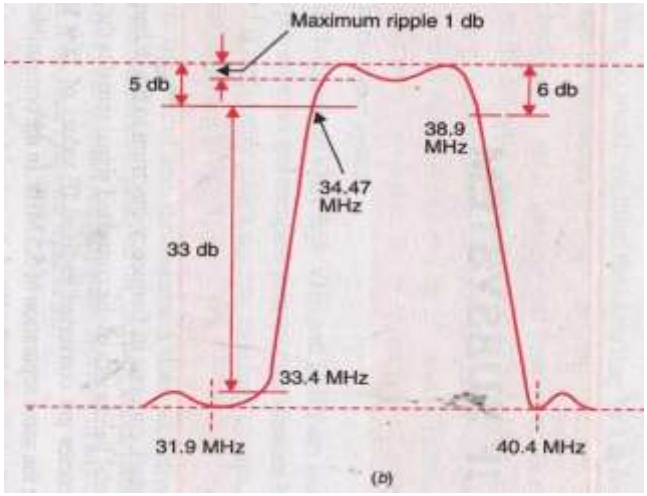



**Figure: Response curve of VIF stage color TV receiver**

**d) Draw circuit diagram of reference oscillator and state its need in PAL-D decoder**

**(Diagram-2 Marks, Need- 2 Marks)**

Ans: **Diagram of reference oscillator:**

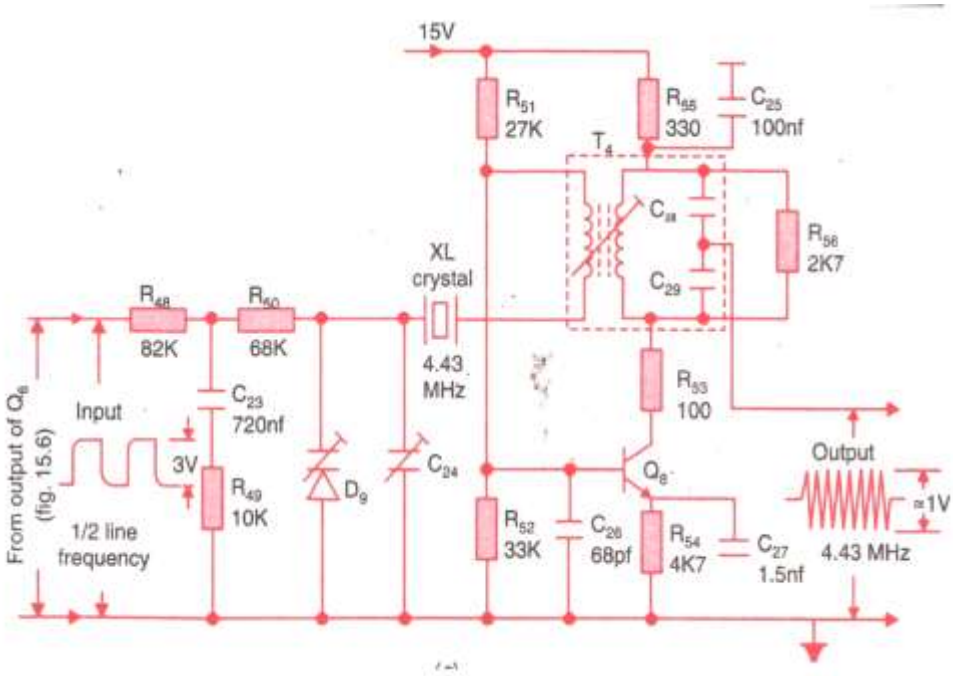



**Figure: Ciruit diagram of reference oscillator**

**Need of reference oscillator in PAL- D decoder:**

- The U and V Chroma signals are separately produced at the transmitting end by what is known as double- balanced suppressed-carrier modulator.
- Thus it is necessary to regenerate the subcarrier in the receiver to affect demodulation of colour-difference signal.
- The reference oscillator circuit that generates a sinusoidal output at 4.43MHz is shown in figure above.
- The frequency is determined by the center-resonant frequency of the crystal (XL) which in this circuit is approximately 4.43MHz.

**e) Compare Plasma and LCD display technology (any 4 points)**

**Ans: (Any 4 Points, 1 Mark Each) (Any other relevant point should also be given marks)**

**Comparison:**

| Parameter | Plasma Display | LCD Display |
|---|---|---|
| **Brightness** | Very poor in direct sunlight without reflective design (battery powered devices); | Some panels are highly reflective, should be used in a dark environment for optimum picture quality |
| **Contrast** | Over 1,000:1 | Over 20,000:1 |
| **Color** | Good on most newer models | Excellent |
| **Ghosting & Smearing** | Display motion blur on models with slow response time, and the elimination technique (strobing backlight) can cause eye-strain | None even during fast motion, advancements in 3D have eliminated phosphor trailing due to the use of fast-switching phosphors |
| **Response Time** | 1–8 ms typical (according to manufacturer data), older units could be as slow as 35 ms | Sub-millisecond |
| **Environmental influences** | Low temperatures can cause slow response, high temperatures can cause poor contrast | High altitude pressure difference may cause poor function or buzzing noises |
| **Aging** | Yes | Yes |
| **Weight** | Light | Heavy, however, less weight gain per size increase |

**Q. 4 A) Attempt any THREE of the following:** **12M**

**i) Explain with suitable diagram how and LCD display works.**

**(Diagram-2 Marks, Explanation -2 Marks)**

**Ans**: **Diagram:**

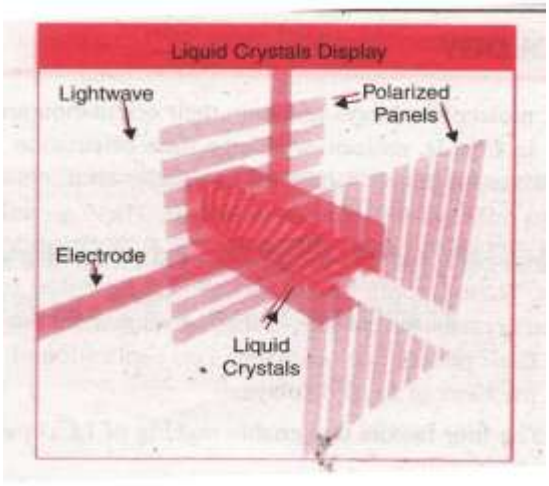



**Figure: LCD display**

**Operation:**

- As any incident light strikes the first glass filter it is polarized. The molecules in each layer of the applied nematic crystals then guide the light they receive to the next layer.
- As the light passes through the liquid crystal layers, its molecules also change the light's plane of vibrations to match their own angle.
- Then light reaches the far side of the liquid crystal substance, it vibrates at the same angle as the final layer molecules. If the final layer is matched up with the second polarized glass filter then the light will pass through.
- If an electric charge is applied to liquid crystal molecules they untwist. On straightening out they change the angle of light passing through them so that it no longer matches the angle of the top polarized filter.
- Consequently, no light can pass through that area of LCD, which makes it darker than the surrounding area.

**ii) State the need of AGC and AFT in colour TV receiver.**

**(Need of AGC- 2 Marks, Need of AFT- 2 Marks)**

**Ans**: **Need of AGC:**

- Automatic Gain Control (AGC) circuit varies the gain of a receiver according to the strength of the signal picked up by antenna.
- Useful signal strength at the receiver input terminals may vary from 50µV to 0.1V or more, depending on the channel being received and distance between transmitter and receiver.
- The AGC bias is a DC voltage proportional to the input signal strength. It is obtained by rectifying the video signal as available after the video detector.
- The AGC bias is used to control the gain of RF and IF stages in the receiver to keep the output at the video detector almost constant despite changes in the input signal to the tuner.

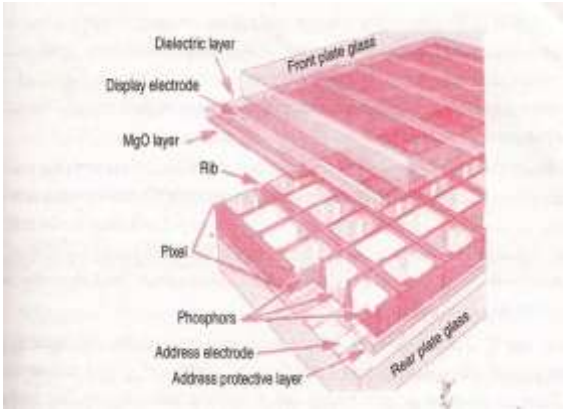
**Need of AFT:**

- The local oscillator frequency in the RF tuner is set to provide exact IF frequencies.
- To improve the stability of oscillator circuit, some drift does occur on account of ambient temperature changes, component ageing, power supply voltage fluctuations and so on.
- For a monochrome receiver a moderate amount of changes in the local oscillator frequency can be tolerated without much effect on the reproduced picture and sound output.
- The fine tuning control is adjusted occasionally to get a sharp picture.

iii) **Explain the working principle of plasma screen**.

**(Diagram-2 Marks, Working Principle of -2 Marks)**

**Ans**: **Diagram:**



**Working Principle:**

- To ionize the gas in a particular cell, the plasma display's computer charges the electrodes that intersect at the cell. The computer does so thousands of times in a small fraction of a second charging each cell in turn.
- When the intersecting electrodes are charged on application of small voltage, an electric current flows through the gas in the cell.
- The current creates a rapid flow of charged particles which simulate the gas atoms to release ultraviolet photons.
- The released ultraviolet photons interact with phosphor material coated on the inside wall of the cell. When ultraviolet photon hits the phosphor atom in a cell, one of its electrons jumps to a higher energy level and the atom heats up.
- When electron falls back to its normal level, it releases energy in the form of visible light photon which illuminates the screen.
- The phosphor in a plasma display give-off colour light when they are excited. Each pixel is made up of three separate sub-pixel cells with different colour (R, G, and B) phosphor.

**iv) Draw the circuit diagram of vertical output amplifier and describe it's working.**

**(Diagram-2 Marks, Working- 2 Marks)**

**Ans**: **Diagram:**

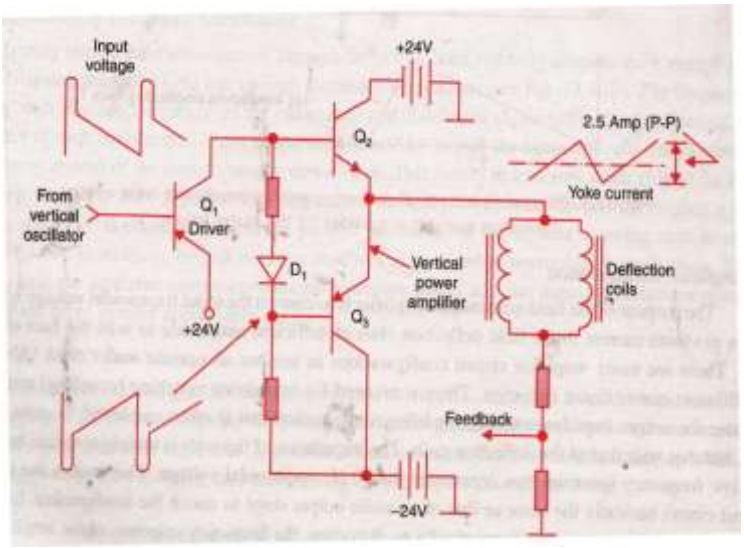



**Figure: Circuit diagram of vertical output amplifier**

**Working:**

- The output transistor Q2 and Q3 operate under class 'B' and are alternately driven in to conduction by a common trapezoidal input signal.
- When Q2 is ON and Q3 is OFF, current flows through the yoke from the positive 24V supply. On the alternate half of the input signal when Q3 is ON and Q2 is OFF, current flows in the opposite direction from the negative 24V supply.
- This amounts to an AC current flow through yoke. Diode D1 is forward biased and voltage drop across it provides suitable bias to Q2 and Q3 thereby preventing any crossover distortion.
- The conduction of diode D1 also ties the bases of Q2 and Q3 allowing signal output from the driver Q1 to feed both of them simultaneously.

**B) Attempt any ONE of the following:** **06M**

**i) Draw schematic diagram of VIF IC and state function of each block.**

**(Diagram- 3 Marks, Explanation -3 Marks)**

Ans: **Block Diagram:**

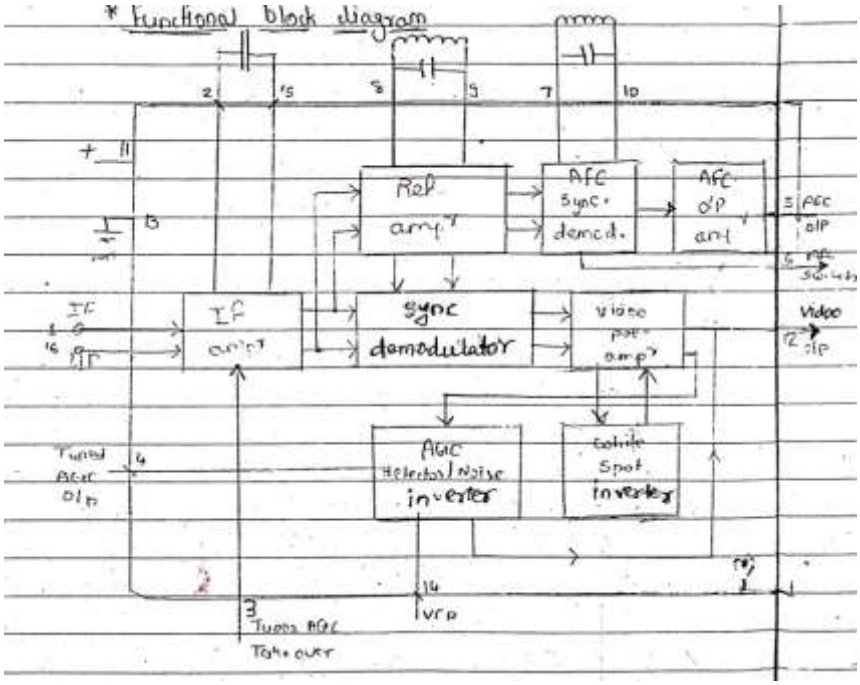



**Figure: Schematic diagram of VIF IC**

**Explanation:**

- **Gain Control of IF amplifier:** The gain control of IF amplifier is a cascade of 3 stage wide band amplifier. It amplifies IF output received from the SAW filter to a suitable level. The maximum overall gain of the IF amplifier is kept about 60dB to obtain sensitivity of 100mV at 38.9 MHz. The gain of IF amplifier is controlled by the AGC controlled voltage which is applied to the 3rd stage of IF amplifier.
- **Synchronous Demodulator:** A synchronous demodulator is used for detecting composite video signal. It requires a dual modulated IF signal and a reference signal for detection. It consists of 2 dual differential amplifiers and 2 modulated transistors that work in push pull configuration to detect video signal output.
- **Video Pre- Amplifier:** The video pre-amplifier with noise cancellation circuit is used as a buffer stage for impedance matching and feeding of signal to the succeeding stages. The bandwidth of this amplifier is slightly greater than 5MHz.
- **White spot inverter:** White spots on the screen are caused by excessive current due to over-modulated signal. This circuit faithfully detects the noise signal and plans them to safe amplitude.
- **AGC detector & noise inverter:** AGC circuit generates control voltage to limit the video signal amplitude during both positive and negative noise spikes and when the voltage of the signal is low. The noise inverter circuit cancels the noise signal by adding inverted noise pulses detected by white spot inverter.
-

**ii) Draw circuit diagram of luminance signal processing and describe it's working.**

**(Circuit diagram-3 Marks, Working- 3 Marks)**

Ans: **Circuit Diagram:**

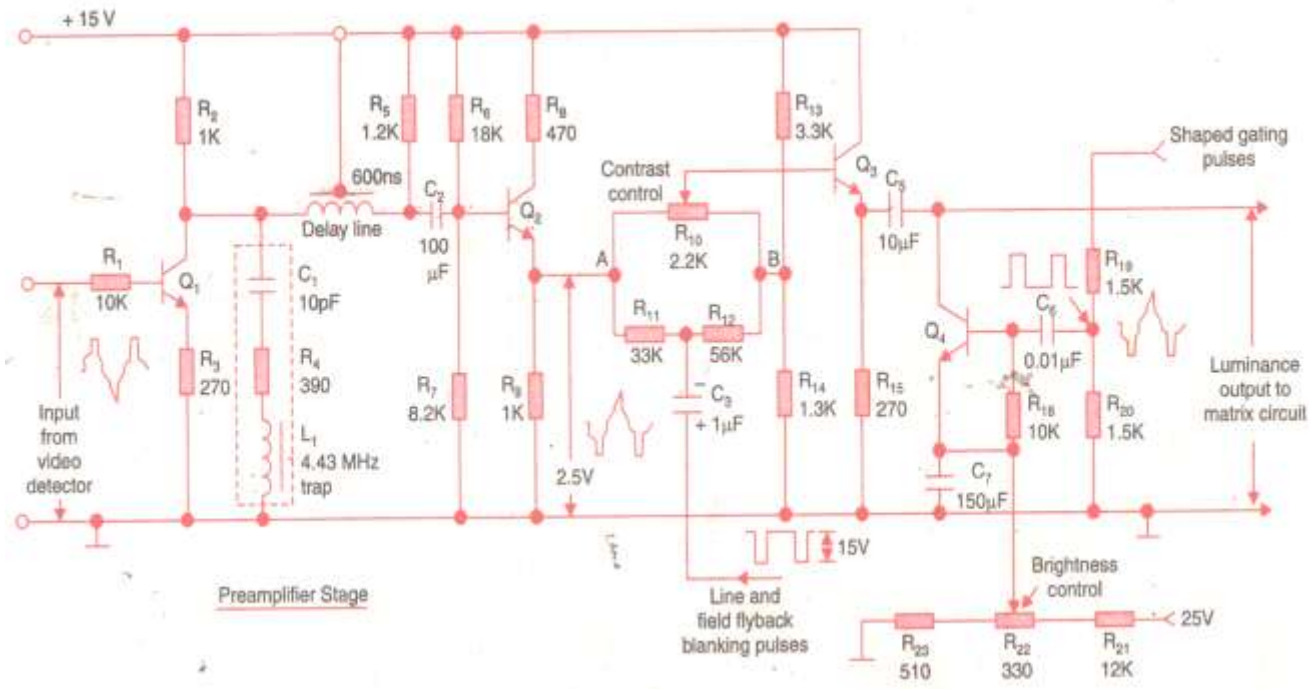



**Figure: Circuit diagram of luminance signal processing**

**Working:**

- Transistor Q1 constitutes the preamplifier and it designated to provide impedance match to the delay line on its output side and video detector on the input side.
- The amplified and inverted signal that becomes available at the collector of Q1 is fed via delay line at the base of Q2. The in between series trap formed by C1, R4 and L1 is to bypass Chroma signal.
- The contrast control elements R10, R11 and R12 form a part of a bridge circuit where potentials at point A and B are at the same level. The dc voltage at point A is nearly 3V and therefore values of R13 and R14 are so chosen that voltage at point B is also equal to 3 volts.
- The clamping voltages are applied directly to the emitter of Q4 which is connected to operate as an electronic switch. During picture content periods of the Y signal, the transistor is held in non-conducting state by resistor R18 connected between base and emitter.
- During back porch intervals of the video signal, Q4 is momentarily forced into full conduction by the arrival of positive going line frequency rate pulses applied to its base via capacitor C6.
- The amplified video (luminance) signal obtained at the output of luminance channel is either passed on to a suitable stage in the Chroma IC or to the discrete R,G &B output stage.

**Q5. Attempt any two of the following: 16M**

**a) Draw block diagram of colour TV receiver. State the function of each block.**

**Ans: (Diagram 04 M; explanation 04 M)**

**IF amplifier & Saw filter:-**

The saw filter is used for $V_{SB}$ correction. It is necessary to provide IF amplifier to compensate for the large uniform attenuation of the signal that occurs in the saw filter.

**AGC stage:-**

AGC circuit varies the gain of the receiver according to the strength of the signal picked up by the antenna. The AGC bias is used control the gain of RF & IF stage in the receiver to keep the output at the video detector almost constant despite changes in the input signal to the tuner.

**Video Detector:-**

Modulated IF signals after due to amplification in the IF section are fed to the video detector. The detector is designed to recover composite video signal and to transform the sound signal to another lower carrier frequency. This is done by rectifying the input signal & filtering out unwanted frequency components. A diode is used which is suitable polarized to rectify either positive or negative peaks of the inputs.

**Luminance Section:-**

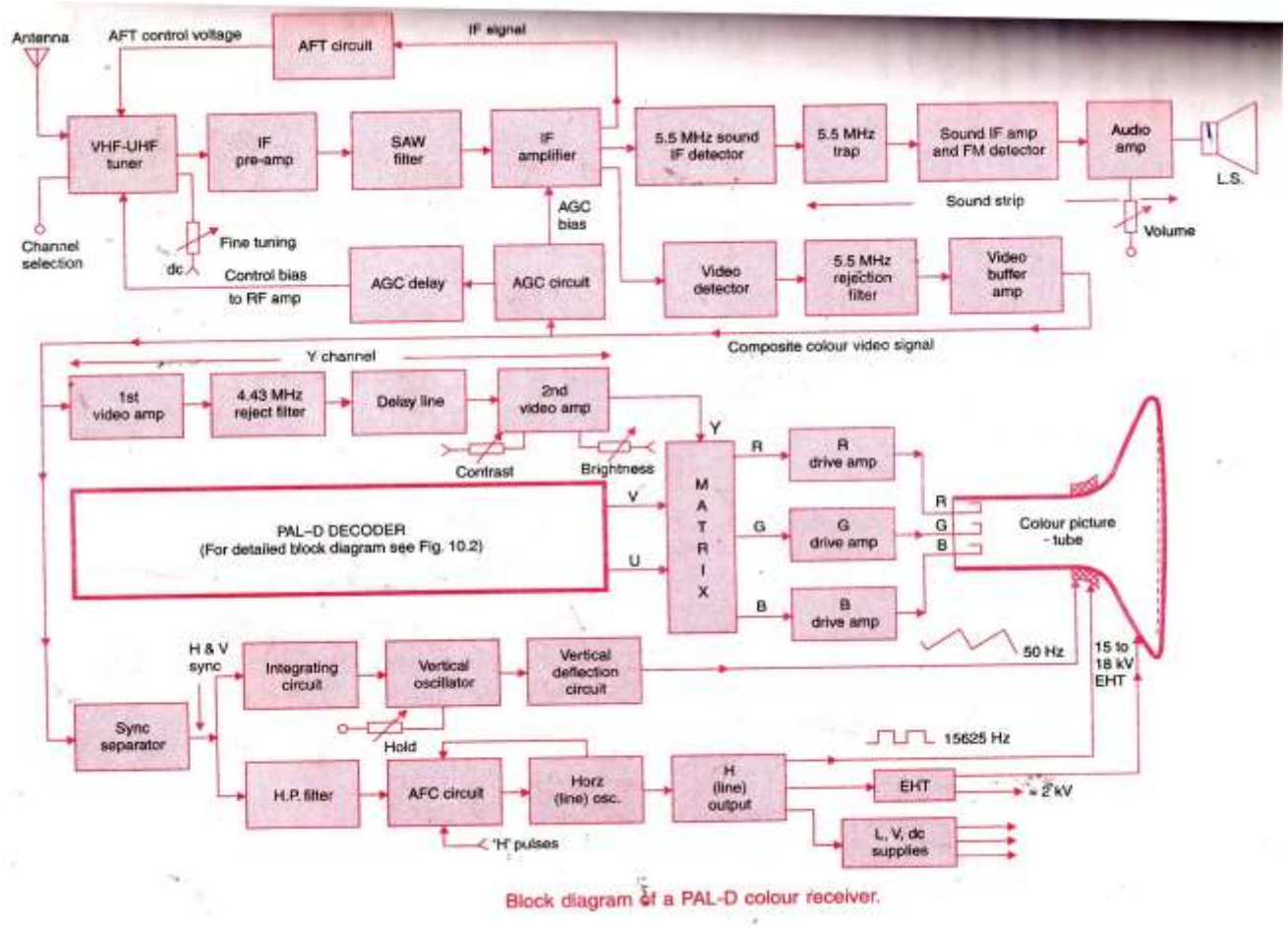
This section blocks the chroma signal and one (1MHz) side bands. Here delay line is used, because luma signal processing requires less stages than chroma signal processing and hence delay of 0.6μs is provided to luma signal and hence they are needed at the same time in RGB matrix and hence synchronization is maintained. The contrast and brightness control is also provided in this stage.

**PAL – D Decoder:-**

The PAL – D decoder performs the following function:

- Chroma signal separation and amplification.

- Separation of U and V signal phasor by employing delay line technique.




Block diagram of a PAL-D colour receiver.

- Demodulation of U & V phasor to recover colour difference signals
- Generation of suitable sub-carrier for the two demodulators.
- To develop ident signal for V channel switching & biased voltage for colour killer circuit.

**RGB Matrix, RGB driver stage & picture tube:-**

The RGB matrix consist of demodulated U & V signals along with Y signal at the output, we get separate R,G,B signal.

RGB driver stage amplify the RGB signal to sufficient level to drive it to picture tube.

Picture tube consist of three separate cathodes for primary colours R,G,& B signals. It also consist of three different control signals.

**b) Draw schematic diagram of IC 7609 and state the function of each block.**

Ans:- **(Diagram 04 M; explanation 04 M)**

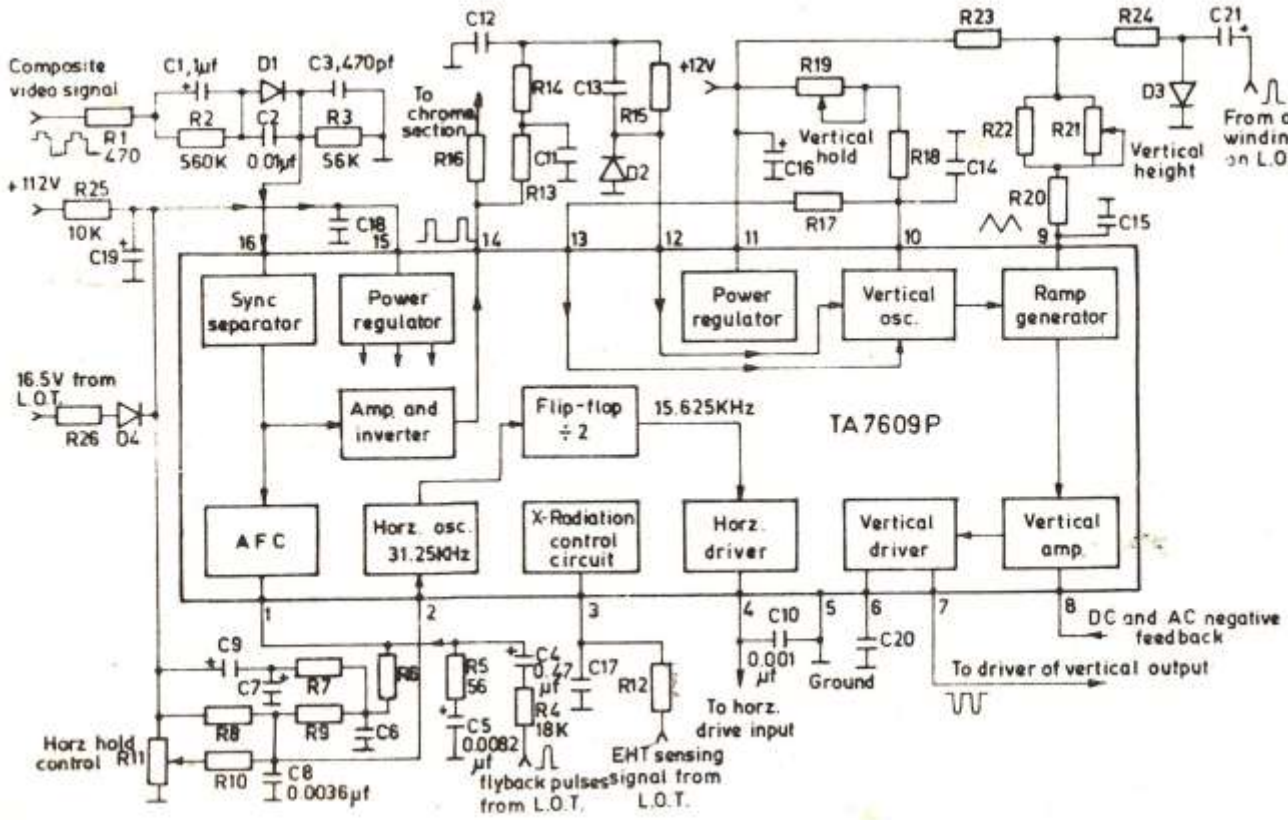



**Figure: Block schematic of IC 7609**

**[Note: marks should be credited even if key functions of blocks are stated]**

Different sections of TA7609P function in the following manner:

**SYNC Separator:-**

A transistor with double time-constant leak-bias input circuit is used as sync separator to prevent blocking g strong noise pulses. As shown in the figure, negative going composite colour video signal obtained either from a pin of the vision IF IC.

The line sync pulses being of much shorter duration (high frequency) pass through the small value capacitor $\mathbf{C_2}$ to cause base current and hence produce sync output. The charge that builds across $C_2$ quickly discharges through $D_1$ when each sync pulse passes away. The double time-constant circuit also prevents any noise pulses from holding the device at cut-off for longer periods. The transistor operates with a small Vcc supply and large load resistance so that it bottoms quickly to provide clean sync pulses. The sync

output (see Fig. 13.1) is fed directly to the AFC circuit and after amplification to the vertical and chroma sections of the receiver from pin 14.

**AFC Circuit:-**

A single ended discriminator similar to the AFC detector is built in the IC to prevent any phase or frequency deviation of the line oscillator. The two inputs to this circuit are the sync pulses and line flyback pulses. The flyback pulses are shaped into sawtooth shape by the integrating capacitor $\mathbf{C_5}$ before feeding from pin 1 to the AFC circuit. On any frequency deviation, control voltage from the AFC circuit is in the form of pulses at the oscillator rate. It is smoothened by the external filter networks $R_6$-$C_6$ (pin 1) and $R_7$-$C_7$ before applying through $\mathbf{R_9}$ to the line oscillator at pin 2.

**Horizontal Oscillator:-**

The line oscillator circuit is around an operational amplifier where the feedback network is for sustained oscillation and input circuitry to determine frequency. The capacitor $\mathbf{C_8}$ at pin 2 forms part of this circuit. The frequency is set at the correct value by varying dc voltage to the oscillator circuit (pin 2) from the 12V dc rail through $\mathbf{R_8}$, $\mathbf{R_{10}}$ and $R_{11}$. Thus potentiometer $R_{11}$ acts as 'hold' control for the line deflection frequency.

The oscillator is operated at 31.25 KHz (twice of 15.625 KHz) and then a flip-flop circuit divides it by 2 to obtain the desired 16525 Hz rate. The reason for fixing the oscillator frequency at 31250 Hz instead of 15625 Hz is twofold. Firstly, the divide circuit indirectly prevents any variations in the width Of output pulses thus minimizing dispersion effects in the line output circuit. Secondly, the magnetic on induction effect from line to frame oscillator in the ICs is identical during both fields of a frame thereby ensuring good interlaced scanning than when alternate fields are affected differently with oscillator operating at 15625 Hz.

**X- Ray Radiation Control:-**

X-ray radiation prevention circuit is designed to disable the line oscillator should the EHT voltage a exceed limit that can cause radiation from the screen face. The signal to sense this is obtained from a section of the line output transformer and fed to the control circuit at pin 3 through $R_{12}$ and $C_{17}$.

**Horizontal Driver:-**

The .driver that is fed from the flip-flop output is a single-ended differential amplifier which besides wave shaping amplifies line drive pulses. The capacitor $C_{10}$ (0.00111F) connected at pin 4 is for wave shaping as necessary. The output from the driver amplifier is fed to the line output stage from pin 4 as shown in the figure.

**Vertical Oscillator:-**

Vertical oscillator is a multivibrator circuit triggered by vertical sync pulses. These pulses on obtaining from pin 14 are passed through a two stage integrating network comprising of $R_{13}$-$C_{ii}$ and $R_{14}$-$C_{12}$. The output is then wave shaped by $R_{15}$-$C_{13}$ and diode $D_2$ before feeding to the oscillator control circuit. The differential amplifier of the multivibrator circuit performs current switching function and generates a positive going

output of constant amplitude at a frequency of 50 Hz. A negative feedback through $R_{17}$ connected between pins 10 and 13 is to stabilized the oscillator operation. The time-constant circuit formed by $C_{14}$, $R_{18}$, $R_{19}$ and connected at pin 10 from the 12V source determines frequency of oscillations. Thus potentiometer $R_{19}$ acts as the vertical 'hold' control.

**Ramp Generator:-**

A ramped shaped drive is necessary for the vertical deflection amplifier. It is generated by charging $C_{15}$ through a transistor driven by oscillator's output pulses. The charge and discharge i.e., retrace and traced periods are controlled by the external R-C network connected at pin 9. With a positive pulse of constant width at the base of ramp generating transistor, capacitor $C_{15}$ charges quickly to provide the retrace period. As the input pulse drops/ the transistor turns-off enabling the capacitor to discharge through resistive network formed by $R_{20}$, $R_{21}$, $R_{22}$, $i_{23}$ and input resistance of dc supply. The time-constant of this discharge path is large enough to provide a near linear trace period. The amplitude of ramp thus generated can be controlled by changing magnitude of dc voltage applied at pin9. This as shown in the figure, is done by varying $R_{21}$.

It is necessary to maintain width to height ratio of the raster constant at 4:3. Any change in dc voltage to the line output stage will affect width of the reproduced picture. It then become necessary to cause corresponding change in height of the picture to maintain the aspect ratio at 4:3. This is obtained by alternating height of the ramp in an interesting way. Any deviation in the amplitude of line output pulses is sampled from a section of the winding on the line output transformer. These positive going pulses are rectified by diode D3 to produce a proportionate dc voltage across C21. The negative end of this voltage is connected to R21via R24 at the point where de supply is connected to it. Any change in the magnitude of negative voltage caused by line pulse amplitude variations will affect net dc voltage applied to the ramp capacitor.

**Vertical Amplifier:-**

This is a single ended differential amplifier designed to amplify ramp output to a level necessary to drive the vertical output stage. Negative feedback, both dc and ac is applied to it from different points in the output stage amplifier to obtain correct centering and linear deflection in the vertical direction.

**Vertical Driver:-**

It is an emitter follower for current gain and impedance matching between the drive amplifier and vertical output stage. The capacitor C20 at pin 6 is for decoupling purposes in the vertical dreiver section of the IC.

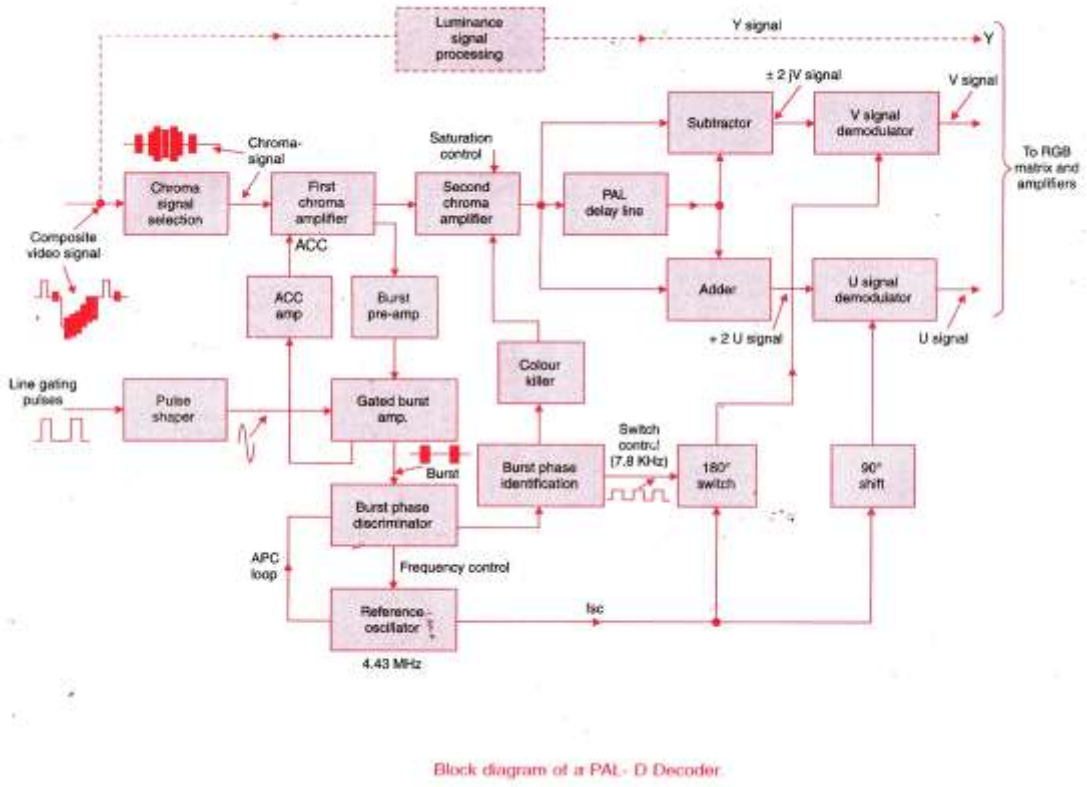
**DC –Supply:-**

As shown in the figure, dc supply to the IC is from two sides. A dc supply at 12V from the L.O.T side feeds at pin 11 to a regulator that feeds vertical section blocks in the integrated circuit. Another dc voltage from L.O.T. at 16.5V is connected to a different dc rail via voltage dropping resistor R26 and diode D4. This is paralleled with a source obtained from ac mains side at 112V and dropped through R25 to obtain

nearly 10V dc on the dc rail. This common dc rail is connected through pin 15 to another voltage regulator for supplying dc voltages to various line oscillator blocks in the IC. This improves efficiency of the line output stage and decreases power drain from ac mains.

**c) Draw block diagram of PAL - D decoder and state the function of each block.**

Ans: **(Diagram 04 M; explanation 04 M)**




Block diagram of a PAL- D Decoder

**[Note: marks should be credited even if key functions of blocks are stated]**

The PAL – D decoder is used to regenerate the original signal red, green and blue colour & fed to the picture tube. The final inputs are applied to R,G,& B amplifier along with the luminance signal.

The chroma signal & colour burst are separated from the incoming composite colour signal by a band pass circuit whose center frequency is 4.43MHz. Also the band pass circuit offers very high impedance at 5.5MHz to prevent breakthrough of the inter-carrier sound signal to the colour decoder. The separated chroma & burst signal are fed to the first chroma amplifier through an emitter followed that provides necessary isolation to the preceding tuned circuits.

The chroma & burst signals are amplifies by the first chroma amplifier which is gain controlled with the voltage developed by the automatic chroma controlled (ACC) amplifier. The amplified input goes to both the second chroma amplifier & burst pre-amplifier. Also the second chroma amplifier incorporates colour saturation control circuit & the output of second amplifier stage is fed into it. The output of second amplifier stage is fed simultaneously to delay line and addition & subtraction circuit. This network generates U & V signal which are given to RGB matrix and amplifier circuits.

**Q6) Attempt any four of the following: 16M**

**a) Draw block diagram of Schematic of AFT and state the function of each block.**

Ans:- **(Diagram 02 M; explanation 02 M)**

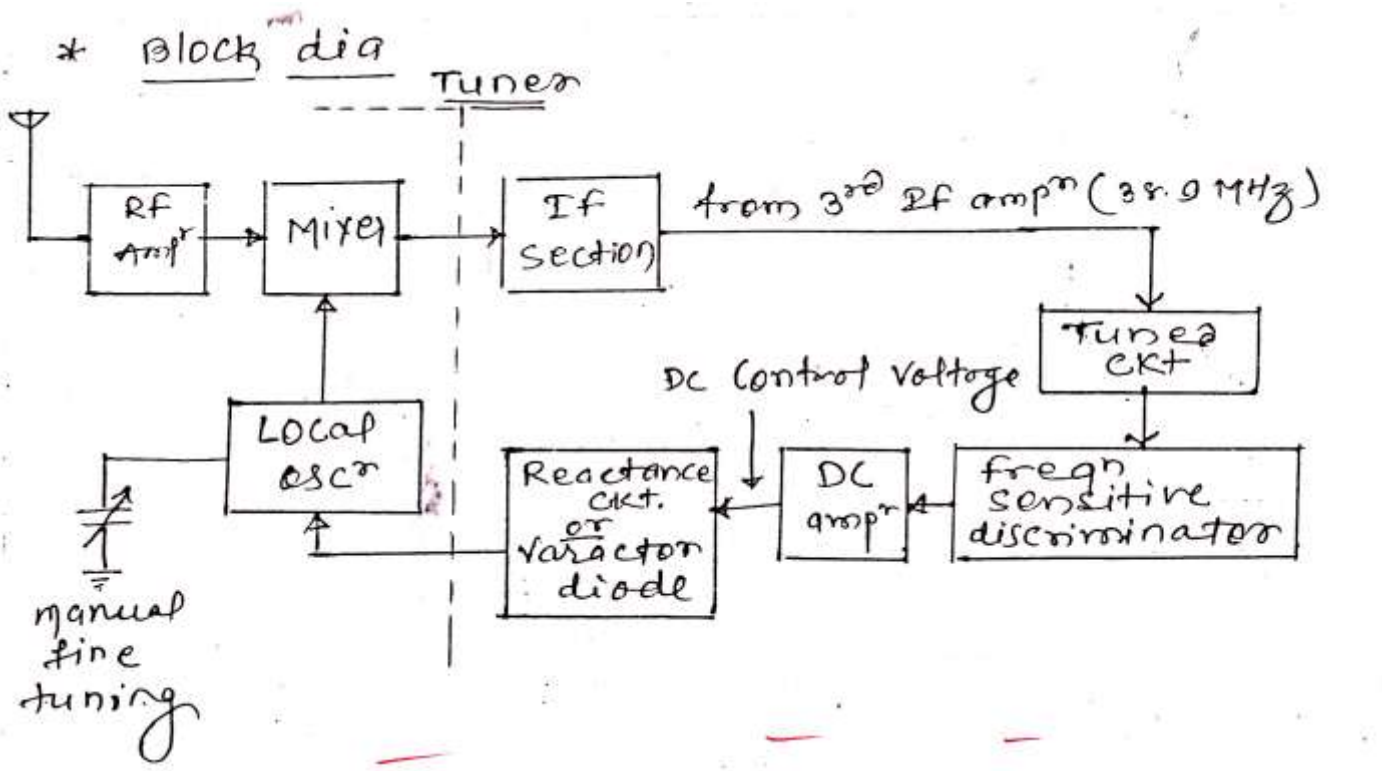



**Figure: Block Diagram of AFT**

**[Note: marks should be credited even if key functions of blocks are stated]**

The AFT circuit is actually automatic frequency control (AFC) on the local oscillator in the tuner. This control aims at obtaining a picture IF frequency of exactly 38.9MHz at the converter output. To achieve this, the IF frequency is obtained from the IF amplifier section is measured by a discriminator that forms part of the AFT control circuit.

- **Frequency sensitive Discriminator :-**

Its output is a DC correction voltage that indicates deviation of IF frequency from its exact value of 38.9MHz. since this frequency depends on the oscillator input to the mixer, the AFT voltage indicates error in the local oscillator frequency.

The AFT control voltage is zero at balance i.e. when the IF frequency is exactly 38.9MHz for frequency deviations on either side of 38.9MHz, the net dc correcting voltage is either positive or negative depending on whether the frequency is above or below the correct value.

- **Reactance circuit or Varactor diode:**

The DC control voltage thus developed is applied to a reactance circuit or to a varactor diode that forms part of the local oscillator tank circuit.

The junction capacitance of the varactor diode varies with the applied dc control voltage and thus changes resonant frequency of the oscillator tuned circuit to shift the frequency to its correct value.

**b) List any eight major controls available in plasma TV. State the function of any two controls**.

**Ans**:- **Controls available in plasma TV (ANY EIGHT)** **0.25 eachx8=2 marks**

i. Change viewing modes
ii. Use picture-in-picture (PIP) mode
iii. Use picture-on-picture (POP) mode
iv. Change plasma TV tuner settings
v. Set the sleep timer
vi. Adjust sound controls
vii. Use the V-Chip (Parental Guide) controls
viii. Adjust the picture
ix. Change on-screen display (OSD) settings
x. View signal frequency information

**Explanation :- (any two): 01 M each = 02 M**

1. Changing widescreen and normal viewing modes

   Plasma TV has several widescreen and normal viewing modes you can use:
   4:3 viewing mode produces a square image similar to a standard TV.
   Panorama viewing mode stretches only the sides of the image to fill the screen, leaving the center of the image unmodified.
   16:9 viewing mode produces a widescreen image similar to the screen at a movie theater. When you are in 16:9 mode, you can select one of three zoom modes.

2. picture-in-picture (PIP) mode

   When the picture-in-picture (PIP) mode is active, one picture is displayed on the full screen and the other picture is displayed in a small window. The OSD in the upper-right corner of your screen lists the programs displayed on the full screen and in the window.
   When the PIP button on the remote control is pressed once to turn on PIP mode. A small window appears in one corner of the screen. The picture on the full screen is the main picture. The picture in the window is the sub-picture.

3. picture-on-picture (POP) mode

   When the picture-on-picture (POP) mode is active, the screen is divided into two equal parts with a picture displayed on each side. The OSD in the upper-right corner of your screen lists the video input source displayed on each side of the screen.
   When press the PIP button on the remote control twice to turn on POP mode. The screen is split into two pictures. The picture on the left side of your screen is the main picture. The picture on the right side of the screen is the sub-picture.

4. Changing TV tuner settings
   One can set the desired tuner setting on plasma TV by using tuner control available on remote .
5. Setting up a favorite channel
   One can change the favorite channel settings using the remote control or the OSD.
6. Locking channels
   If one do not want a channel to be accessible, he can set the channel lock for that channel. When anyone tune to a locked channel, they are prompted to enter your password.

**c) Explain with diagram working of frequency synthesizer tuning.**

Ans:- **(Diagram 02 M; explanation 02 M)**

**Explanation:**

The reference oscillator is crystal and its frequency is reduced to 1KHz by divider circuits. The aim being to reduce the frequency to a range that can be proceed and counted by standard logics circuit. The output of prescaler feeds into a programmable divider, the divide ratio of which is determined by microcomputer. The output of programmable divider is compared with reference frequency by phase comparator. The inputs to the comparators are of same frequency, the dc error voltage developed by PLL filter is zero and no correction is applied.

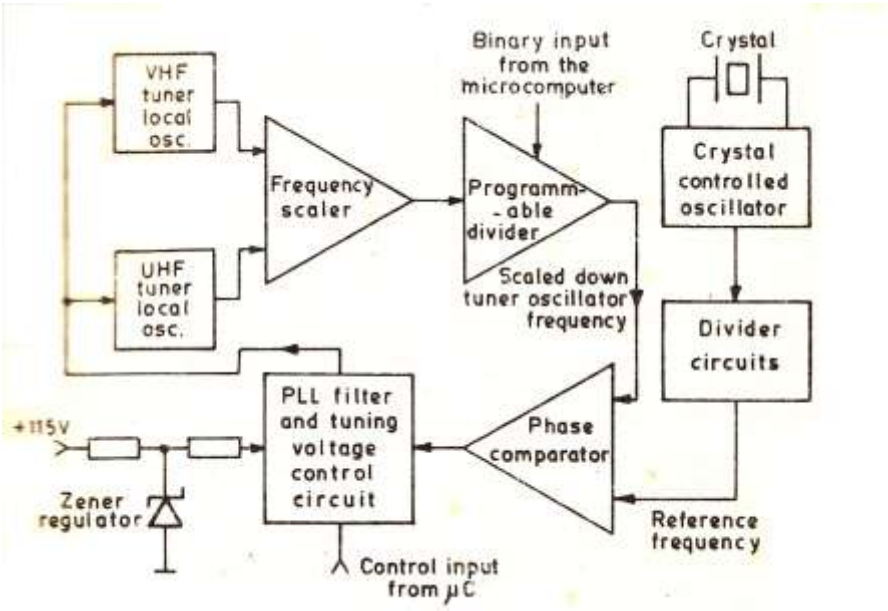



**Figure: Diagram of frequency synthesizer**

If there is mismatch in the input of comparator the correct voltages are generated by PLL filter i.e, the comparator senses the difference and develops appropriate error voltage which gets added to the applied tuning voltage with proper polarity that the oscillator is forced to return to the correct frequency. The PLL circuit continuously monitors the local oscillator frequency and apply necessary corrections.

**d) What is 3D TV technology? Why it is necessary to use special glasses for watching 3D programmers**.

Ans:- **(3D technology 02M; glasses used reason 02 M)**

**Explanation:**

The 3D system relies on a visual process called STEREOPSIS which enables 3D perception. This comes out of the fact that the eyes of an adult human lie about 2.5inches (≈6.5cm) apart which lets each eye see objects from slightly different angles. The combined effect of this on the viewer's mind is that of a three dimensional picture. This ability of our eyes is used in 3D TVs by showing the same object from difference angles on the screen to cause the same the same 3D perception.

Everyone sitting around 3D TV must wear special glasses to see the 3D effect. Without glasses the image on the TV screen will appear doubled, distorted and for most practical purposes unwatchable. Currently there is no technology that enables watching 2D and 3D content simultaneously without glasses.

**Necessary of glasses:-**

The technique used in 3D TV receiver for display of pictures on screen were based on the use of two video signals in different ways to create the illusion of 3D pictures when viewed with special glasses. In 3D the phosphor strips of green colour of picture tube are excited by G video signal originated at one of the two cameras. Similarly all red phosphor strips are excited by R video signal generated by another camera and blue phosphor strips are not excited at all. Therefore special filter glasses are needed to be worn while watching 3D picture on TV screen.

**e) Draw construction of chroma delay line and describe its working.**

Ans:- **( 2 marks—Diagram; 2 marks explanation)**

**Diagram:**

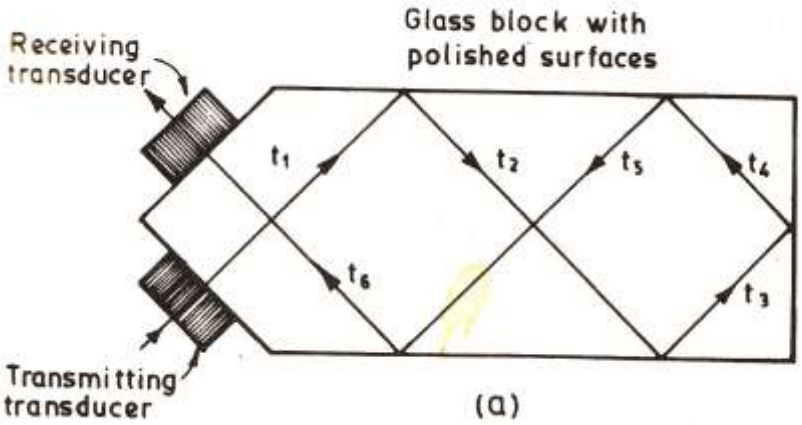



**Figure: Construction of chroma**

**Working:-**

It consists of a block of special glass (Isopaustic) fitted with two ultrasonic transducers. One transducer function to convert electrical signal into an ultrasonic signal whose mean frequency & amplitude variations are identical to those of the electrical signal while the other converts that the ultrasonic signal into electrical form at the same frequency.

The electrical signal from the chroma amplifier with a mean frequency of 4.43MHz is coupled into the transmitting transducers where it is converted into an equivalent ultrasonic signal having the same mean frequency & pattern of amplitude variations. The signal travels through the glass block in a multiple path due to reaction from the polished surface before it reaches the receiving transducer. In the figure it is converted back into the original electrical form but delayed in time with respect to the signal at the input of transmitting transducer.

The delay of signal is caused by low velocity of the ultrasonic signal as it passes through glass of the delay line. This is typically 3mm per μs as compared to the hundreds of thousands of mm per μs transferred by an electrical signal passing along a length of wire.