WINTER – 14 EXAMINATION

Model Answer

Subject Code: **17445**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.

2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.

3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).

4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.

5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.

6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.

7) For programming language papers, credit may be given to any other program based on equivalent concept.

1. a) Attempt any SIX of the following: **12**

i. State ideal and typical values of
1) Input offset voltage **(1M)**
2) CMRR **(1M)**

Ans i.

Sr. No		Ideal	Typical
1	Input offset voltage	0	6mV
2	CMRR	∞	90dB

ii. Draw circuit diagram of subtractor using op amp

Ans ii. **Correct circuit diagram- 2M**

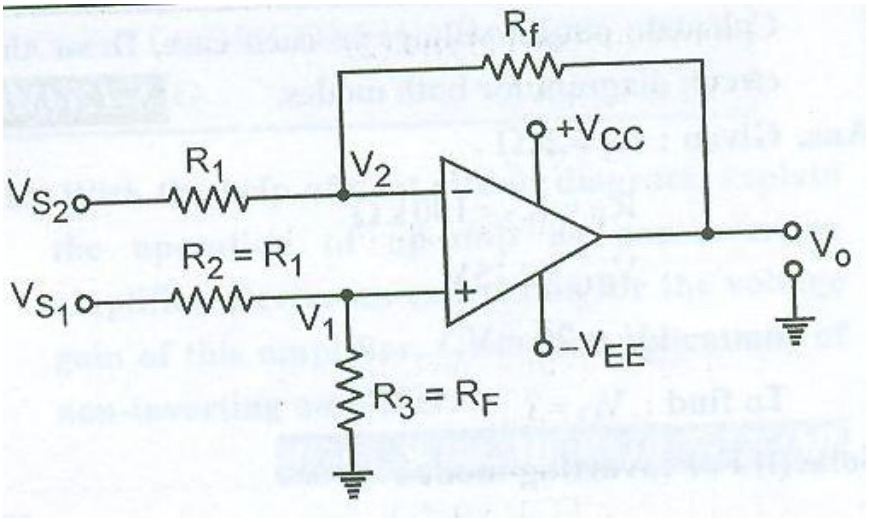


Fig: Subtractor using op- amp

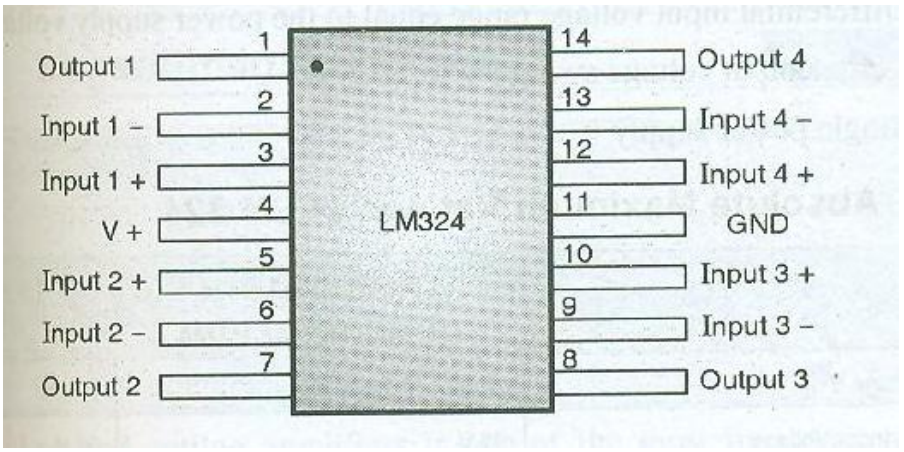
iii. State the need of signal conditioning and signal processing.

Ans iii. **Any Relevant Correct Explanation – 2 M**

- In an instrumentation system, a transducer is used for sensing various parameters. The output of transducer is an electrical signal proportional to the physical quantity sensed such as pressure, temperature etc.
- However the transducer output cannot be used directly as an input to the rest of the instrumentation system.
- In many applications, the signal needs to be conditioned and processed. The signal conditioning can be of different types such as rectification, clipping, clamping etc. Sometimes the input signal needs to undergo certain processing such as integration, differentiation, amplification etc.

iv. Draw pin diagram of IC LM 324

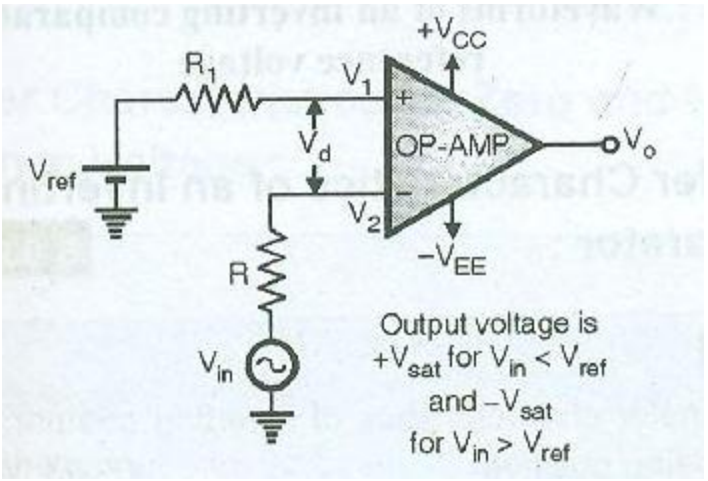
Ans iv. **Correct pin diagram: 2M**



Pin diagram of IC LM 324

v. Draw circuit diagram of inverting comparator.

Ans v. **Correct circuit diagram: 2M**



Inverting comparator

vi. Define

1. Cut off frequency **(1M)**
2. Roll off rate with reference to filter **(1M)**

Ans vi.

Cut off frequency: It is the frequency at which signal strength drops by 3 db (i.e. Signal power becomes half)

Roll off rate with reference to filter: The gain falls off rapidly in the stop band. The rate at which it falls off is called as the Roll off rate.

vii. State four merits of active filter over passive filter.

Ans vii. Any four correct points- **2M**

1. Flexibility in gain and frequency adjustment.
2. No loading problem
3. Low cost
4. No insertion loss
5. Passband gain
6. Interstage isolation and control of impedance
7. Small component size
8. Use of inductors can be avoided

viii. State functions of the following pins of IC 555.

1. Pin no 2 trigger i/p **(1M)**

2. Pin no 6 threshold input **(1M)**

Ans viii.

Pin 2 trigger: The output of the timer depends on the amplitude of the external trigger pulse applied to this pin.

Pin 6 Threshold: This is non- inverting terminal of comparator C_1 which monitors the voltage across the external capacitor. When the voltage at this pin is greater than or equal to 2/3 V_{CC}, the output of comparator C_1 goes high which in turn switches the output of the timer low.

b. Attempt any TWO of the following **8**

i. Draw block diagram of op amp and describe the function of input stage and DC level shifting stage.

Ans i. **Block Diagram: 2M**

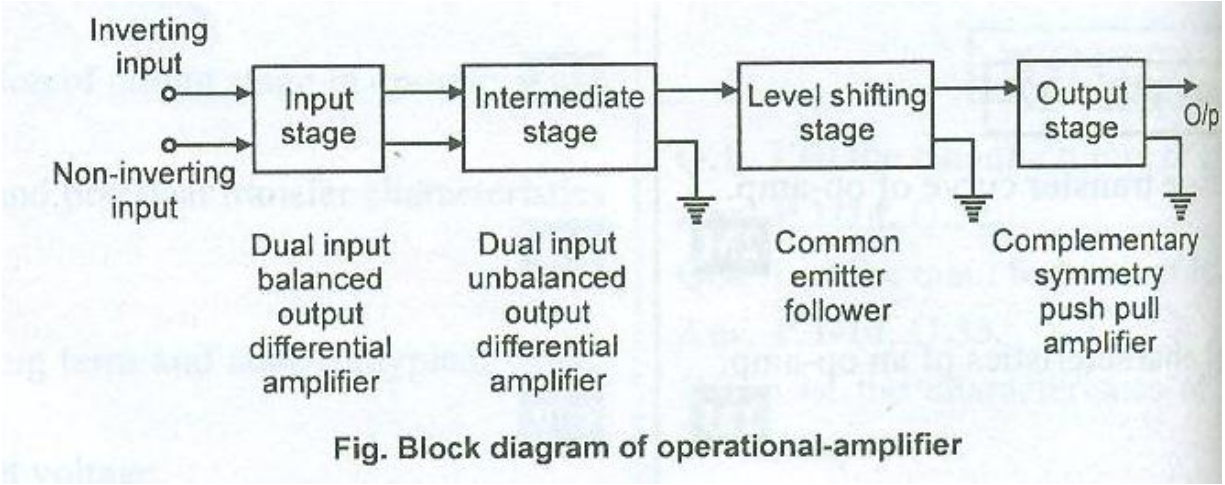


Fig. Block diagram of operational-amplifier

Input stage: 1M

In this stage dual input balanced output differential amplifier is used. Due to this circuit the voltage gain and input resistance of the op amp increases to a high value.

Level shifting stage: 1M

In this stage common emitter follower circuit is used. If, the output of intermediate stage is shifted above or below the DC level, the level shifter stage brings back the signal to its original position.

ii) Define the following parameters of OP amp.

1. Input bias current **(1M)**
2. Input offset current **(1M)**
3. Slew rate **(1M)**
4. CMRR **(1M)**

Ans ii.

- **Input bias current:** It is defined as the average of the two currents flowing through inverting and non-inverting terminals of op amp
- **Input offset current:** It is algebraic difference between the two currents flowing at the input terminals of op amp [Ideal value =0, practical value for 741= 20nA]
- **Slew rate:** It is defined as the maximum rate of change of output voltage per unit time.
  S.R.= $\Delta V_o / \Delta t$ at max ; Unit = V/μs
- **CMRR:** It is defined as the ratio of differential gain to the common mode gain. It is the ability of an amplifier to reject the common mode signal

iii. Draw dual input balanced output differential amplifier and describe the operation of it.

Ans iii. **Diagram: 2M; Operation: 2M**

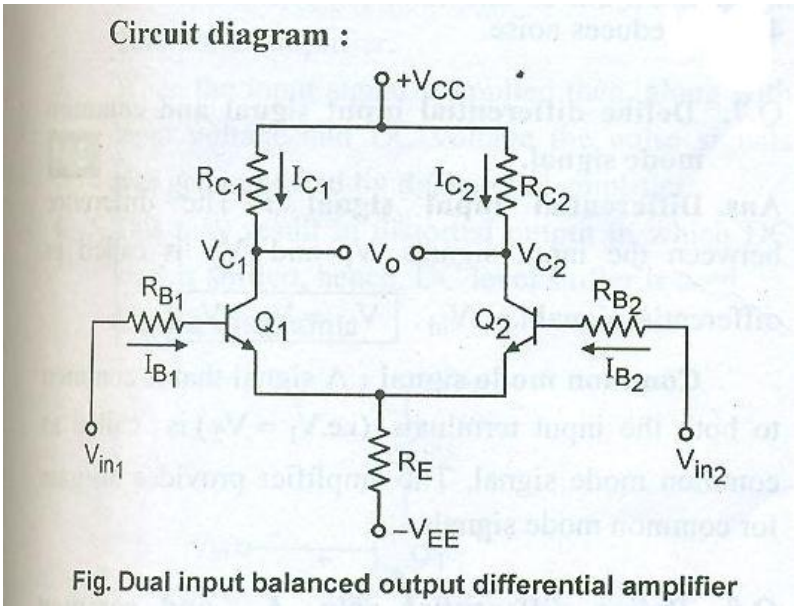


Fig. Dual input balanced output differential amplifier

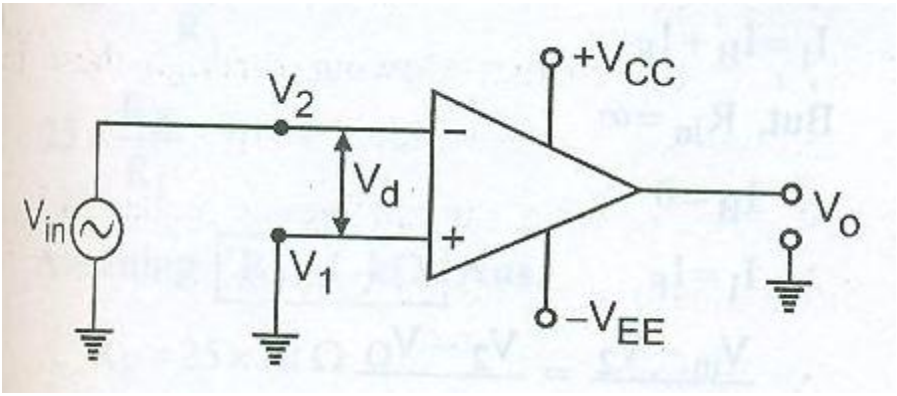
Differential amplifier is a two input transistor amplifier which amplifies the difference between the two input signals V_{in1} and V_{in2}.

- The circuit is in the form of bridge and is excited by $+V_{CC}$ and $-V_{EE}$ and output $V_o = I$ $V_{C1} - V_{C2}$
- When supply voltages are applied then Q_1 and Q_2 turns ON. As the circuit is symmetrical
- Therefore $I_{B1} = I_{B2.}$
  $I_{C1} = I_{C2}$
- By applying KVL at the output, we get,
  $V_{C1} = V_{CC} - I_{C1} R_{C1}$
  $V_{C2} = V_{CC} - I_{C2} R_{C2}$
  As,
  $I_{C1} = I_{C2}$, $R_{C1} = R_{C2,}$ therefore, $V_O = 0$
- As null output is obtained, the bridge is said to be balanced.

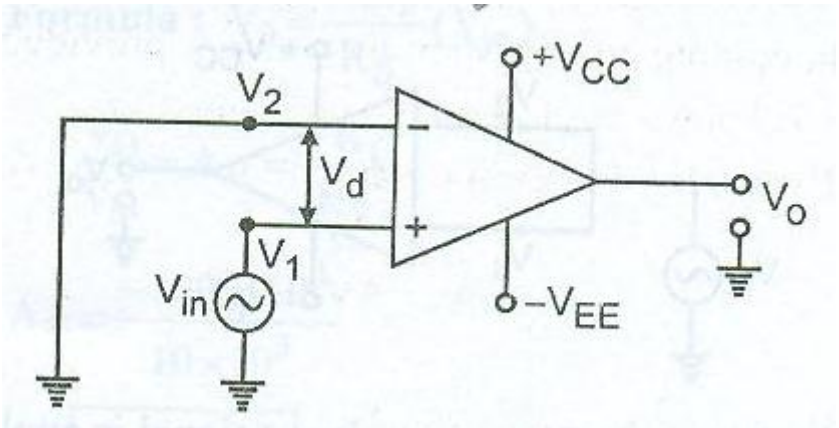
2 Attempt any FOUR of the following: 16

a. Draw open loop inverting and non-inverting amplifiers circuit diagram.

Ans a. Each diagram: 2M



Inverting amplifier



Non inverting amplifier

b. Draw closed loop inverting amplifier using Op amp and derive expression for its gain.

Ans b. Diagram: 2M; Derivation:2M

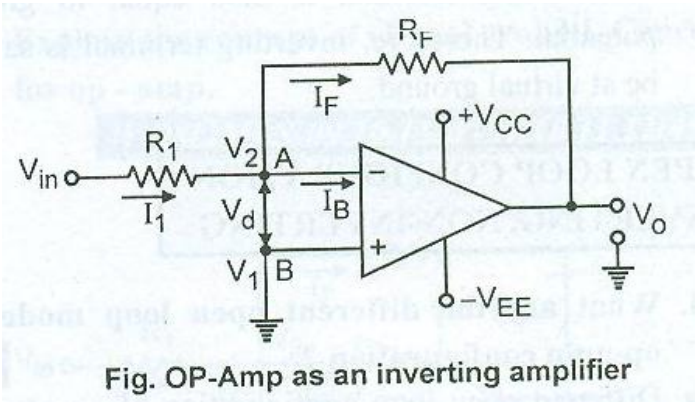


Fig. OP-Amp as an inverting amplifier

1. As input signal V_{in} is applied to inverting input, hence it is called as inverting amplifier and non inverting terminal is grounded.
2. The phase difference between input and output is 180^0
3. A negative feedback is provided from output to inverting terminal through R_F (Feedback resistor)

(A) Derivation:

Apply KCL at node 'A', we get,

$I_1 = I_B + I_f$ — (1)

But, $R_{in} = \infty$

$\therefore I_B = 0$

$\therefore I_1 = I_F$

$\therefore \frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_o}{R_F}$

According to virtual ground condition,

$V_1 = V_2 = 0$

$\therefore \frac{V_{in}}{R_1} = \frac{-V_o}{R_F}$

$\therefore \boxed{V_o = -\left(\frac{R_F}{R_1}\right) V_{in}}$ — (2)

$\therefore \boxed{A_V = \frac{V_o}{V_{in}} = -\frac{R_F}{R_1}}$ — (3)

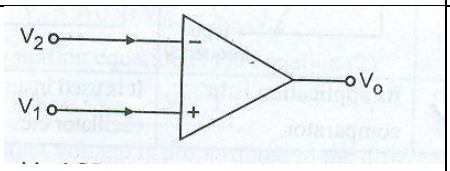
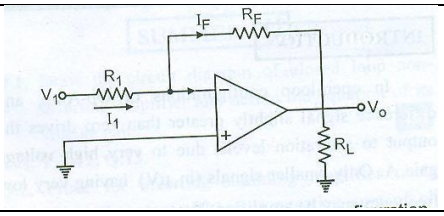
where, A_V = closed loop voltage gain

V_o= output voltage, V_{in}= input voltage, R_F= Feedback resistor, R_1= Input resistor

c. Compare open loop and closed loop configuration of Op amp on following basis.

i. Circuit diagram (1M)
ii. Gain (1M)
iii. Bandwidth (1M)
iv. Application (1M)

Ans c.

Sr. No	Parameters	Open loop	Closed Loop
1	Circuit Diagram		
2	Gain	Voltage gain is very high	Voltage gain is low as compared to open loop.
3	Bandwidth	Bandwidth is low	Bandwidth is high
4	Application	Comparator	It is used in amplifier, oscillator etc.

d. Draw the circuit of basic differentiator and derive the output expression.

Ans d. **Diagram: 2M; Derivation: 2M**

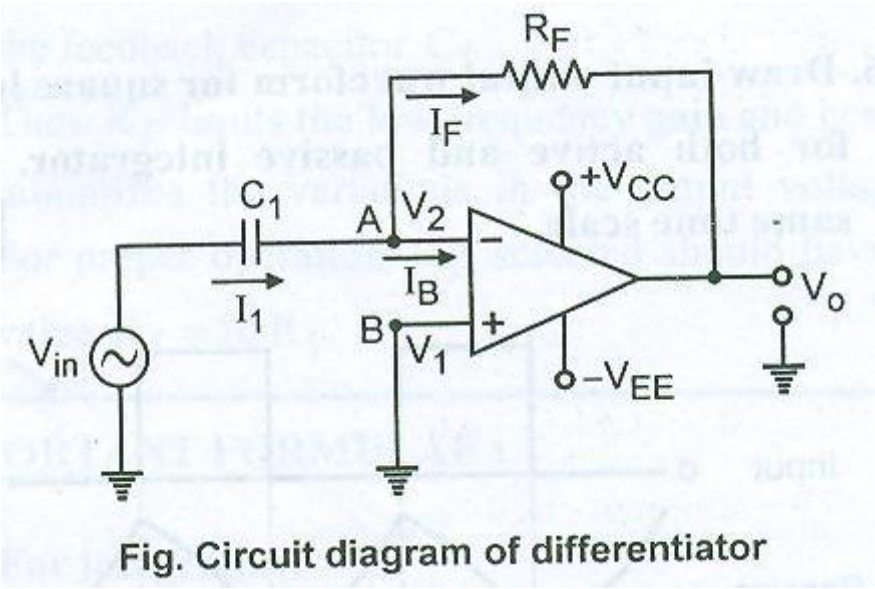


Fig. Circuit diagram of differentiator

1. The op- amp is working in inverting mode.

2. Derivation:

Applying KCL at node 'A'

$I_1 = I_B + I_f$

$\therefore R_{in} = \infty, I_B = 0$

$\therefore I_1 = I_f$

$$C_1 \frac{d}{dt}(V_{in} - V_2) = \frac{V_2 - V_o}{R_F}$$

Due to virtual ground condition

$V_1 = V_2 = 0$

$$\therefore C_1 \frac{d}{dt} V_{in} = -\frac{V_o}{R_F}$$

$$\therefore V_o = -R_F C_1 \frac{d}{dt} V_{in}$$

Negative sign indicates that it is an inverting amplifier and $V_o \propto \frac{d}{dt} V_{in}$.

e. Design the circuit to get the output expression
$V_o = -(2V_1 + V_2 + 5V_3)$

Ans e. **Calculation: 2M; Circuit Design diagram: 2M**

Output expression is

$V_o = -(2V_1 + V_2 + 5V_3) = -2V_1 + V_2 + 5V_3$ ----------(1)

Output expression for inverting amplifier adder is

$$V_o = -\left(\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right)$$

$$= -\frac{R_f}{R_1} V_1 - \frac{R_f}{R_2} V_2 - \frac{R_f}{R_3} V_3 \quad \text{— (2).}$$

Compare equation (1) & (2) we get,

- $(R_F/R_1) \times V_1 = 2V_1$

$R_F = 2R_1$

Let $R_F = 10k\Omega$

Therefore, $R_1 = 5k\Omega$

- $(R_F/R_2)x\ V_2 = V_2$

  $R_F = R_2$

  Let $R_F = 10k\Omega$

  Therefore, R2= 10kΩ

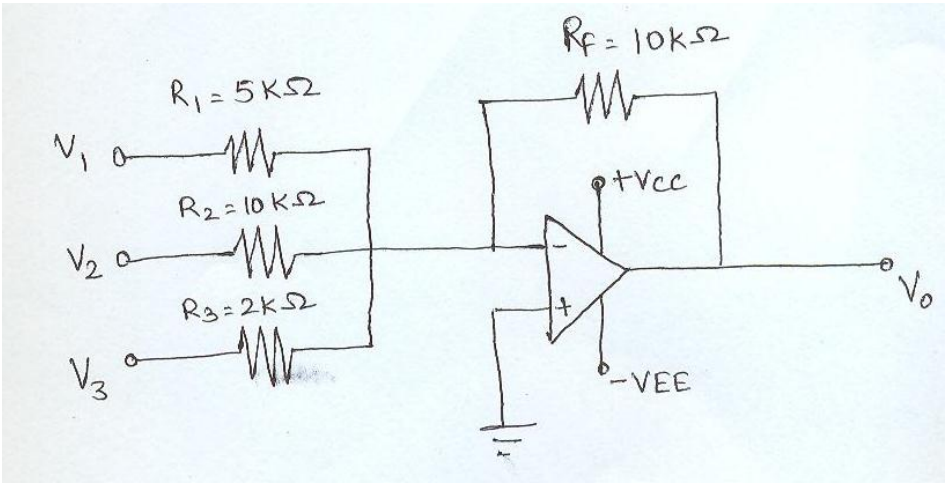
-

  $(R_F/R_3)x\ V_3 = 5V_3$

  $R_F = 5R_3$

  Let $R_F = 10k\Omega$

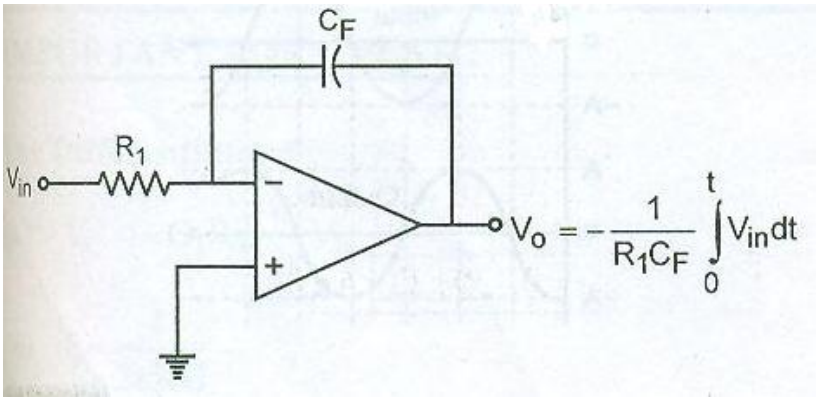
  Therefore, $R_3 = 2k\Omega$



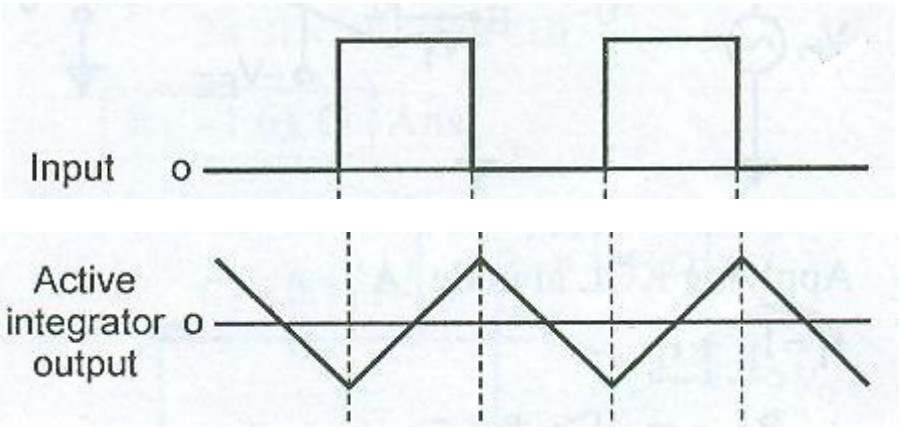
f. Suggest Op amp based circuit to convert square wave to triangular wave. Draw the circuit diagram with input and output waveforms.

Ans f. **Correct answer: 1M; Circuit diagram:$1^{1/2}$ M; Waveform: $1^{1/2}$ M**

Integrator based circuit can be used to convert square wave to triangular wave.



Circuit Diagram



3. Attempt any FOUR of the following: **16**

a. Draw the circuit of V to I converter with floating load and describe its operation.

Ans a. **Diagram: 2M; Operation: 2M**

- Figure shows the circuit of voltage to current (V to I) converter with floating load. This is also called as transconductance amplifier.
- The circuit converts the voltage applied to the output current. Figure shows the V to I converter in which load resistor R_L is floating i.e. its neither side is connected to ground since A_V is large.

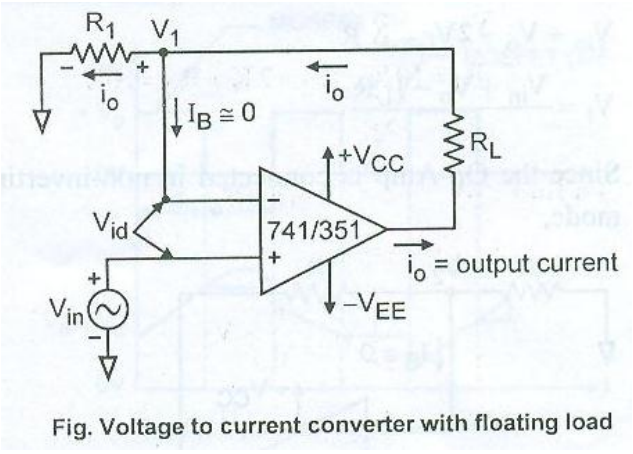


Fig. Voltage to current converter with floating load

- Derivation:
  V_{id}= 0 and this means
  V_{in}= V_1
  = $R_1 I_L$
  Therefore,
  $I_L = V_{in}/ R_1$
  Since I_L is load current through R_L at output, the input V_{in} is converted into an output current V_{in}/ R_i

b. Describe the operation of instrumentation amplifier using two Op amp with neat circuit diagram.

Ans b. **Diagram: 2M; operation: 2M**

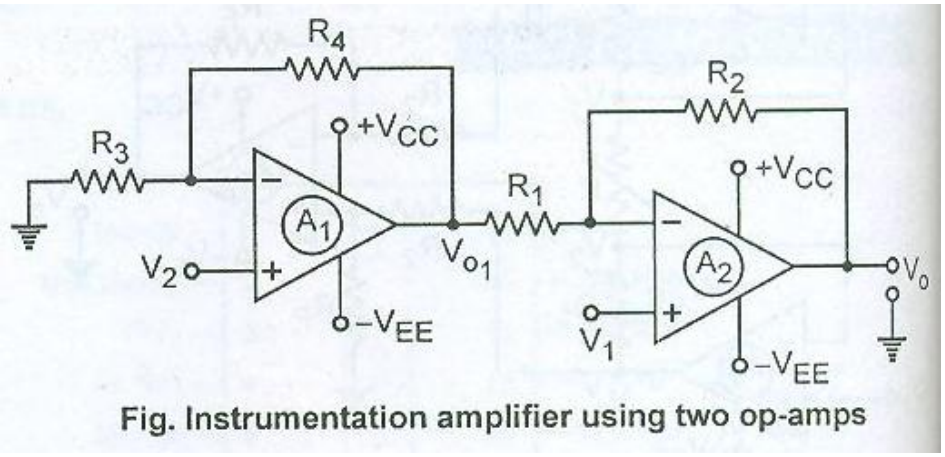


Fig. Instrumentation amplifier using two op-amps

Derivation :-

Op amp A_1 is in non-inverting mode,

$$\therefore V_{o1} = \left(1+\frac{R_4}{R_3}\right) V_2 \quad \text{---} \quad (1)$$

As op-amp A_2 is a differential amplifier or subtractor

$$\therefore V_o = V'_{o1} + V''_{o1}$$

$$\therefore V'_{o1} = -\frac{R_2}{R_1} \times V_{o1}$$

$$V''_{o1} = \left(1+\frac{R_2}{R_1}\right) V_1$$

$$\therefore V_o = -\frac{R_2}{R_1} V_{o1} + \left(1+\frac{R_2}{R_1}\right) V_1 \quad \text{---} \quad (2)$$

Putting equation (1) & (2) we get,

$$V_o = -\frac{R_2}{R_1}\left(1+\frac{R_4}{R_3}\right) V_2 + \left(1+\frac{R_2}{R_1}\right) V_1$$

Assuming,

$R_4 = R_1$, $R_3 = R_2$

$$\therefore V_o = -\frac{R_2}{R_1}\left(1+\frac{R_1}{R_2}\right) V_2 + \left(1+\frac{R_2}{R_1}\right) V_1$$

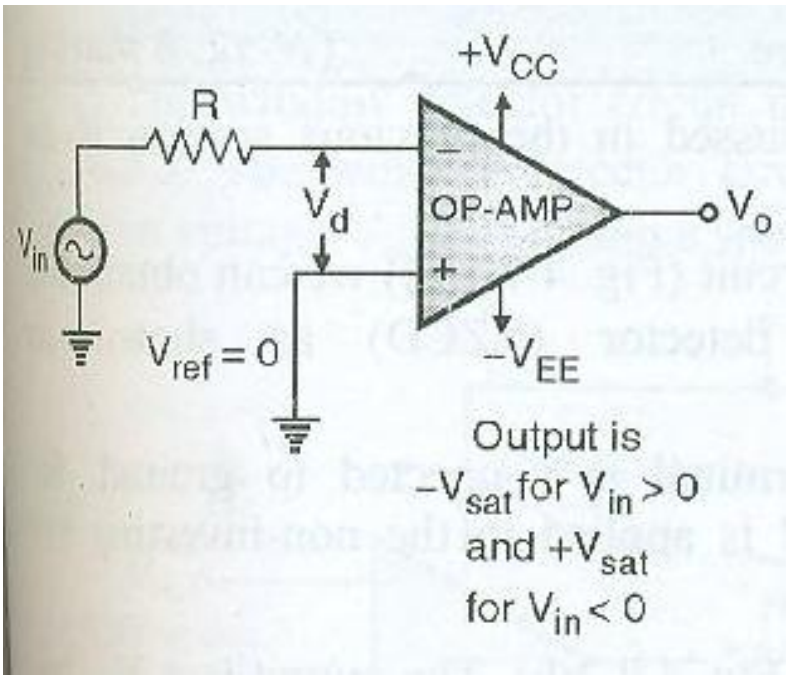
$$\therefore V_o = -\left(1+\frac{R_2}{R_1}\right) V_2 + \left(1+\frac{R_2}{R_1}\right) V_1$$

$$\therefore \boxed{V_o = \left(1+\frac{R_2}{R_1}\right)(V_1 - V_2)}$$

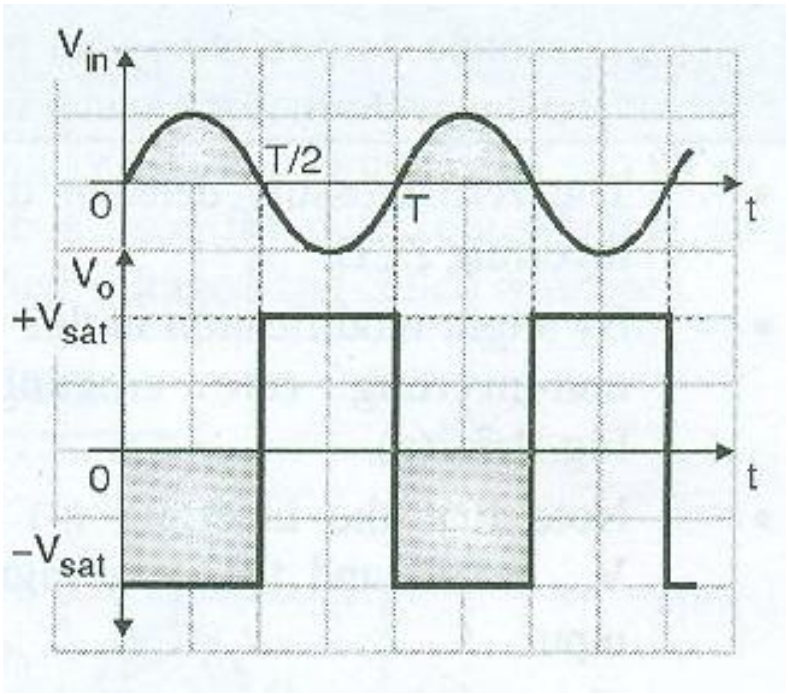
$$\boxed{\text{Gain} = A_V = \frac{V_o}{V_1 - V_2} = 1+\frac{R_2}{R_1}}$$

c. Draw the circuit of zero crossing detectors. Draw its input and output waveforms.

Ans c. **Circuit: 2M; Waveform:2M**



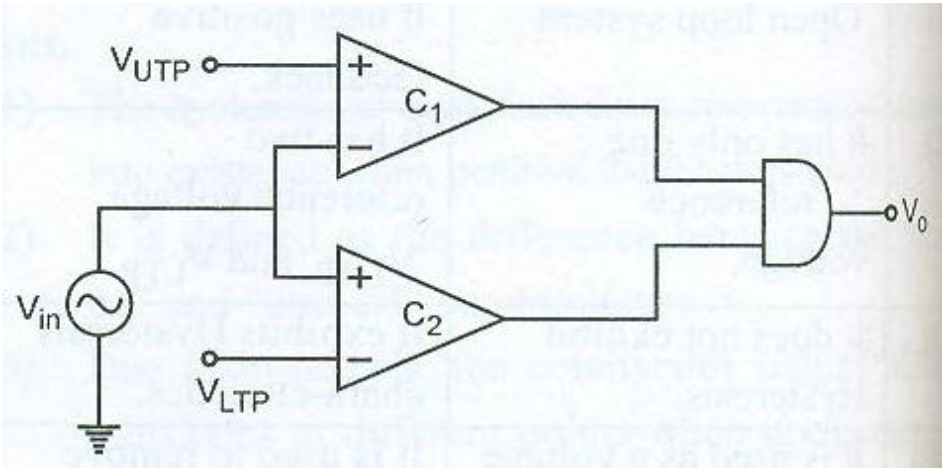
Zero crossing detector



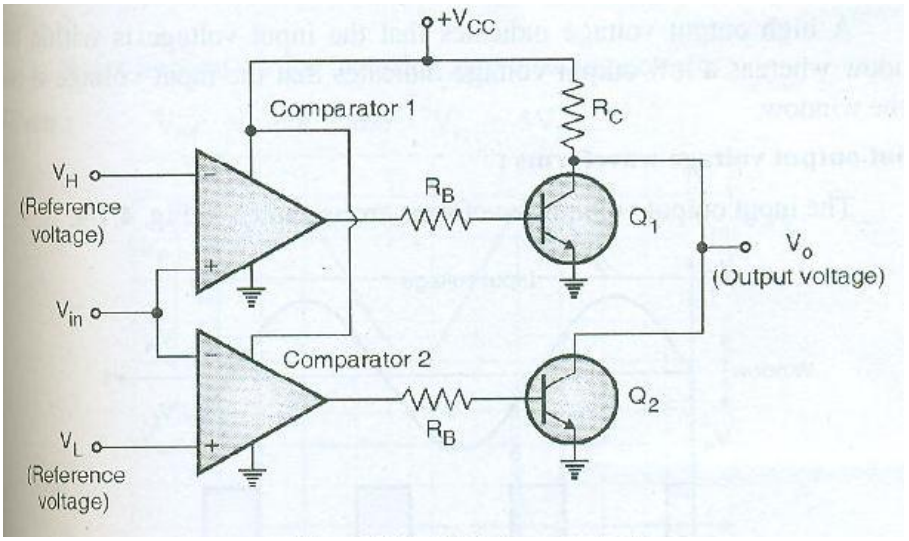
Input Output Waveforms

d. Draw the circuit of window detector. Describe operation of it.

Ans d. **Circuit:2M; Operation:2M**



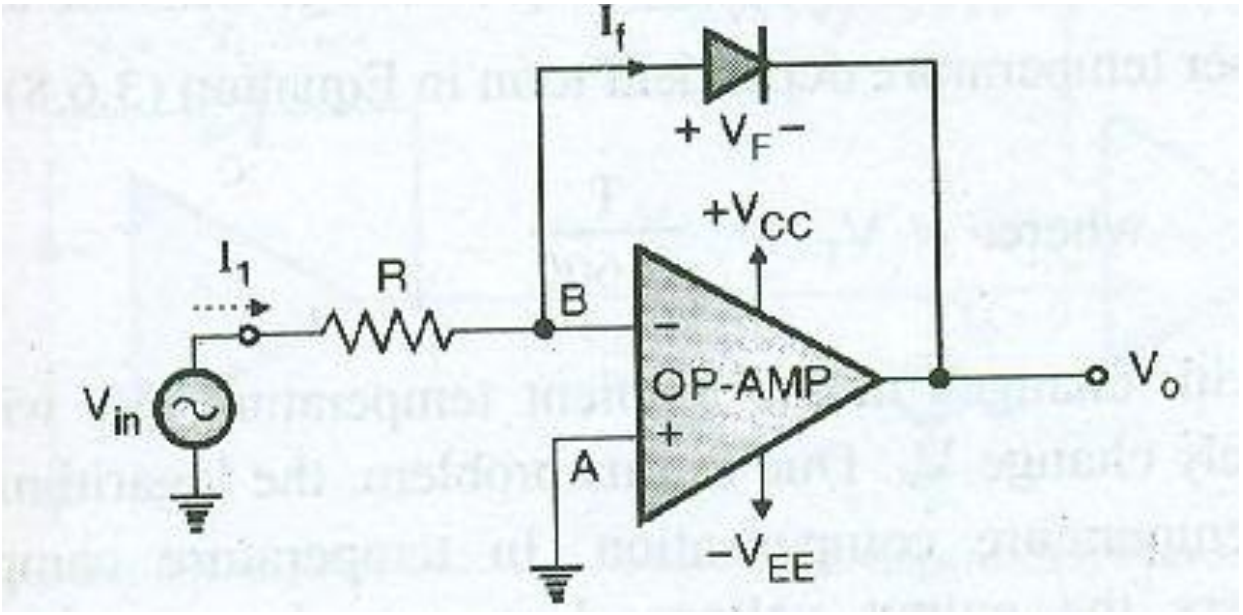
(OR)



- The window detector uses two comparator C_1 and C_2.
- The reference voltage of inverting comparator C_1 is V_{UTP} and the reference voltage of the non-inverting comparator C_2 is V_{LTP}. Assume $V_{LTP} < V_{UTP}$
- Case I: When $V_{in} < V_{UTP}$ then the differential voltage of C_2 is negative. Hence output of C_2 is low. V_{in} is also less than V_{UTP}. Hence output of C_1 is high and output V_o of AND gate is low.
- Case II: When $V_{in} > V_{UTP}$, then the differential input voltage of C_2 is high. The differential input voltage of C_1 is negative. The differential input voltage of C_1 is negative. Hence output of C_1 is low and output V_o of AND gate is low.
- Case III: When $V_{LTP} < V_{in} < V_{UTP}$, the differential input voltage of C_1 and C_2 is positive and output is high. The output of AND gate is high.

e. Describe the operation of logarithmic amplifier with neat circuit diagram.

Ans e. **Circuit Diagram – 2 Marks, Operation – 2 Marks**



- A p-n junction diode is connected in the feedback path. Therefore the output voltage is nothing but the voltage across this diode.
- Therefore $V_o = -V_F$ --------1
- Due to high impedance of OP- AMP the current going into the inverting terminal is zero
- Therefore $I_1 = I_F = V_{in}/R$--------2

$$V_o = -\eta V_T [\log_e (I_f) - \log_e (I_o)]$$

$$= -\eta V_T [\log_e (V_{in}/R) - \log (I_o)]$$

$$\text{Thus } V_o = -\eta V_T \log_e \left[\frac{V_{in}}{R \cdot I_o}\right]$$

$$\therefore V_o = -\eta V_T \log_e \left[\frac{V_{in}}{V_{ref}}\right]$$

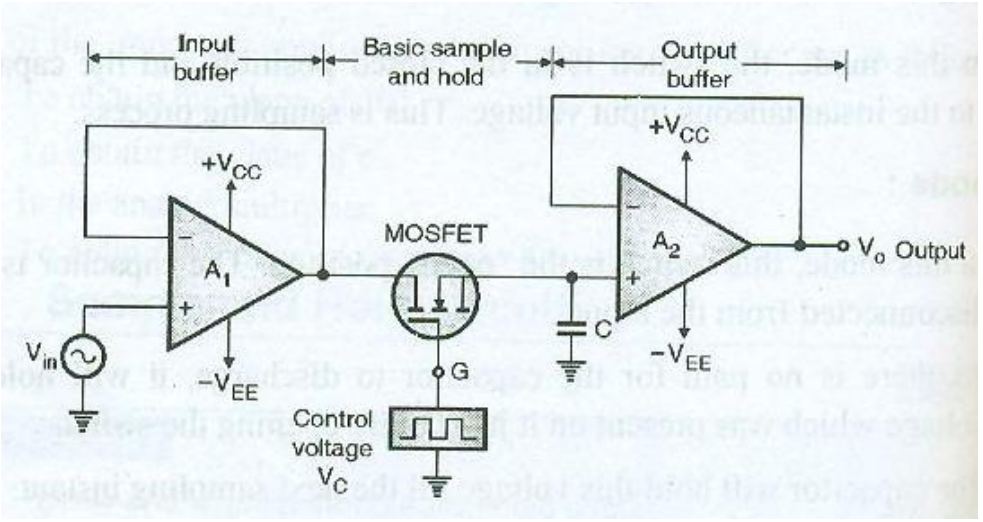
where $V_{ref} = R \cdot I_o$ = fixed dc voltage.

- The output voltage is proportional to the logarithm of input voltage.
- The output is in terms of natural log i.e. $\log_e$. If we want the output to be in terms of $\log_{10}$ then we should use the following conversion equation:
  $\log_{10} V_i = 0.434 \log_e (V_i)$

f. Describe the working of sample and hold circuit with circuit diagram.

Ans f. **Circuit Diagram – 2 Marks, Operation – 2 Marks**

- The n channel MOSFET is driven by a control voltage V_C acts as a switch. The control voltage V_C is applied to the gate of the MOSFET.
- The circuit diagram can be spilt into three stages. First stage is the voltage follower second one is the switch and capacitor and the third one is again the voltage follower.
- When V_C is high the MOSFET turns on and acts like a closed switch. This is sampling mode. The capacitor charges through the MOSFET to the instantaneous input voltage.
- As soon as V_C= 0 the MOSFET turns off and the capacitor is disconnected from OP-AMP 1 output. Capacitor cannot discharge through amplifier A_2 due to its high impedance.
- Thus this is the hold mode in which the capacitor holds the latest sample value.



Sample and hold circuit

4 . Attempt any four of the following: **16**

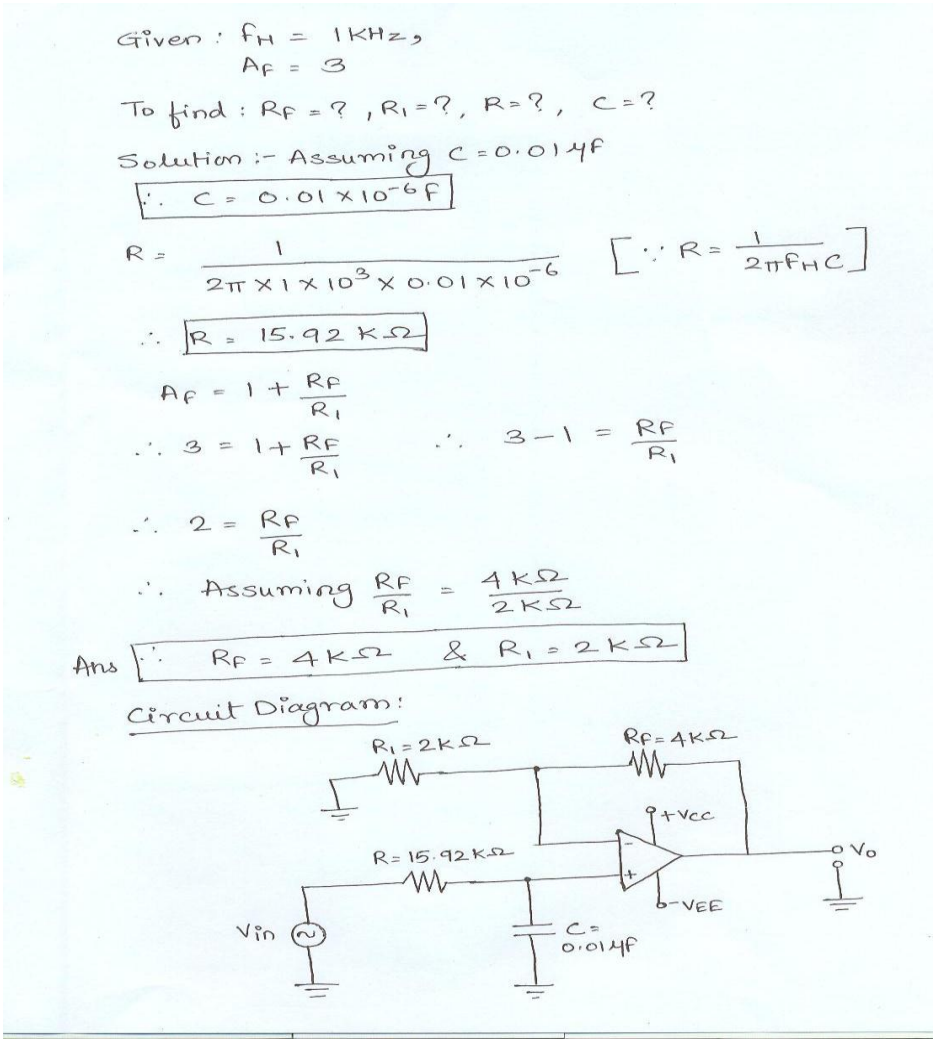
a. Compare comparator and regenerative comparator (Schmitt trigger) on four points.

Ans a. **Any four relevant points- 4M**

Sr. No	Comparator	Schmitt trigger
1	Open loop system	It uses positive feedback
2	It has only one reference voltage	It has two reference voltage V_{UTP} and V_{LTP}
3	It does not exhibit hysteresis	It exhibits hysteresis characteristics
4	It is used as a voltage level detector	It is used to remove the noise between two reference voltages due to hysteresis

b. Design first order low pass filter with 1 KHz cut off frequency and pass band gain 3

Ans b. **Value of R= 1M, Value of R_F& R_1= 1M, Design= 2M**



c. Compare active filters and passive filters on four points.

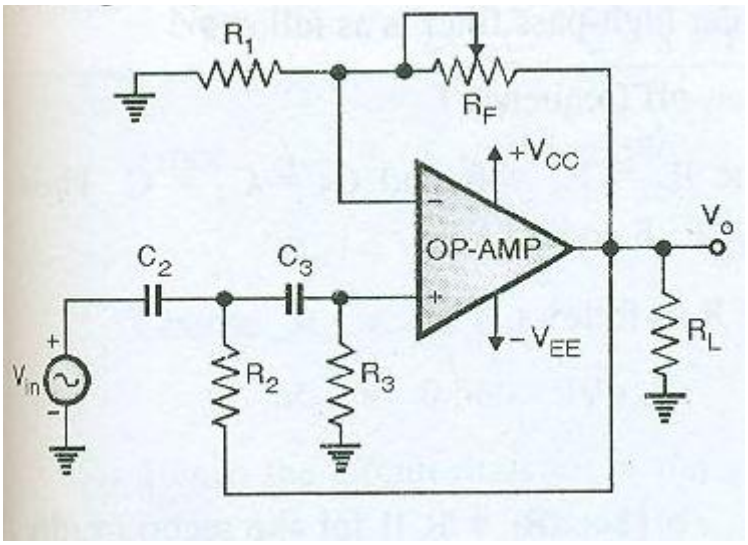
Ans c. **Any four points-4M**

Sr.No	Parameter	Active filters	Passive filters
1	Components used	Uses active elements such as op amp and transistors	Uses passive elements such as capacitors, inductance
2	Gain	High gain filter	Low gain filter
3	Frequency adjustment	Easier to tune	Not easy to tune
4	Loading Problem	Since high input and low output impedance hence causes no loading problems	Causes loading problem
5	Cost	Cost of op amp is less and are available in large varieties	Cost of large inductor increases the cost of the filter

6	Handling	Portable and contains less components	Not as handy as active filter
7	Building capability	Easier to build and changes can be done easily	Not as easy as in active filters

d. Draw the second order high pass filter and describe its operation.

Ans d. **Diagram: 2M; Explanation: 2M**



Second order high pass filter

- The resistors R_1 and R_F will decide the gain of the high pass filter. The gain can be made variable by keeping R_F variable.

The cut-off frequency f_c is determined by R_2, R_3, C_2 and C_3 as follows:

$$f_c = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

- The voltage gain magnitude is given by,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{VF}}{\sqrt{1+(f_c/f)^4}}$$

$A_{VF} = 1 + \frac{R_F}{R_1}$ = Passband gain of the filter.

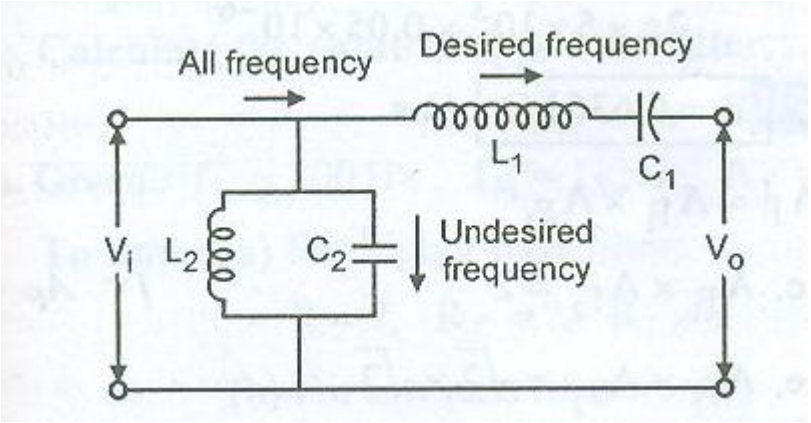
- The frequency response of the second order filter. It shows that the gain increases at a rate of 40 db/ decade in the attenuation band. This is doubled the rate of first order filter. This makes the frequency the frequency response sharper.
- The second order filters are important because they can be used for designing the higher order filters.

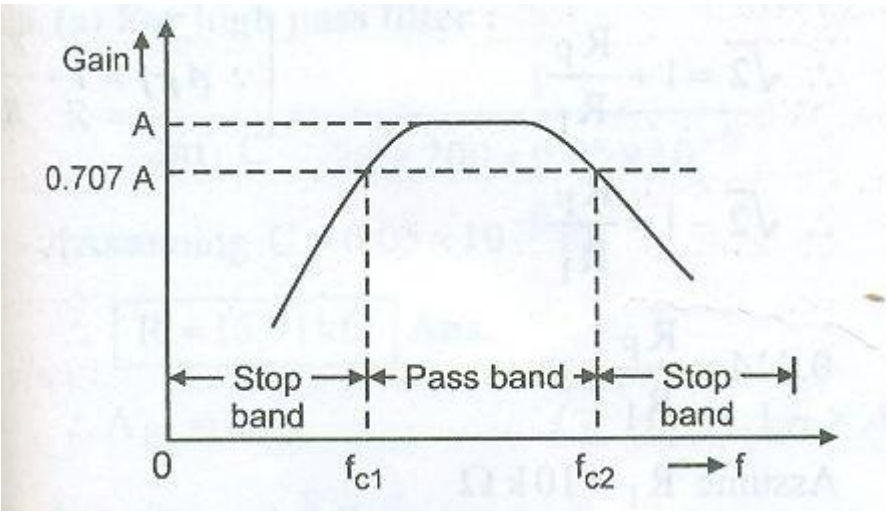
e. Describe the working of band pass filter with neat circuit diagram.

Ans e. **working: 2M; Neat circuit diagram: 2M**

Note: Any 1 type of band pass filter (wide band or narrow band) should be considered

- Figure shows the circuit of band pass filter. This filter transmits a specified band of frequencies and stops others as shown in figure.(pass band between f_{C1} and f_{C2})
- The filter consists of two resonant circuits, one connected in series with the line and the other across it. Both are tuned to the same frequency.
- The series resonant circuit passes whose frequencies are at or near its resonant frequency and blocks all those whose frequencies outside the narrow band.
- However, these blocked frequencies get shunted out of the circuit by the parallel resonant circuit which offers them very little impedance.
- This circuit transmits all those frequencies whose values lie between the cut off frequencies f_{C1} and f_{C2} and stops all frequencies lying either below f_{C1} or above f_{C2}.





f . Draw the circuit of notch (narrow band reject) filter and describe its operation.

Ans f. **Circuit: 2M; Operation: 2M**

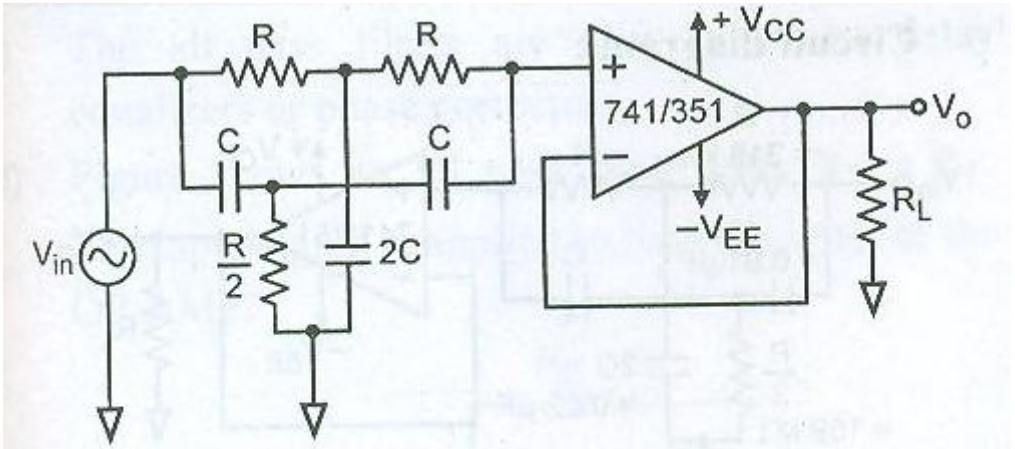


Fig. (a) Narrow band reject filter

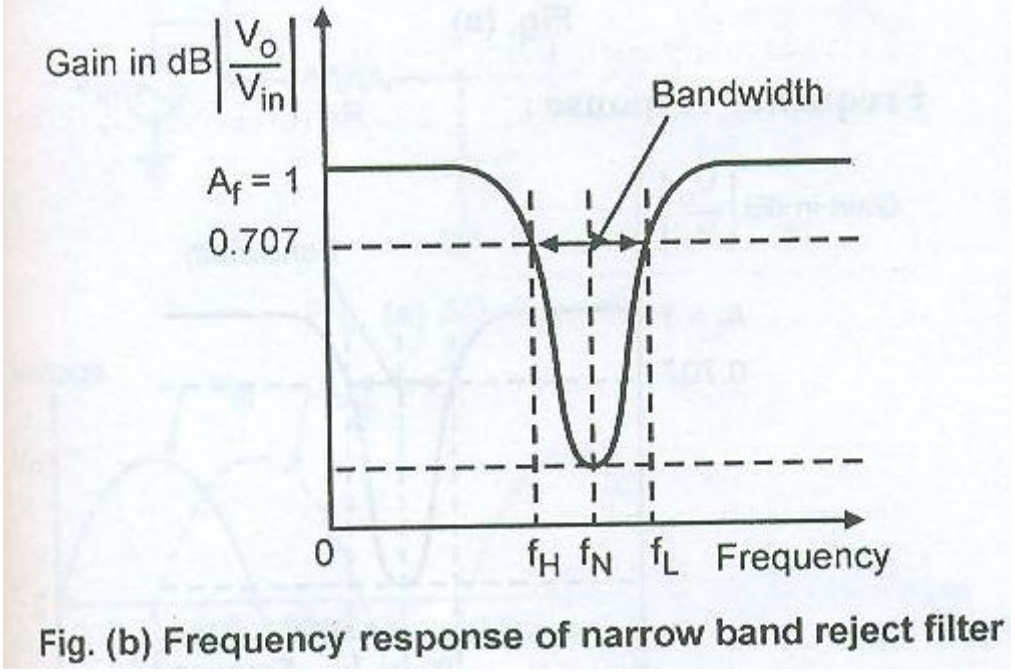


Fig. (b) Frequency response of narrow band reject filter

i. Fig. shows a narrow band rejects active filter often called as Notch filter. It uses a twin T- network.

ii. The twin T- network is a passive filter composed of two T- shaped networks.

iii. One T- network is made up of two resistors and capacitors while the other uses two capacitors and a resistor.

iv. The notch out frequency is the frequency at which maximum attenuation occurs, it is given by

$f_N = 1/ 2\pi RC$ Hz---------- (1)

v. The twin T- network has very low figure of merit Q. this is increased by using it with a voltage follower as shown in fig. The output of the voltage follower is fed back to the junction of R/2 and C.

vi. Q> 10 for narrow band reject filter.

vii. One typical application of such filter is for rejection of single frequency, such as 50 Hz power line frequency hum. This notch filter is also used in communication and Bio- medical instruments for eliminating undesired frequencies.

viii. Frequency in equation (1) is the frequency to be rejected. Choosing C≤ 1μF and then calculate for R, from the equation.

5. Attempt any FOUR of the following: 16

a. Draw the functional block diagram of Timer IC 555. State function of internal resistors of 5kΩ in IC 555.

Ans a. **Block Diagram: 2M; function: 2M**

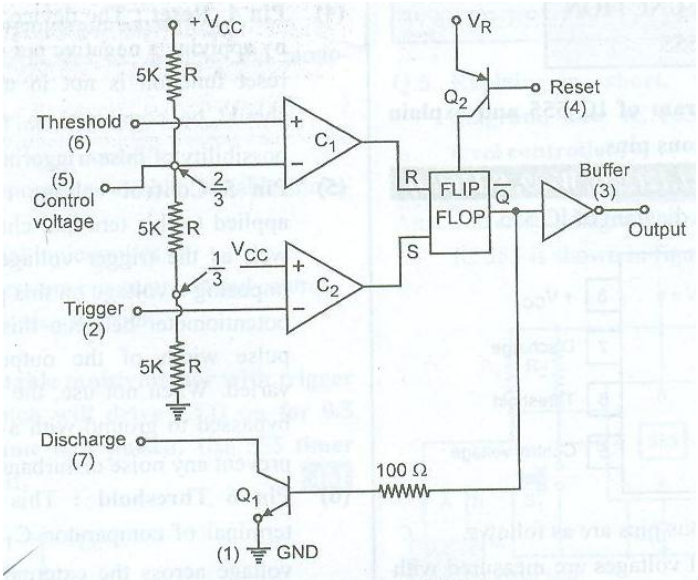
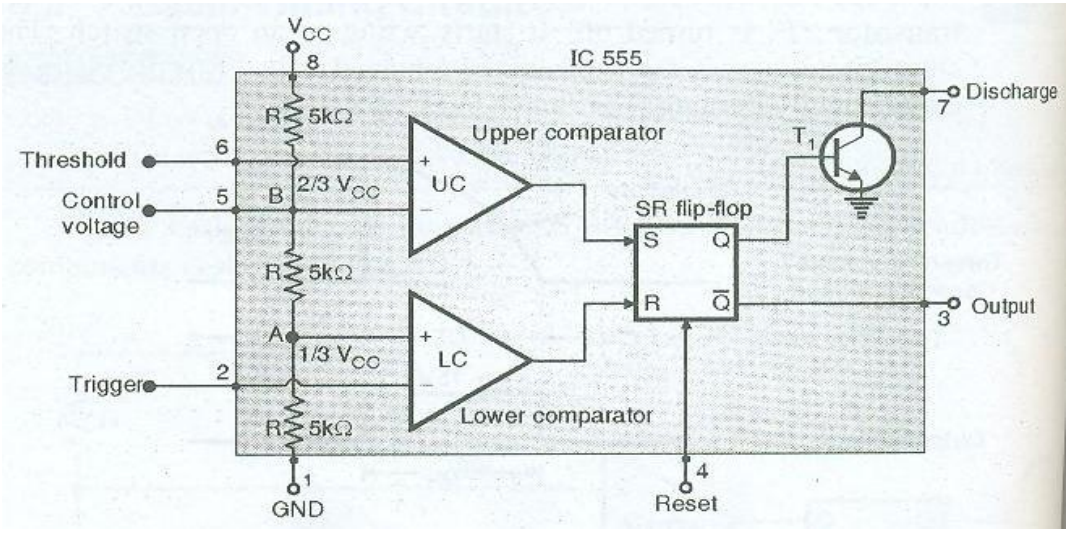


Fig. Block diagram of IC 555

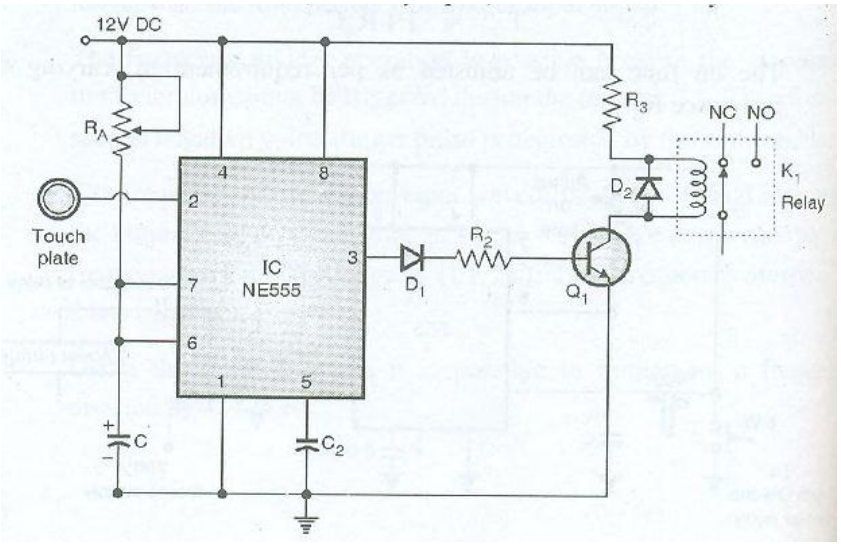
OR



The comparator reference voltages are fixed at 2/3 V_{CC} for C_1 and 1/3 V_{CC} for C_2 by means of voltage divider made of 3 resistors.

b. Describe the application of IC 555 as touch plate switch. Draw the circuit diagram of it.

Ans b. **Application: 2M; Circuit Diagram: 2M**



(OR)

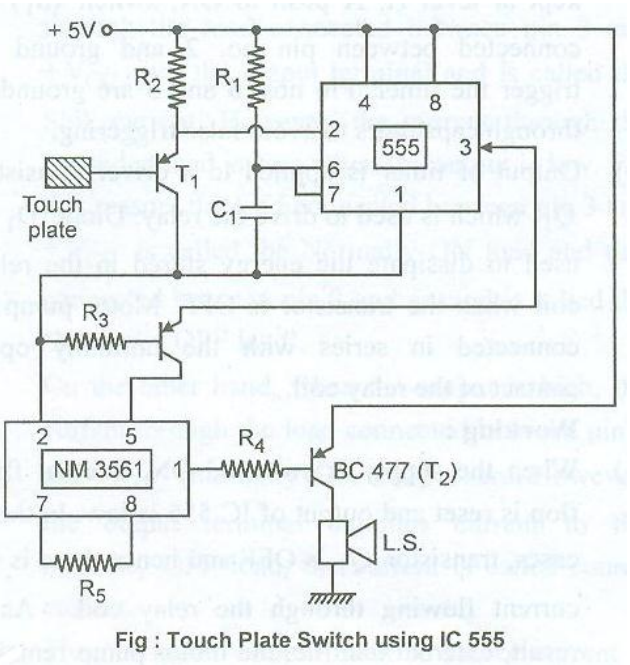


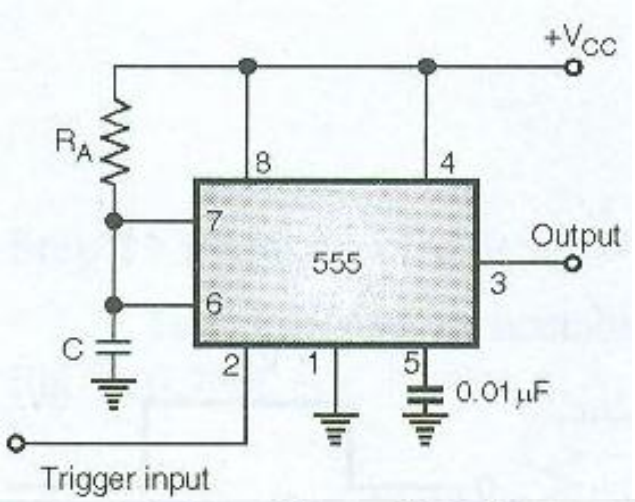
Fig : Touch Plate Switch using IC 555

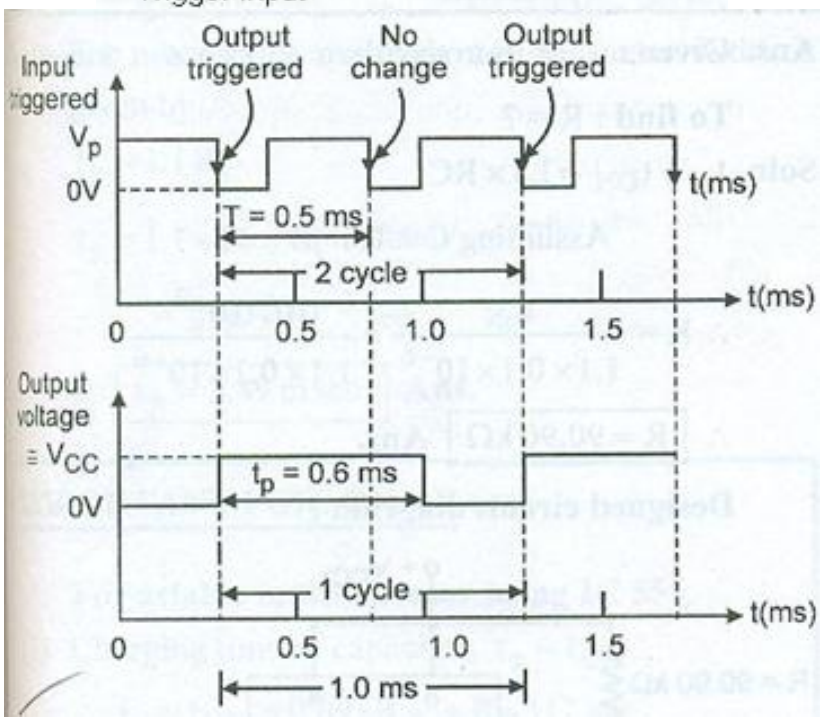
- When this circuit is connected to a metal locker or cupboard, generates an alarm when touched by an undesirable entity.
- The transistor gets saturated by just touching its base. The 50 Hz hum present in our body is the key to this circuit. The circuit is basically a burglar alarm with timer. Timer circuit is a monostable multivibrator.
- If the sensor, which is base of the transistor T_1, touched by the finger, transistor T_1, is saturated. Now the voltage at pin 2 of IC_1 is less than 1/3 V_{CC}. As a result IC_1 gets a trigger pulse at its trigger input pin 2. Therefore its output goes high for a predetermined time period.
- The period can be adjusted by varying the value of resistor R_1 or capacitor C_1 as $T= 1.1R_1C_1$ sec.

c. Describe the operation of frequency divider using IC 555 with suitable diagram.

Ans c. **Operation: 2M; Diagram: 2M**

- The monostable multivibrator can be used as frequency divider by adjusting the length of the timing cycle t_p with respect to time period T of the trigger input signal applied to pin 2.
- To use the monostable multivibrator as divide by 2 circuit, the timing interval t_p must be slightly larger than the time period T of the trigger input signal as shown in figure below. By the same concept, to use the monostable multivibrator as divider by 3 circuit, t_p must be slightly larger than twice the period of the input trigger signal and so on.
- The frequency divider application is possible because the monostable multivibrator cannot be triggered during the timing cycle.





d. Draw block diagram of PLL and describe the function of each block.

Ans d. **Block Diagram: 2M; Function: 2M**

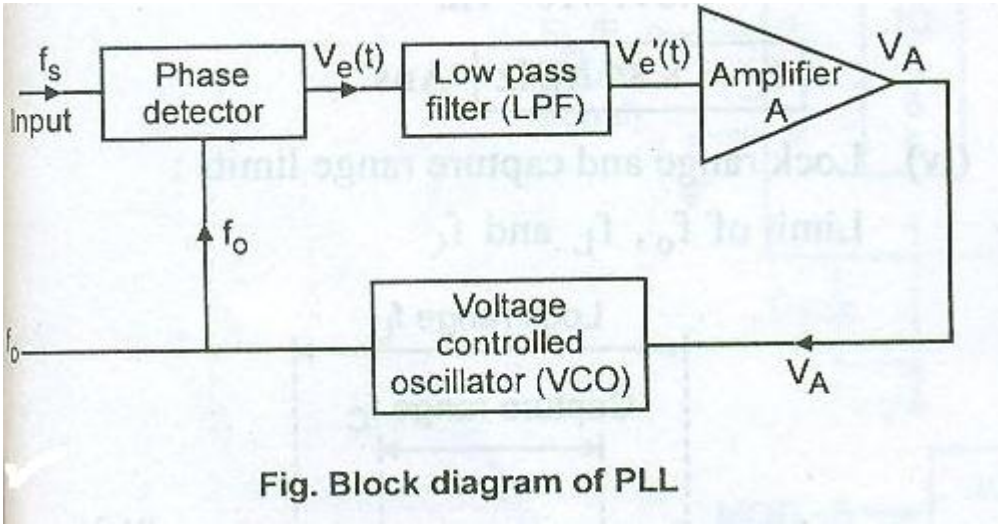


Fig. Block diagram of PLL

Here f_s is the signal frequency & f_o is the output frequency.

- The voltage controlled oscillator (VCO) is a free running multivibrator and operates at a frequency f_o, which is determined by external timing capacitor and external resistor.
- The operating frequency can be shifted on either side by applying a dc control voltage V_C externally.
- The change in frequency is directly proportional to the dc control voltage applied and hence it is termed as voltage controlled oscillator (VCO).
- If an input signal frequency f_S is applied to PLL, then the phase comparator/ detector compares the phase and frequency of the input signal with the output signal or feedback signal f_o of VCO.
- If the two signals differ in frequency/ phase an error voltage $V_e(t)$ is generated.
- The phase detector used is basically a multiplier which produces the sum $(f_s + f_o)$ and difference $(f_s - f_o)$ frequency signal at the output.
- The high frequency signal $(f_s + f_o)$ is removed by low pass filter and the difference frequency signal $(f_s - f_o)$ is amplified by amplifier which is passed by low pass filter.
- This difference frequency signal is then applied to VCO. VCO shifts the frequency so as to reduce the frequency difference between f_s and f_o.
- Once this controlling action starts, the signal is in the capture range of PLL.

e. Explain the working of PLL as frequency multiplier.

Ans e. **Diagram – 2 Marks, Explanation – 2 Marks**

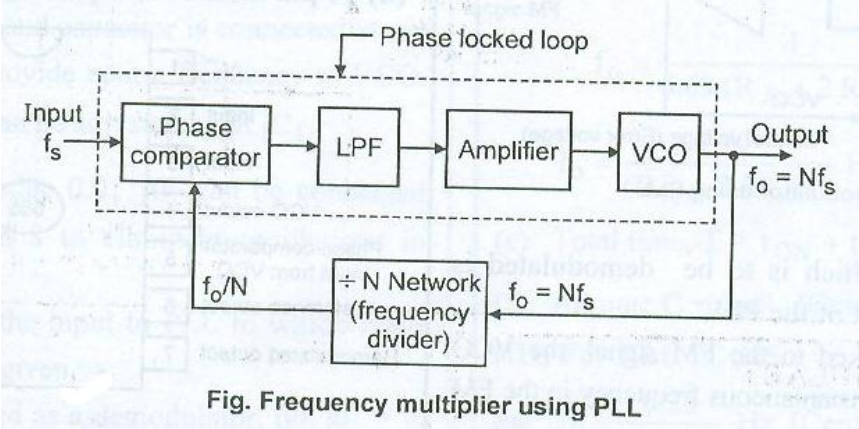
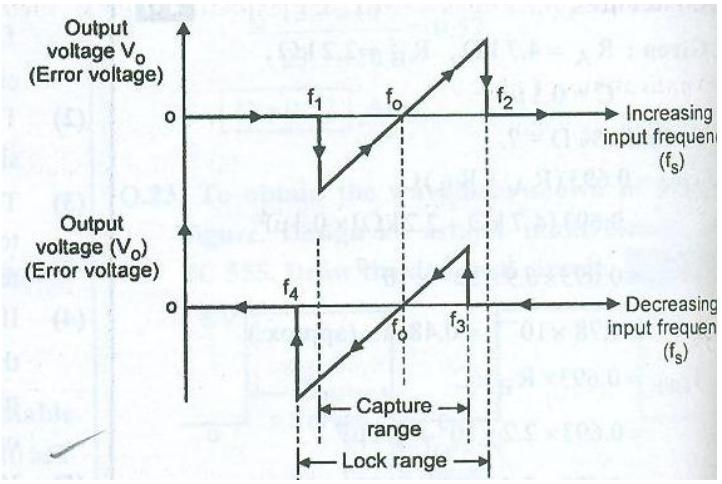


Fig. Frequency multiplier using PLL

- A divide by N network is connected externally between the VCO output and phase comparator input.
- Since the output of the divider network is locked to the input frequency f_s, the VCO actually operated at the frequency which is N times higher than f_s.
- Therefore $f_o = Nf_S$
- The multiplying factor can be obtain by proper selection of the scaling factor N.

5 Draw transfer characteristics of PLL. Define
- Lock Range and **(1M)**
- Capture range of PLL. **(1M)**

Ans g. **Characteristics: 2M**



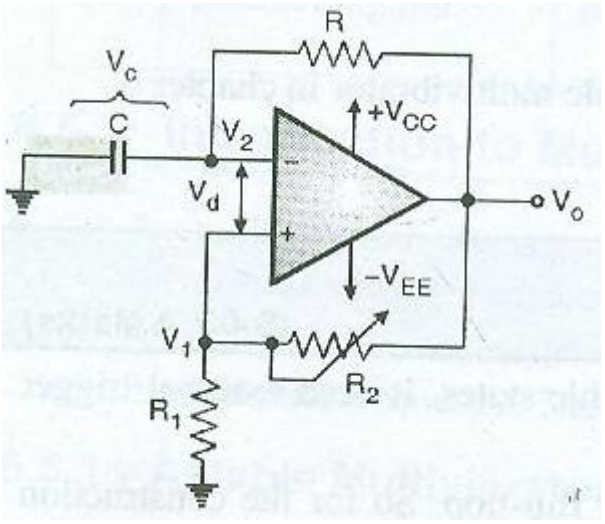
Lock in range: The range of frequencies over which the PLL can maintain the pahse lock with the incoming signal is defined as the lock in range.

Capture range: Capture range of PLL is defined as the range of frequencies over which the PLL can acquire lock with the input signal

6 . Attempt any FOUR of the following: 16

a. Draw astable multivibrator using IC 741 and state the formula for calculating frequency of output.

Ans a. **Diagram – 2 Marks, Formula – 2 Marks**



- The time period the output waveform is given by,

$$T = 2RC \log_e \left[\frac{2R_1 + R_2}{R_2}\right]$$

- The expression for output frequency is given by,

$$f_o = \frac{1}{T} = \frac{1}{2RC \log_e [(2R_1 + R_2)/R_2]}$$

- If we substitute $R_2 = 1.16R_1$ then the above equations becomes
  $f_o = 1/2RC$

b. Draw circuit diagram of Schmitt trigger using IC 555 with its input and output waveforms.

Ans b. **Circuit diagram: 2M; Waveforms: 2M**

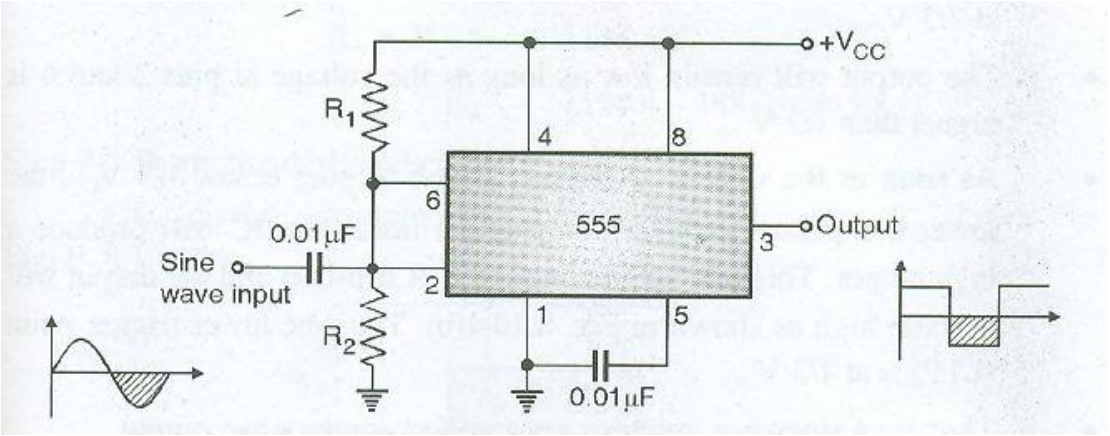


Fig: Schmitt trigger using IC 555.

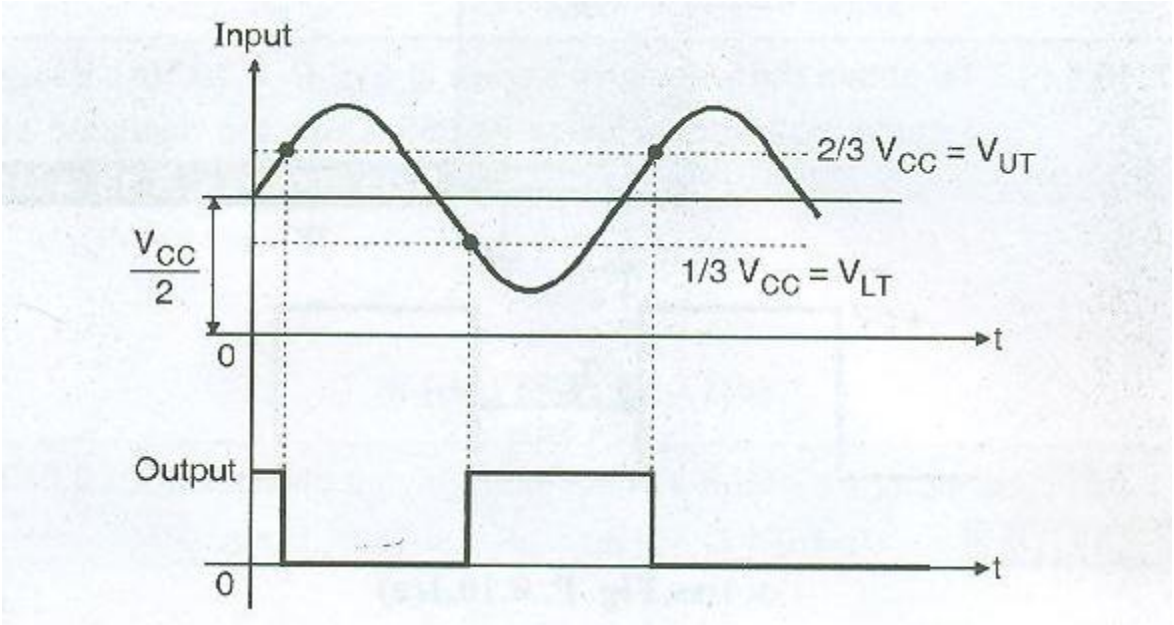


Fig: Waveforms of Schmitt trigger using IC 555

c. Draw and explain the working of phase shift oscillator using IC 741

Ans c. Diagram: 2M; Explanation: 2M

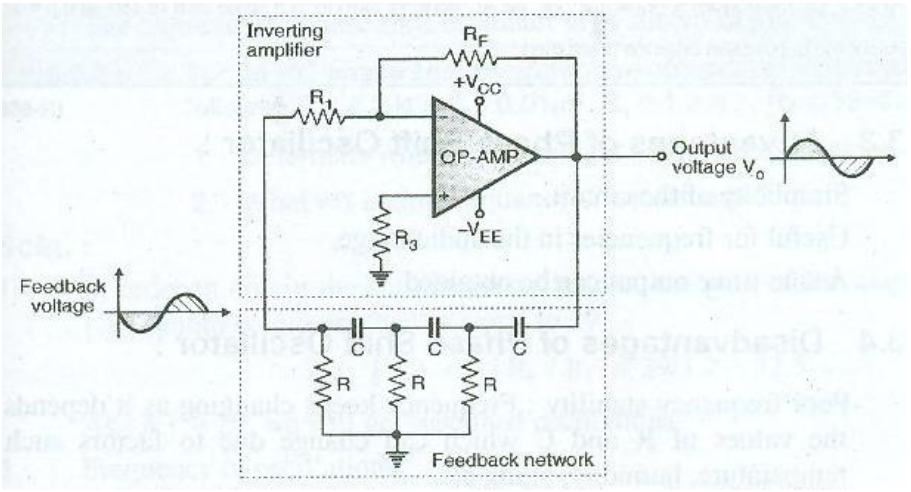


Fig: RC phase shift oscillator using OP- AMP

- The OP- AMP is used as an inverting amplifier. Therefore it introduces a phase shift of 180^0 between its input and output.
- The output of the inverting amplifier is applies at the input of the RC phase shift network. As discussed earlier, this network will introduce a phase shift of 180^o. This feedback network attenuates the signal at its input and feeds it to the amplifier input. The level of attenuation is decided by the feedback factor β.
- The gain of the inverting amplifier is decided by the values of R_F and R_1. This gain is adjusted in such a way that the product Aβ is slightly greater than 1.

- It can be proved that the value of feedback factor β at the frequency of oscillations is β=1/29. For sustained oscillations, the loop gain Aβ ≥ 1. Therefore, in order to make the loop gain Aβ ≥, the gain of the inverting amplifier A should be greater than or equal to 29.
- Gain of the inverting amplifier is given by,
  $A = R_F / R_1$
  Therefore: $R_F/R_1 \geq 29$ or $R_f \geq 29R_1$
- These values of R_F and R_1 will insure sustained oscillations.
- The expression for frequency of oscillations of an RC phase shift oscillation using OP_ AMP is given by,

$$f_o = 1/ 2\pi \sqrt{6} RC$$

d. Describe the working of voltage controlled oscillator using IC 555.

Ans d. **Diagram:2M; Working:2M**

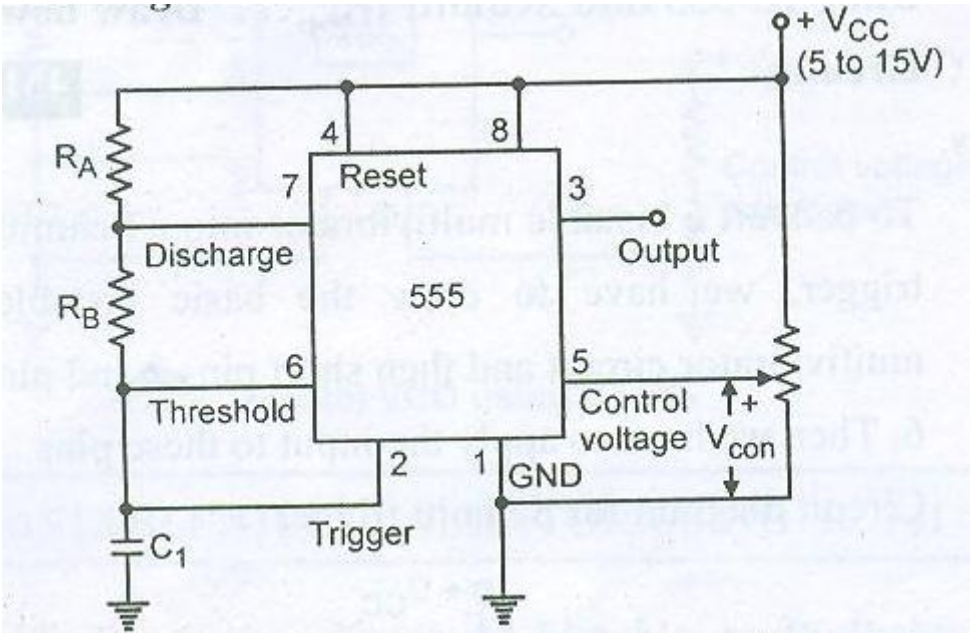


Fig: Circuit diagram of IC 555 as a VCO

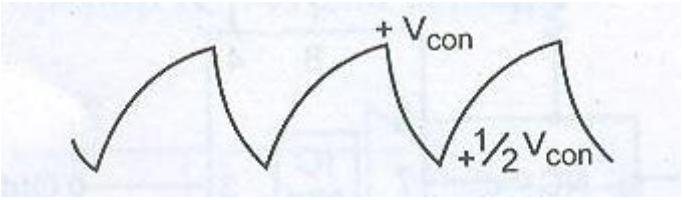


Fig: Waveform for VCO

- **T**he VCO is a system whose frequency can be varied linearly with input voltage. It is also called as voltage to frequency converter which is shown in fig.
- The pin 5 connects to the inverting input of the upper comparator. Normally the control voltage is $2V_{CC}/3$ because of the internal divider inside the IC.

- As shown in the circuit, the voltage from an external potentiometer overrides the internal voltage.
- The control voltage can be varied by varying the value of R.
- The voltage varies from $+V_{con}/2$ to $+V_{con}$. If we increase V_{con}, the capacitor takes large time to charge or discharge and therefore, the frequency decreases. Thus the frequency can be varied by varying the control voltage.

e. Draw the circuit of bistable multivibrator using IC 555 and describe its operation.

Ans e. **Circuit diagram:2M, Operation:2M**

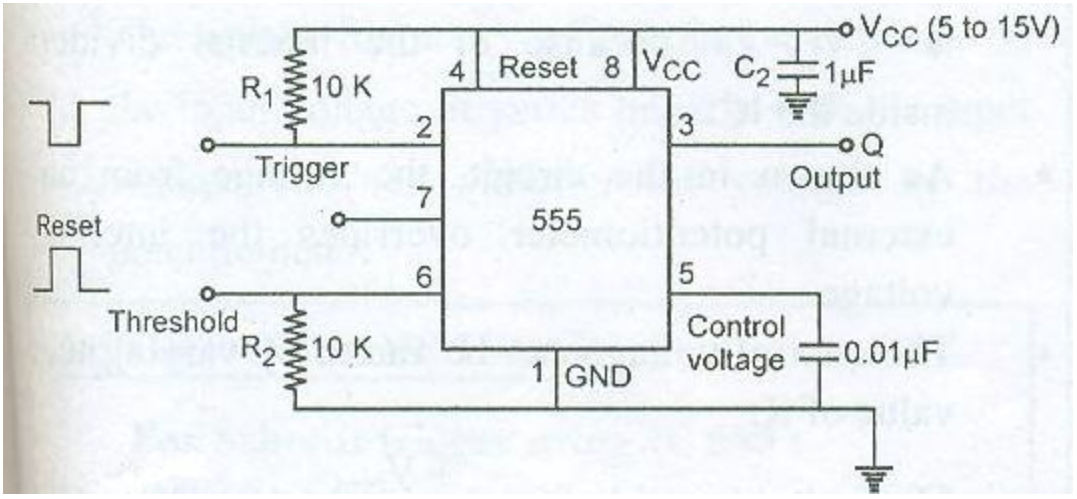


Fig: 555 timer operated as a bistable multivibrator

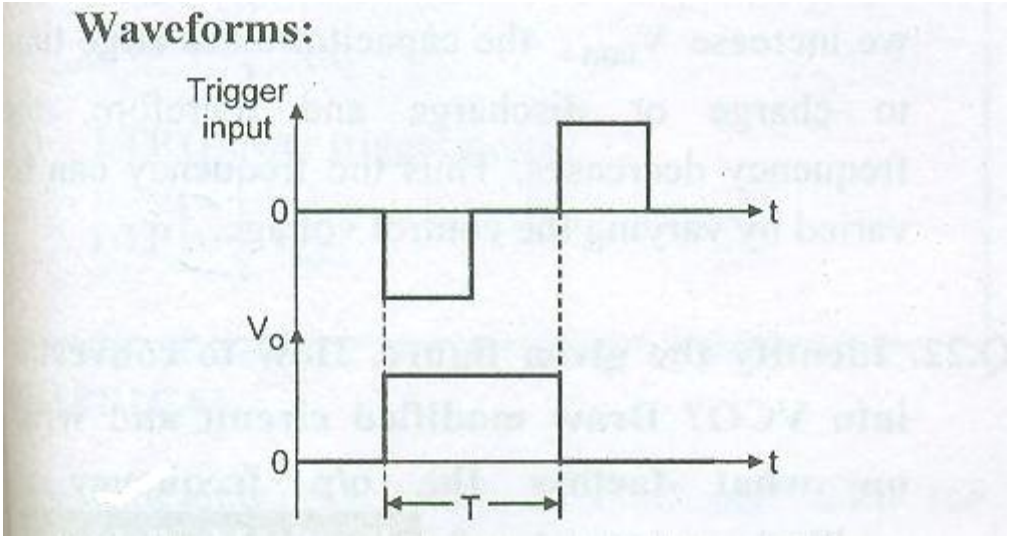


Fig: Waveform for IC 555 as a bistable multivibrator

- The IC 555 also provides a direct relay driving capability.
- In the figure, the negative pulses are applied to trigger input and that sets flip flop.

- The output goes high with the positive pulse applied to the threshold resets the flip- flop and the output goes low. Thus, with the help of the trigger, the output is forced to go from one stable state to the other.

f. Describe the working principle of wein bridge oscillator using IC 741.

Ans f. **Circuit Diagram: 2M; Working: 2M**

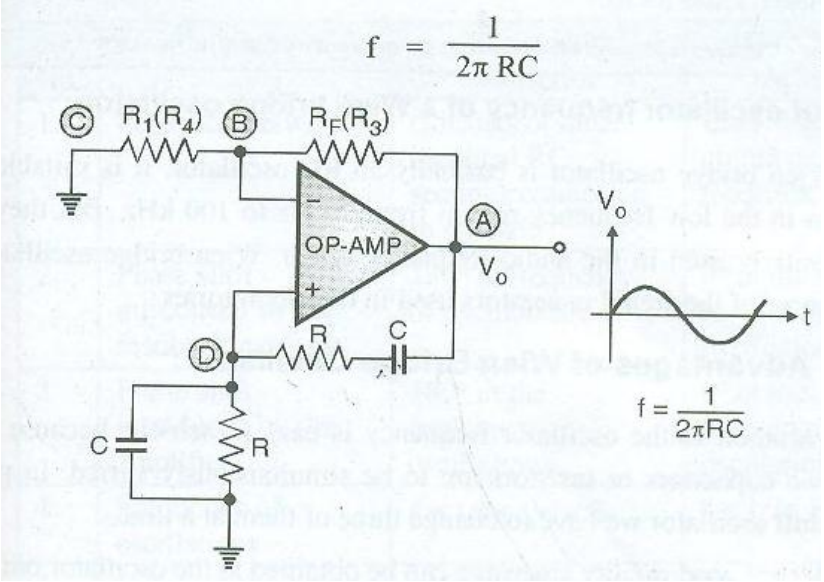


Fig: Wein bridge oscillator using OP-AMP

- The wein bridge oscillator using OP- AMP instead of transistor is as shown in fig.
- The OP- AMP output is applied as an input voltage to the Wein Bridge between points A and C. The output of the Wein Bridge which acts as the feedback network is applied to the OP- AMP input between points D and B.
- The R and C components in the frequency sensitive arms of the bridge will decide the oscillator frequency. The expression for oscillator frequency is,
- The resistor R_3 gets connected in the feedback path of OP- AMP whereas resistor R_4 get connected from the inverting (-) terminal to ground. Thus the amplifier configuration is called as the non-inverting amplifier.
- The gain of this configuration is given by:
  $A= 1+ R_3 /R_4$
- We know that at the oscillating frequency the value of feedback factor is $\beta = 1/3$ and the gain should be $A \geq 3$.
- Therefore,
  $(1+ R_3 /R_4) \geq 3$
  Therefore, $R_3 /R_4 \geq 2$
- Thus R_3 should be greater than two times the value of R_4 to ensure sustained oscillations.
- The oscillator frequency can be varied by varying both the capacitors (C) simultaneously and the amplifier gain can be changed by changing the value of resistor R_3.