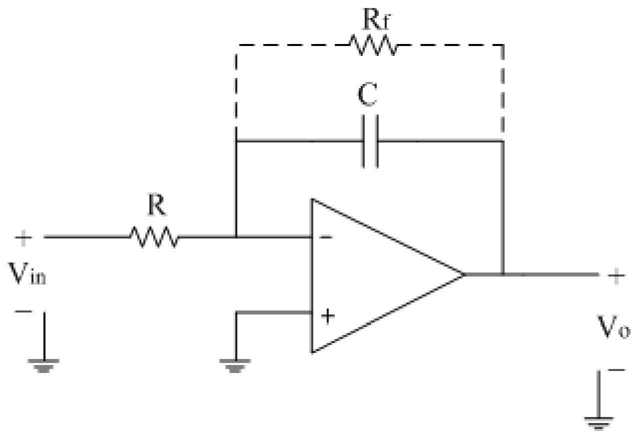
WINTER– 16 EXAMINATION
Model Answer

Subject Code: 17445

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q. N.	Answer	Marking Scheme
1	a)	**Attempt any SIX of the following:**	12
		i)Define: SVRR Slew rate	2
		Ans:- (Definition – 1mks each) 1. SVRR-It is defined as the ratio of change of input offset voltage to the change in one supply voltage while keeping other supply voltage constant . Ideally, SVRR= 0. 2. Slew rate-: It is defined as the maximum rate of change of output voltage per unit time. Ideally Slew Rate = ∞ .	
		ii)Draw practical integrator using op-amp. Ans:- (Diagram- 2 mks)	2



iii)Give applications of Instrumental Amplifier.

Ans:-Any four- 4 mks 2

i) Instrumentaiton amplifier is used in measurement of displacement.
ii) Instrumentation amplifier is used in measurement of temperature.
iii) Instrumentation amplifier is used in measurement of pressure.
iv) Instrumentation amplifier is used in measurement of humidity.
v) Electronic weighing scale.
vi) Light intensity meter.
vii) Temperature indicator & temperature controller.

iv)State the need of signal conditioning.

In an instrumentation system, a transducer is used for sensing various parameters. The output of transducer is an electrical signal proportional to the physical quantity sensed such as pressure, temperature etc.

However the transducer output cannot be used directly as an input to the rest of the instrumentation system. 2

In many applications, the signal needs to be conditioned and processed. The signal conditioning can be of different types such as rectification, clipping, clamping etc. Sometimes the input signal needs to undergo certain processing such as integration, differentiation, amplification etc.

v)State the use of Schmitt trigger.

Ans:-Schmitt trigger finds applications in(any 2- 2 mks) 2

1)To increase the Noise rejection / immunity of circuit digital circuits

2)Used as relaxation oscillator

3)Square wave generator

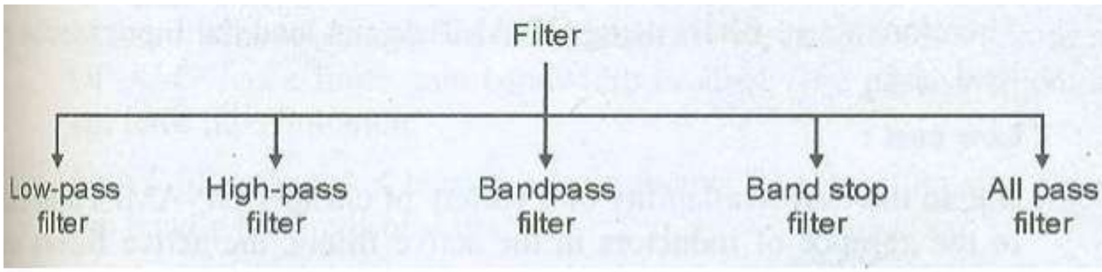
4)In the overvoltage and overcurrent protection circuits as a comparator

5)Function generator

6)Signal Conditioning

7)In the ON/OFF type temperature controllers

vi)Give classification of filters.



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vii)Define:

1)Roll off rate

2)Bandwidth

2

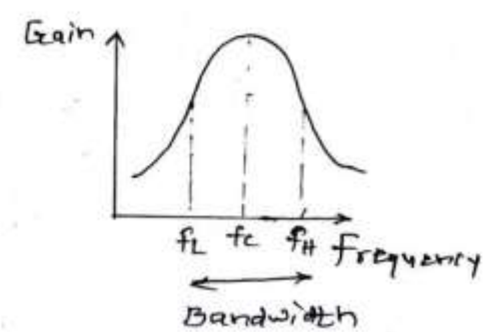
Ans:-Roll off rate:-

The rate at which gain falls off rapidly in stop band is Roll off rate.

Bandwidth:-

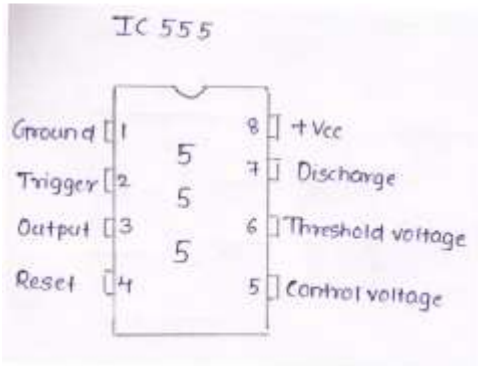
The difference between higher cutoff frequency (f_H) and lower cutoff frequency (f_L) is bandwidth.

$BW = f_H - f_L$



vii)Draw pin diagram of IC 555.

Ans:- (proper pin diagram- 2 mks) 2



1 b)

Attempt any TWO of the following: 8

i)Draw balanced input unbalanced output amplifier. State the use of need of this stage.

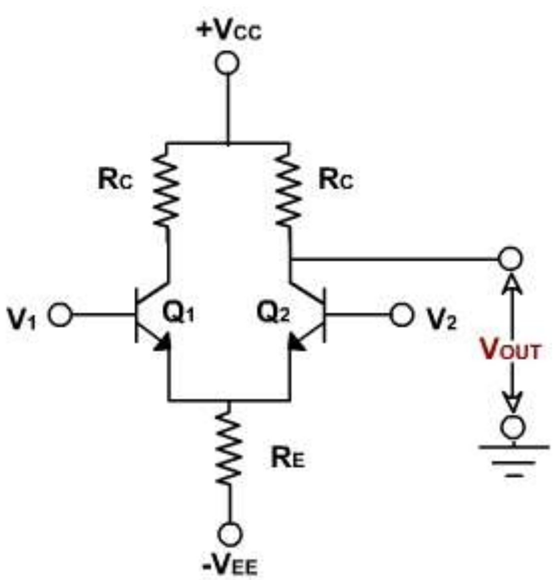
Ans:- (Diagram- 2 mks, need – 2 points -2 mks) 4

Need:-

1.Provides isolation between the two stages

2.Provides additional CMRR

3.Provides additional gain for Opamp



ii)Compare ideal and practical op-amp value w.r.t.

1)PSRR

2)Gain bandwidth product 4

3)Output offset voltage.

4)Input bias current.

Ans:-(Comparison – relevant answer- 4 mks)

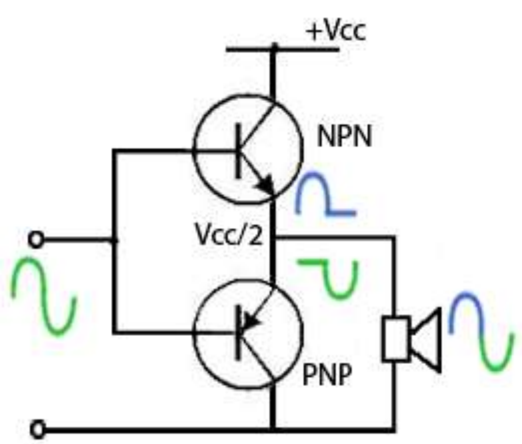
Parameters	Ideal Opamp	Practical Opamp typical values
1) PSRR	zero	150 μv/v
2) Gain bandwidth product	infinite	1 Mhz
3) Output offset voltage	zero	6mV
4) Input bias current.	zero	20nA

iii)What is the need of complementary push-pull amplifier? Draw the circuit and explain.

Ans:- (Need- 2 mks, diagram – 2mks) 4

Complementary push pull amplifier is the output stage op amp -

Output stage: This stage uses complementary symmetry push pull amplifier. This stage provides low output resistance and hence increases the current supplying capability of op-amp and also this stage increases the output voltage swing.

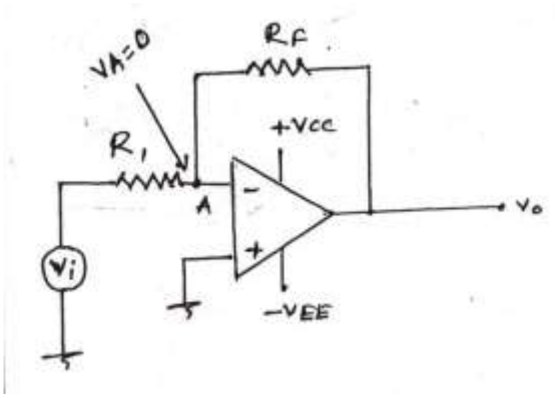


2 **Attempt any <u>FOUR</u> of the following:** 16

a) Derive the equation for virtual ground concept in op-amp.

Ans:- (diagram – 2 mks, explanation- 2 mks)

Virtual ground is a concept related to the negative feedback in an op amp.



Derivation- (description)

Potential voltage VA=0, as Non inverting terminal is grounded and Vid=0.

The voltage $V_I = 0$, implies that terminal A has same potential at terminal 2(non - inverting) since non inverting is grounded hence terminal A is also virtually grounded thus we can say that there is virtual ground at negative terminal (at A). The term virtual is used to implies that since feedback serves to keep the voltage V_i at zero, no actual current flows from negative to positive terminal i.e. inverting and non - inverting. Thus virtual ground point has a zero Voltage at A and draws no current. Due to zero potential at A this concept is called Virtual ground concept. 4

b) For unity again amplifier if Vin = +2V. What will be the output voltage? Draw the circuit diagram of unity gain amplifier.

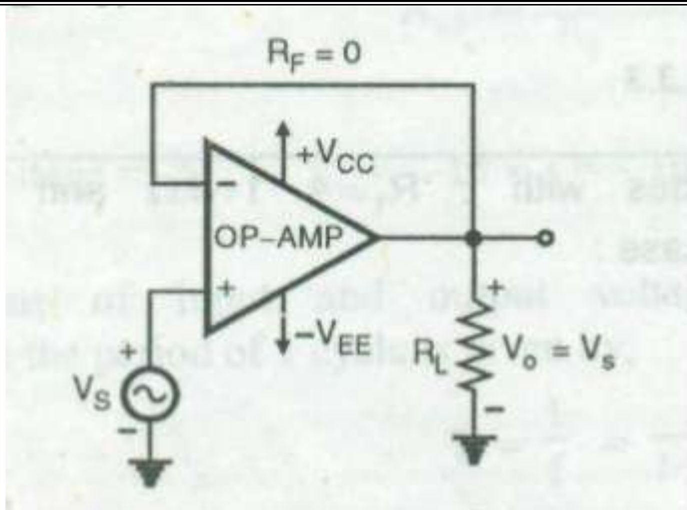
Ans:- (Explanation- 2 mks, diagram- 2 mks) 4

For input +2 V for unity gain amplifier o/p will be + 2 v only, Ie opamp is in Non-inverting mode.

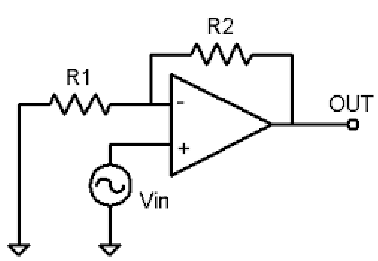
For non-inverting mode gain is given
Af=1+(Rf/R1)

When $R_1 = \infty$ and $R_F = 0$ the non-inverting amplifier gets converted into a voltage follower or unity gain amplifier.

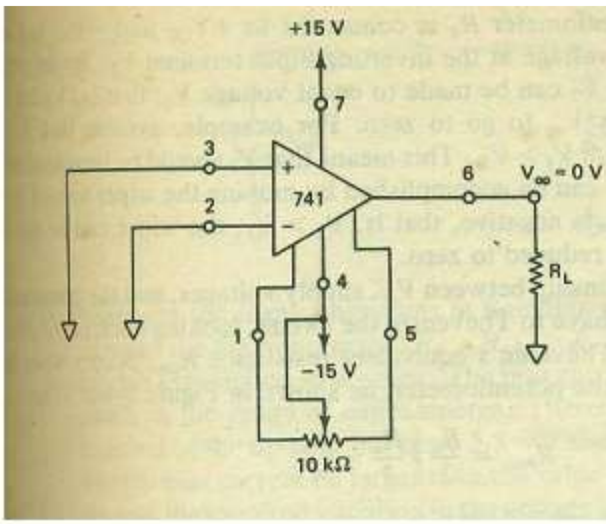
When the non- inverting amplifier is configured so as to obtain a gain of 1, it is called as voltage follower or unity gain non- inverting buffer.



	c)	Design a circuit that gives voltage gain of $\left(1+\frac{2}{3}\right)$. Ans:- (diagram – 2 mks, design values 2 mks) The circuit will be Non Inverting opamp amplifier circuit with R2/R1 = 2/3 as the gain of opamp is given as Av= 1 +(R2/R1) . The ratio R2/R1 should be 2/3. For example - Suppose R2=2KΩ then R1= 3 KΩ	4



	d)	Why offset nulling is required? Explain how is it done by using pin 1 and pin 5 with proper circuit diagram. Ans:- (Need – 2mks, diagram- 2 mks) An offset voltage exists because a real omp-amp can't be ideal. There will always be some unintended asymmetries due to random variation in manufacturing. In all cases, there are op-amp designs that can minimize these errors, but usually at the expense of some other parameter, like cost. It can be safely ignored in AC applications, where this offset will be ignored by the AC	4

		coupling. It becomes more important in DC applications, especially amplifiers, since this DC error will be amplified by the next stage. The 741 type op – amp the manufacturer recommends that a 10 kΩ potentiometer be placed across offset null pins 1 and 5 and a wiper be connected to the negative supply pin 4 . Adjustment of this pot will null the output. By varying the position of the wiper on the 10kΩ potentiometer, we are trying to remove the mismatch between inverting and non- inverting input terminals of the op- amp. Adjust the wiper until the output offset voltage is reduced to zero.  **Fig: Voltage offset null circuit**	
	e)	Design a circuit that convert square wave to spikes. Draw input-output waveforms. Ans:- (diagram- 2 mks, input output waveforms- 2 mks) The circuit suggested is a differentiator as square wave is to be converted to spikess	4

As the input square waveform is converted into spikes, the circuit suggested is differentiator.

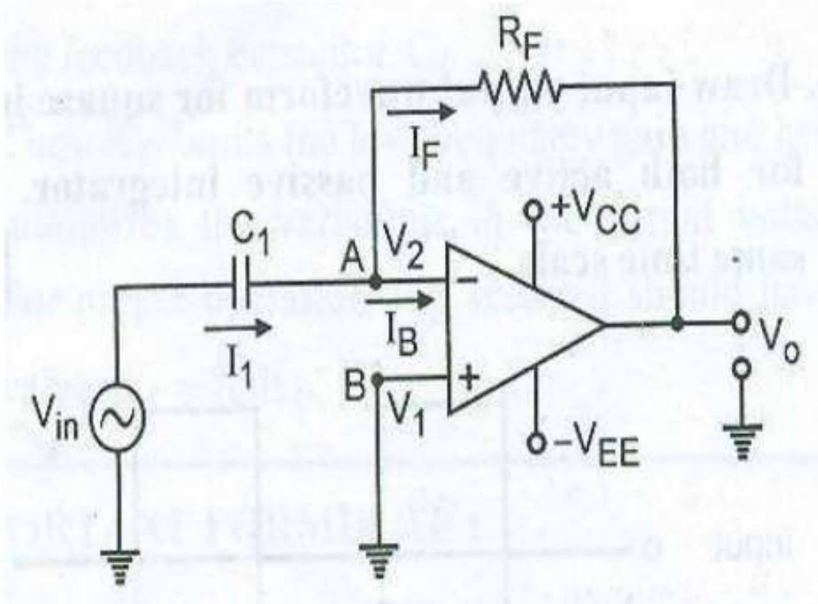
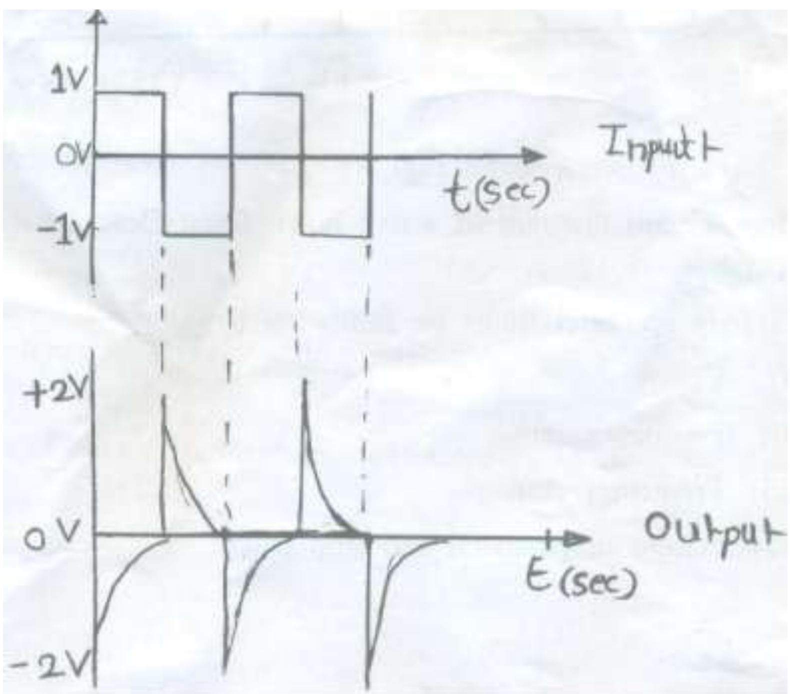


Fig. Circuit diagram of differentiator

Waveforms-



f) Design the circuit to get the output expression $V_o = -(2V_1 + V_2 + 5V_3)$.

Ans:-(design- 2 mks, diagram- 2 mks)

The given equation is opamp as adder in inverting mode whose o/p equation is given as

VO= - RF (V1/R1+V2/R2+V3/R3)

It becomes

VO = -(RF* V1/R1+ V2*RF/R2+V3* RF/R3) 4

Comparing with the given o/p equation and assuming say RF= 10 K ,

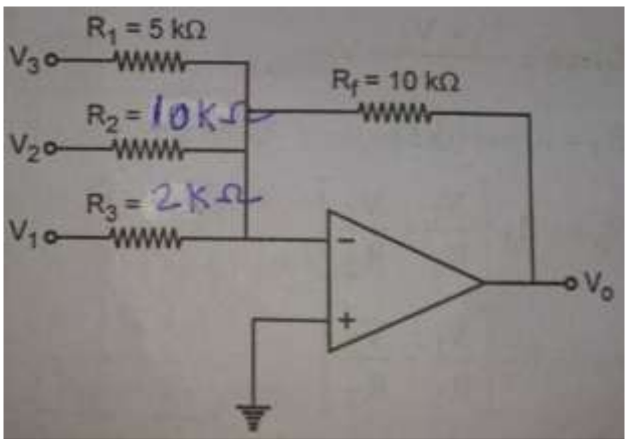
We get

RF=2 R1 , So R1=5K Ω

RF=R2= 10 KΩ

RF=5 R3, R3=2 KΩ

So the designed circuit is –



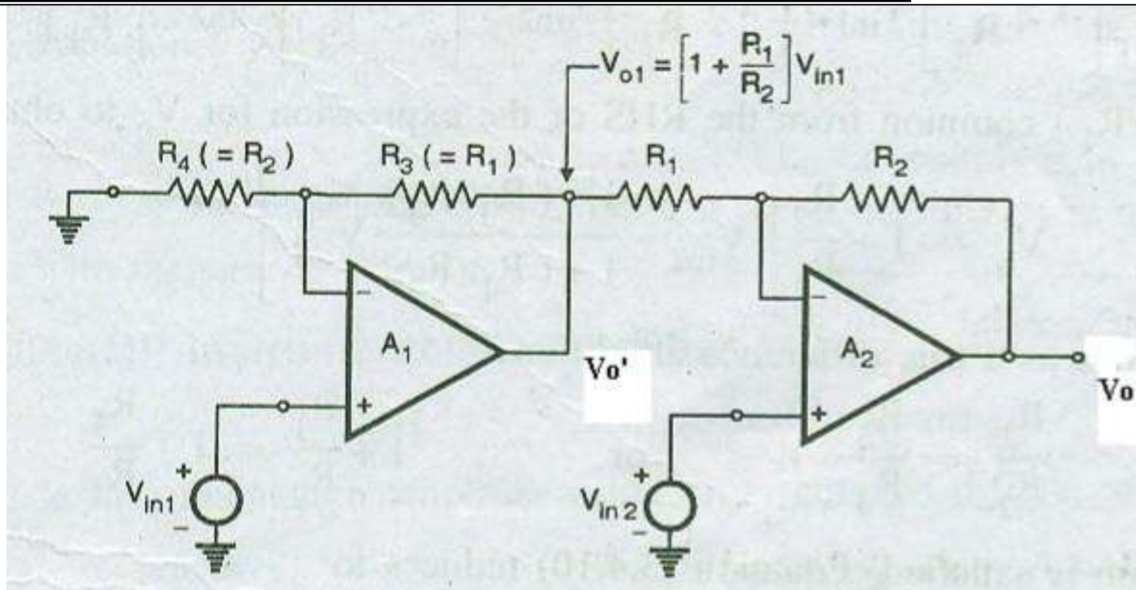
16

3

Attempt any <u>FOUR</u> of the following:

a) Draw circuit and derive equation of 2 op-amp instrumentation amplifier.

Ans:- (diagram- 2 mks, derivation- 2 mks)



4

2M

(2M)

- A_1 is an non – inverting amplifier hence its output voltage is given by,

  $V_{01} = [1 + R3/ R4] \times Vin\ 1$

- Vo1 is applied at the inverting terminal of A2. Hence its output voltage Vo can be obtained with the help of superposition theorem by considering Vo1 and Vin2 separately.
- Output voltage V'_o by considering only V_{o1}

  $V'_o = - R_2 / R_1 \times V_{o1} - - R_2 / R_1 [1 + R_3 / R_4] Vin_1$

- And the output voltage V''_o by considering only Vin_2

  $V''_o = [1 + R_2 / R_1] Vin_2$

- Hence the output voltage $V_o = V'_o + V''_o$
- Substituting the values we get,

  $V_o = - R_2 / R_1 [1 + R_3 / R_4] Vin_1 + [1 + R_2 / R_1] Vin_2$

  $= [1 + R_2 / R_1] Vin_2 – [R_2 / R_1 (1 + R_3 / R_4)] Vin_1$

- Take out $[1 + R_2 / R_1]$ common from the RHS of the expression for V_o to obtain,

$$V_o = 1 + \frac{R_2}{R_1}\left[V_{in_2} - \frac{1 + (R_3/R_4)}{1 + (R_1 + R_2)} V_{in_1} \right]$$

- The circuit will work as a true difference amplifier if

$$\frac{R_1}{R_2} = \frac{R_3}{R_4} \quad \text{or} \quad 1 + \frac{R_1}{R_2} = 1 + \frac{R_3}{R_4}$$

- When this condition is satisfied, Equation reduces to

$$V_o = \left[1 + \frac{R_2}{R_1}\right](V_{in_2} - V_{in_1})$$

b) Draw V-I converter with grounded load. Derive the equation of 'VO'.

Ans:- (diagram- 2 mks, derivation- 2 mks)

4

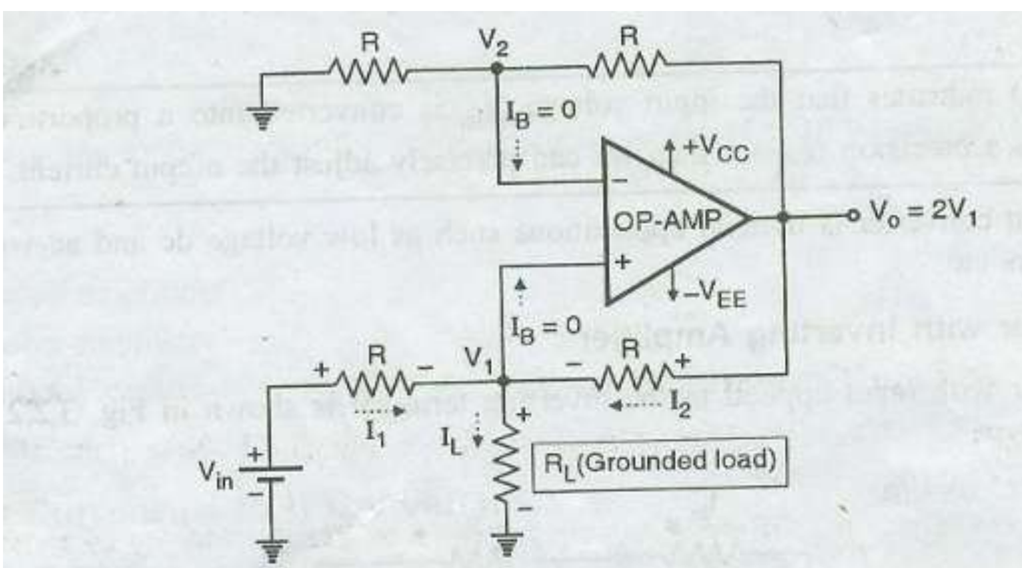


Fig. : Voltage to current converter with grounded load

Analysis of the circuit: **(1M)**

- The analysis of the circuit can be done by following two steps: First step is to determine the voltage V_1 at the non- inverting (+) terminal and the second step is to establish relationship between V_1 and the load current I_L.
- Applying KCL at node V_1,

  $I_l = I_1 + I_2$ ------------ (1)

  But $I_1 = V_{in} - V_1 /R$ and $I_2 = V_o - V_1 /R$, Substituting these expression into equation (1)

$$I_L = \frac{V_{in} - V_1}{R} + \frac{V_o - V_1}{R}$$

$$\therefore \quad V_{in} + V_o - 2V_1 = I_L R$$

$$\therefore \quad V_1 = \frac{V_{in} + V_o - I_L R}{2} \quad \text{-----(2)}$$

Thus we have obtained the expression for V1.

- The OP- AMP is connected in the non- inverting mode. Therefore gain of the circuit is,

$$A_{VF} = 1 + \frac{R}{R} = 2.$$

- The output voltage is given by,

$$V_o = A_{VF} \times V_1 = 2V_1$$

- Substituting V1 from equation (2) we get,

$$V_o = V_{in} + V_o - I_L R$$

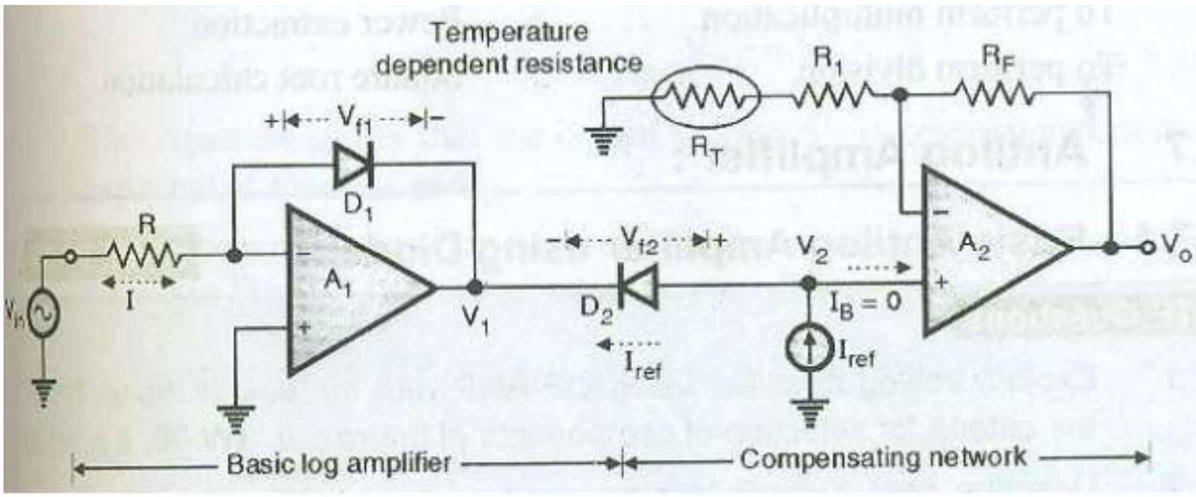
$$\therefore \quad I_L R = V_{in}$$

$$\boxed{\therefore \quad I_L = \frac{V_{in}}{R}} \quad \text{-----(3)}$$

- Equation 3 shows that the load current is dependent on the input voltage and resistor R. Note that all resistors in the figure must be equal in value.

c) Draw temperature compensated log amplifier. State the equation for output voltage 'VO'. 4

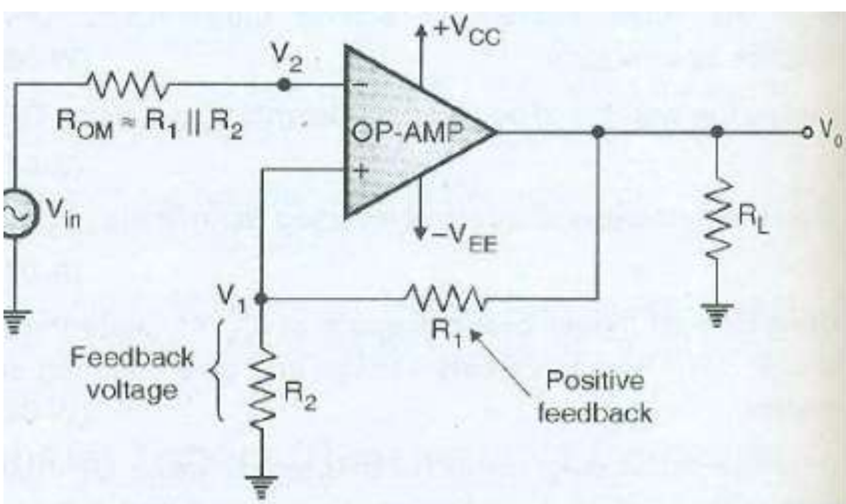
Ans:- (Diagram- 3 mks, Equation- 1 mks



$V_O = - nV_T \log (1 + R_F/R_2+R_T) \log (V_{in}/R_1 * I_R)$

d) Draw circuit diagram of Schmitt trigger using op-amp. 4

Ans:- (Proper relevant diagram- 4mks)



e) Explain antilog amplifier with proper circuit diagram.

Ans:- (Diagram- 2 mks, explanation/derivation 2 marks

$$I_f = I_o e^{V_{in}/\eta V_T}$$ 4

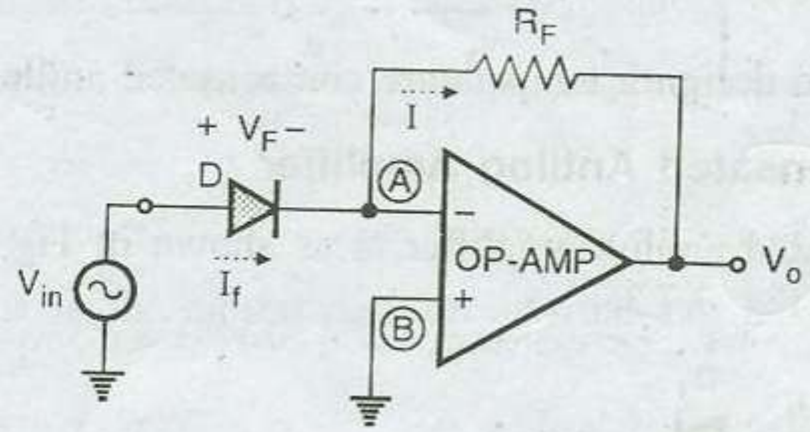


Fig. : Basic antilog amplifier using a diode

Operation: **(2M)**

Note that the diode and resistor in the log amplifier have interchanged their places.

As the non-inverting terminal B has been connected to ground, The inverting terminal A is also connected to the ground potential.

As point A is a virtual ground $V_{in} = V_F$. Therefore the expression for the forward current I_F through the diode is given by

(2M)

- Assuming the input current of the OP-AMP to be zero, the current I flowing through the feedback resistor R_F is given by:

$$I = I_f = -\frac{V_o}{R_F}$$

$$\therefore \quad -\frac{V_o}{R_F} = I_o e^{V_{in}/\eta V_T}$$

$$\therefore \quad V_o = -I_o R_F e^{V_{in}/\eta V_T}$$

- This equation shows that the output voltage Vo is proportional to the exponential function of V_{in}
- The exponential function is same as the antilog.

f) Draw and explain 7V to 12V widow detector.

Ans:- (Diagram – 2 mks, waveform- 1 mks, explanation- 1 mks)

- There is a need to determine when an unknown input is between two precise reference thresholds V_{ut} and V_{lt}.
- This determination can be made by a circuit called the window detector.

The window detector circuit is used for detecting whether an unknown voltage V_{in} falls within a specified voltage band called window. 4

As shown ,the upper trigger point is V_H or V_{UT} which is 12 V while the lower trigger point is V_L or V_{LT} as 7 V , the output will be detected high between these two voltage levels ie 7 V to 12 V.

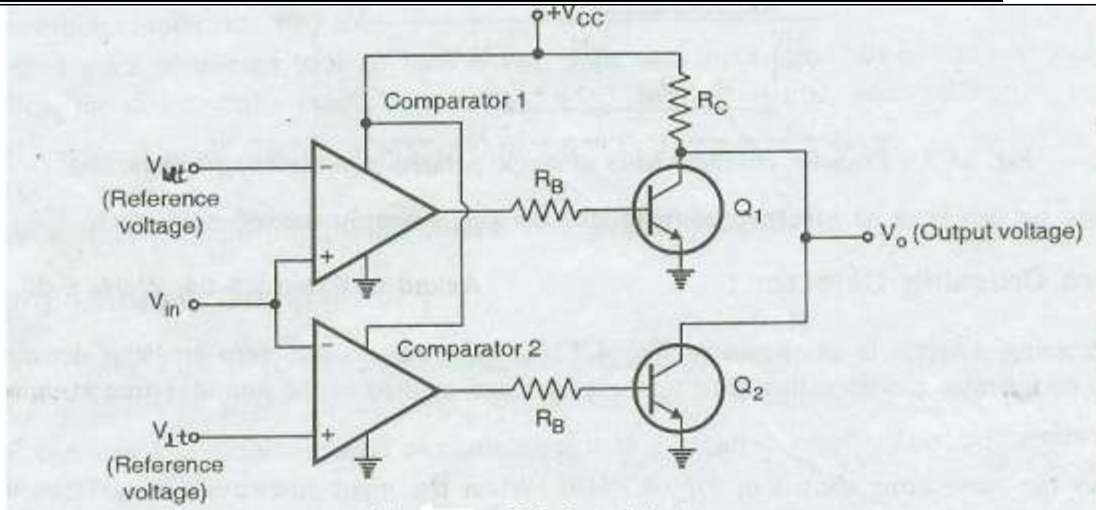
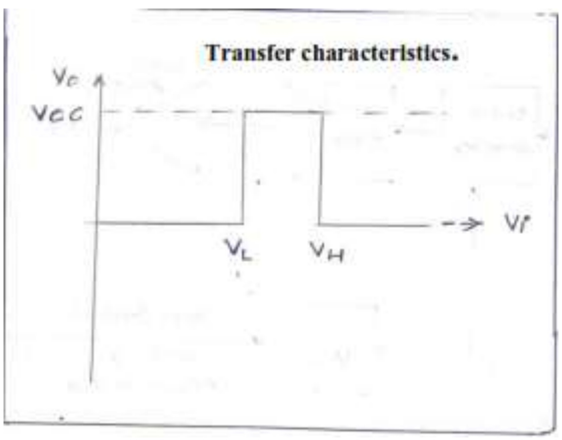


Fig. : Window detector

Here the Reference voltage levels are –

VL= 7 V and VH =12 V



Operation of the circuit: **(2M)**

- V_H and V_L are two references voltages with $V_{ut} > V_{lt}$ an Vin is the input voltage. The outputs of the two comparators are applied to two transistors which operates as switches. The output voltage is obtained at the common collector terminal of the two transistors.
- If V_in is between the two reference voltages i.e. $V_{lt} < V_{in} < V_{ut}$ then the outputs of both the comparators will be low. So both the transistors will remain in OFF state. So the collector voltage i.e. the output voltage will be equal to Vcc.

$$\therefore \quad V_o = +V_{CC} \quad : \text{For } V_{lt} < V_{in} < V_{ut}$$

- If V_{in} is less than V_L then the output of the comparator 1 will be low and that of comparato 2 will be high. This will turn off transistor Q_1 but saturate transistor Q_2 and the output voltage will be $V_{CE\,(sat)}$ i.e. low.

$$\therefore \quad V_o = V_{CE(sat)} = \text{low} \; : \text{For } V_{in} < V_{lt}$$

- If V_{in} is greater than V_H then the output of comparator 1 will be high and that of comparator 2 will be low. Thus transistor Q_1 will saturate and Q_2 will remain off. The output voltage will be $V_{CE\,(sat)}$ i.e. low.

4 **Attempt any <u>FOUR</u> of the following:** 16

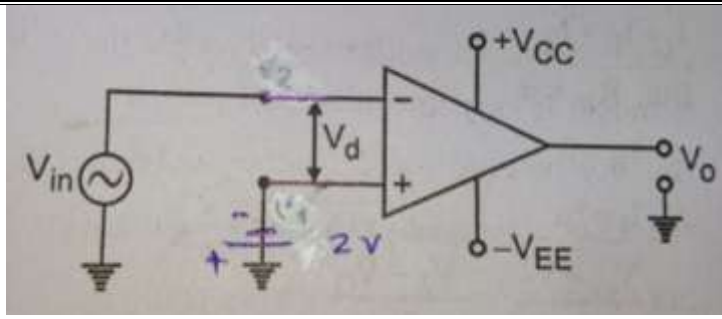
a) Design a comparator to detect -2 volt dc. 4

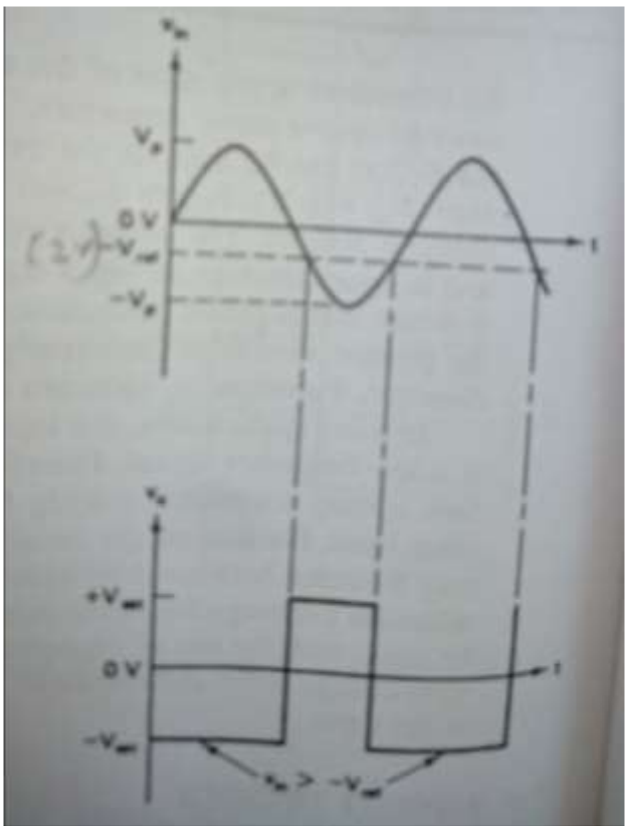
Ans :- (Diagram- 2 mks, Waveforms- 1 mks, explanation – 1 mks)

As shown below to detect -2 V , op-amp works as comparator (either in inverting or noninverting mode) .

The inverting terminal is connected to input signal while the noninverting is at reference voltage=-2 V.

The diagram and waveforms are as shown-





	b)	Design second order low pass filter to get pass band gain 2 and cut off frequency 1 KH_Z. Ans:-Given:- Passband gain Af=2 Cut off frequency F_c = 1Khz	4

Pass band Gain (A_f) is given by the formula

$$A_f = 1 + \frac{R_f}{R_1}$$

Here, $A_f = 2$

Therefore, $2 = 1 + \frac{R_f}{R_1}$

So, $1 = \frac{R_f}{R_1}$

Therefore, $R_f = R_1$

Let $R_f = 10k\Omega$

Therefore, $R_1 = 10k\Omega$

Assume C = 0.01uF

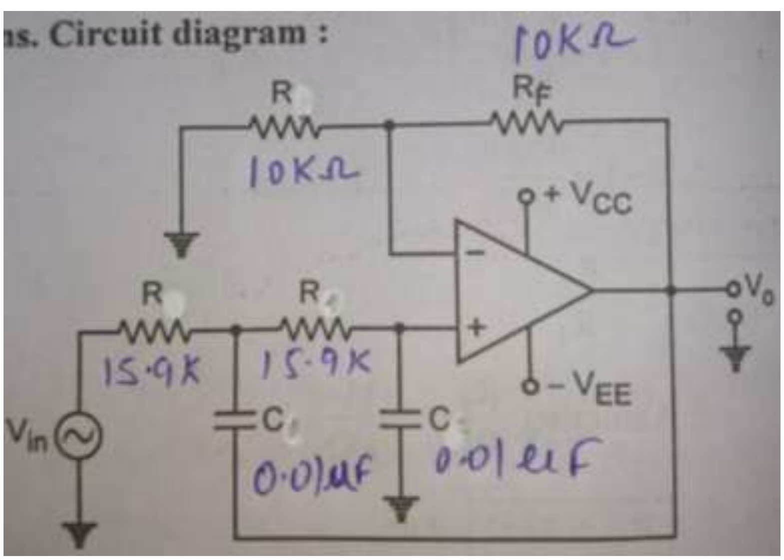
But $f_c = \frac{1}{2\pi RC}$

Given- Fc=1Khz

$1000 = 1/(2*\pi*R*0.01*10^{-6})$

R= 15.91 KΩ

The designed circuit is-



	c)	Design a band reject filter to reject band of 10 KH_Z to 20 KH_Z.	

Ans:-Given-

F_H= 10 KHz and F_L= 20 KHz

Let the gain = 2 | 4

Soln. (a) For high pass filter :

Assuming $\boxed{C = 0.01\,\mu F}$ **Ans.**

$\therefore\ R = \frac{1}{2\pi f_L C}$

$\therefore\ R = \frac{1}{2\pi \times 2 \times 10^4 \times 0.01 \times 10^{-6}}$

$\therefore\ \boxed{R = 79.6\ \Omega}$ **Ans.**

$A_f = 2$

As $A_F = A_{f1} = A_{f2}$

$\therefore\ A_{f1} = 1 + \frac{R_F}{R_1}$

$2 = 1 + \frac{R_F}{R_1}$

$\therefore\ 1 = \frac{R_F}{R_1}$

Let $R_1 = 10\,k\Omega$

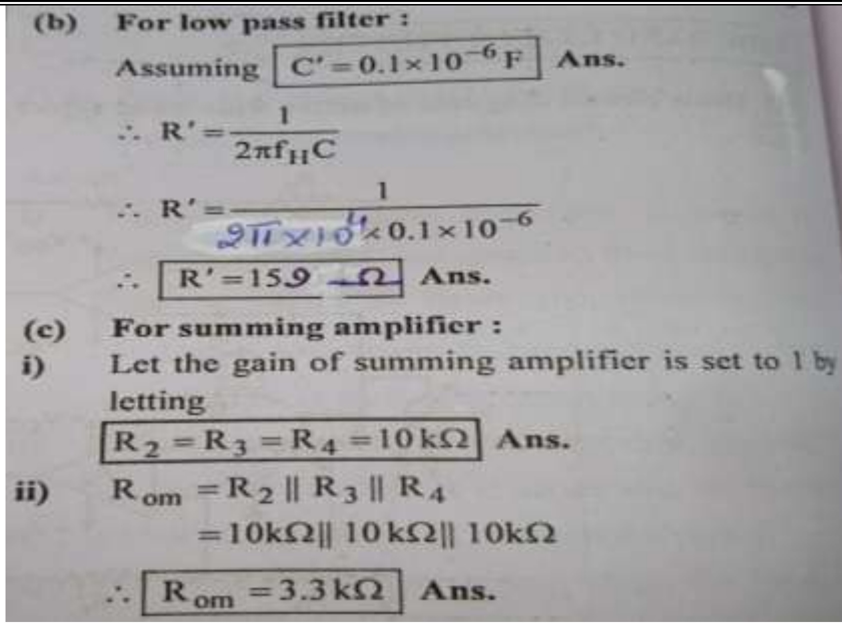
$\therefore\ \boxed{R_F = 10\,k\Omega}$ **Ans.**

$\boxed{R_1 = 10\,k\Omega}$ **Ans.**

As $A_{f2} = A_{f1}$

$\therefore\ \boxed{R_F = R'_F = 10\,k\Omega}$ **Ans.**

$\therefore\ \boxed{R_1 = R'_1 = 10\,k\Omega}$ **Ans.**



(b) **For low pass filter :**

Assuming $\boxed{C' = 0.1 \times 10^{-6} F}$ **Ans.**

$\therefore R' = \frac{1}{2\pi f_H C}$

$\therefore R' = \frac{1}{2\pi \times 10^4 \times 0.1 \times 10^{-6}}$

$\therefore \boxed{R' = 159\ \Omega}$ **Ans.**

(c) **For summing amplifier :**

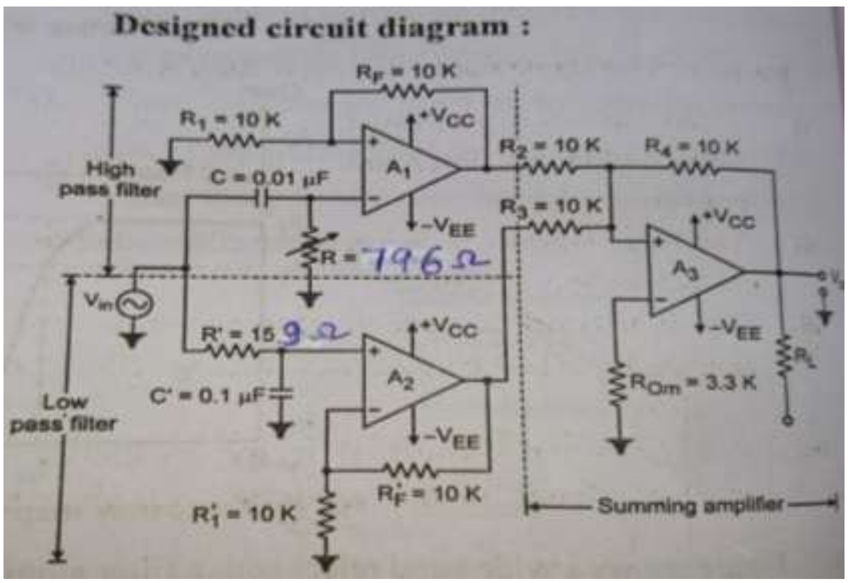
i) Let the gain of summing amplifier is set to 1 by letting

$\boxed{R_2 = R_3 = R_4 = 10 k\Omega}$ **Ans.**

ii) $R_{om} = R_2 \parallel R_3 \parallel R_4$

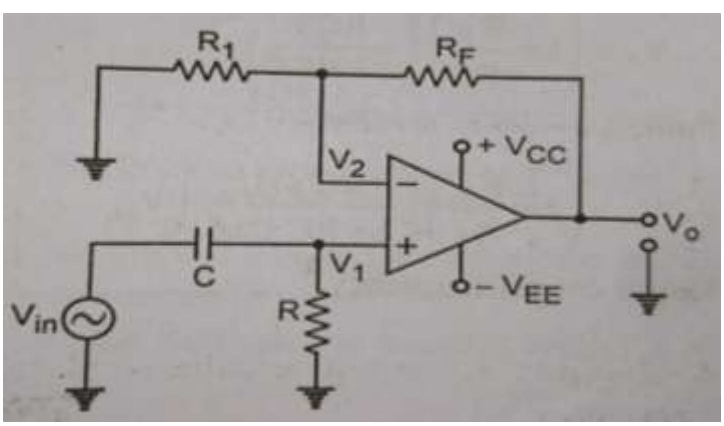
$= 10k\Omega \parallel 10k\Omega \parallel 10k\Omega$

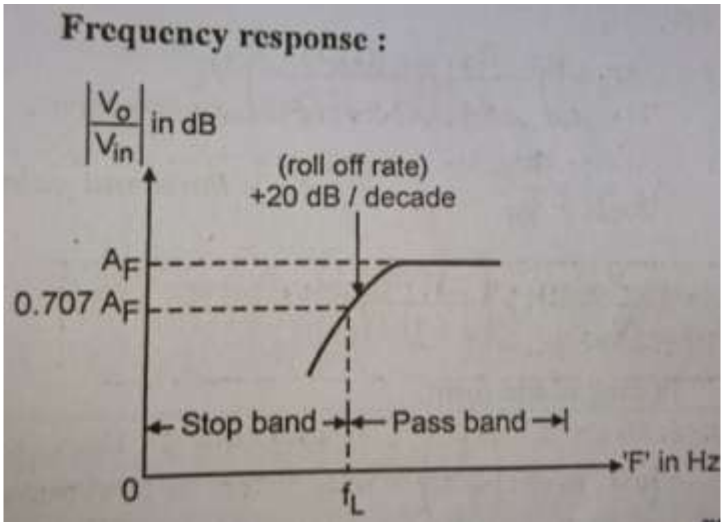
$\therefore \boxed{R_{om} = 3.3 k\Omega}$ **Ans.**

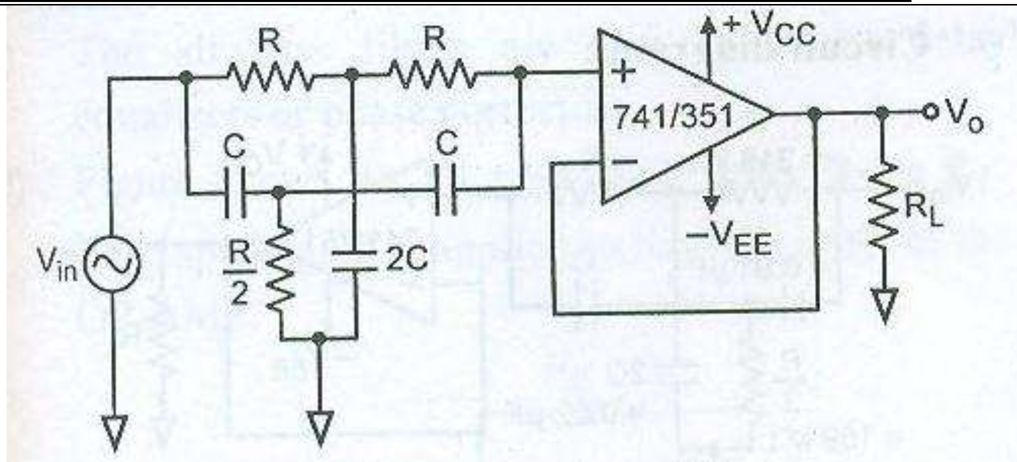


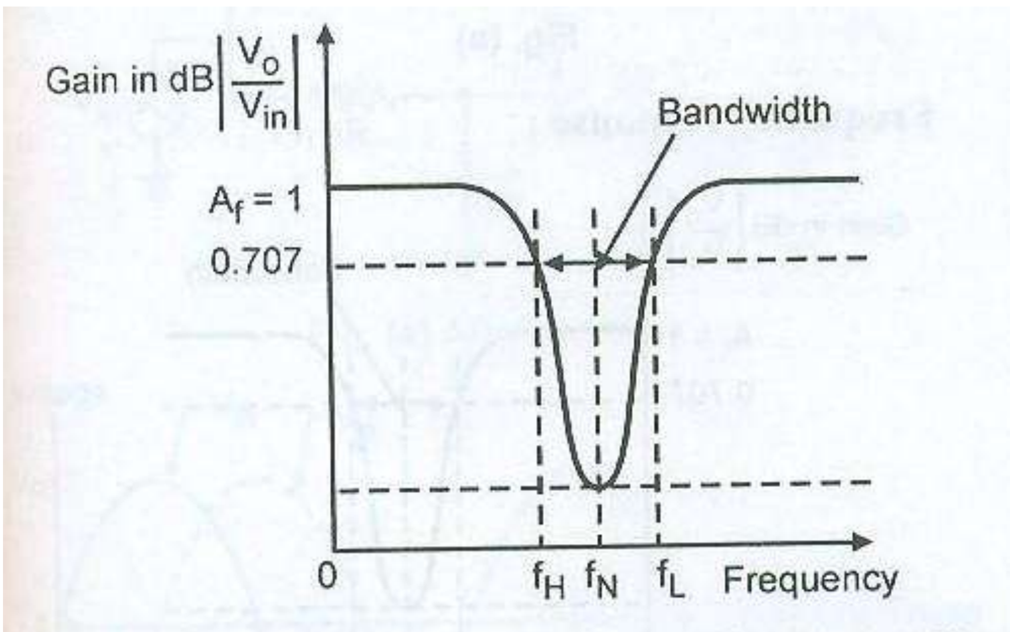
d) Draw high pass filter and explain with characteristics. | 4

Ans:- (Diagram- 2 mks, characteristics- 1 mks, explanation- 1 mks)



		A high pass filter is one that passes the high frequency components and blocks the low frequency at a cut off frequency F_L as shown in the characteristics below. The cut off frequency separates the pass band and the stop band. After F_L, the gain increases at the rate of +20 dB per decade increase in frequency. 	
	e)	Explain how active filter is better than passive filter. Ans:-(Any four relevant points- 4 mks) Advantages of active filters over passive filters 1. Active filters have flexibility in gain and frequency adjustments 2. They provide pass band gain 3. Because of high input resistance and low output resistance ,they donot have loading problems 4. The components required for active filters are of smaller size 5. They donot exhibit any insertion loss 6. Due to absence of inductors and easy availability of variety of cheaper op-amps active filters are cheaper 7. They allow for interstage isolation and control of input and output impedance	4
	f)	Draw notch filter. Explain with characteristics. Ans:- (Diagram – 2 mks, characteristics- 1 mks, explanation- 1 mks)	4





Characteristics-As seen from the characteristics-The notch filter has very narrow band rejection which depends on the value of Quality factor Q. Higher the value of Q, narrower is the band rejection .

The Notch out frequency is the frequency at which maximum attenuation occurs. It is given by

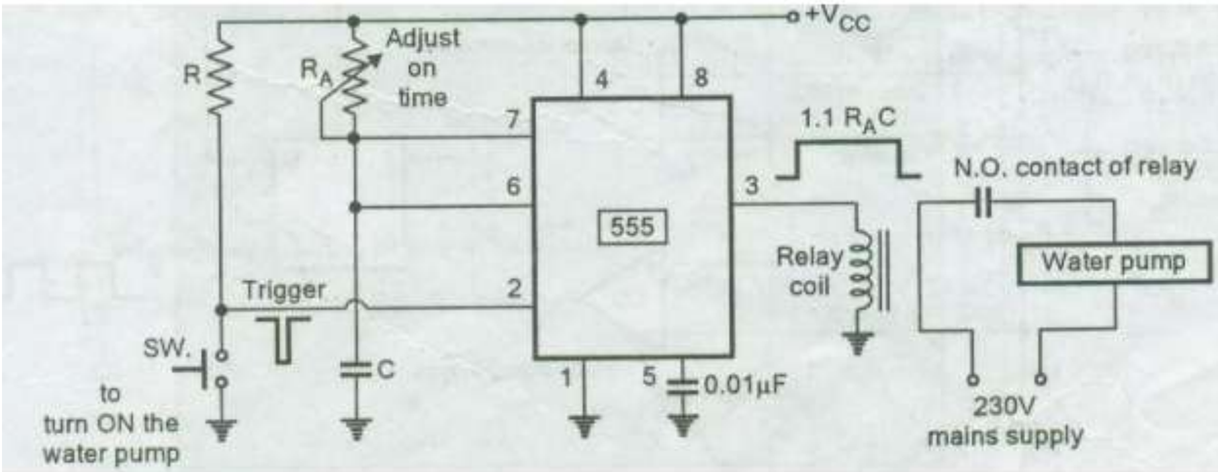
$$F_N = \frac{1}{2\pi RC}$$

Q > 10 narrow band reject filter.

5 **Attempt any <u>FOUR</u> of the following** 16

a) Draw circuit diagram of IC555 as water level controller. Explain its working. 4

Ans:- (Diagram- 2 mks, explanation- 2 mks)



Explanation-

- IC 555 is used in the monostable multivibrator mode.
- "SW" is a push to ON switch is used to turn on the timer and the water pump motor.
- As soon as SW is switched this is used to turn on the timer and the water pump motor. IC 555, and output of 555 goes high.
- It will remain high for period of $T_{on} = 1.1\ R_AC$. The high output of IC 555 will energize the relay coil, and close the N.O (normally open) contact of the relay to connect the 230 V ac supply to the water pump motor.
- The pump motor will start and the water will be pumped into the overhead tank.
- The motor will remain on for the ON time of the monostable circuit.

  $T_{on} = 1.1\ R_AC$
- The on time can be adjusted as per requirement by varying the resistance R_A.

b) Design AMV for 10 KH_Z frequency and 60% duty cycle. 4

Ans:-(solving for components and designed circuit- 4 mks)

Given- Duty cycle D= 60%

Frequency F= 10 KHz

5

Soln. Time period $T = \frac{1}{f} = \frac{1}{10\text{kHz}} = 0.1\ \text{msec}$

$T = 1\text{ms}$

Now, duty cycle $D = \frac{T_{ON}}{T} \times 100 = 60$

$T_{ON} = \frac{D \times T}{100}$

$= \frac{60 \times 0.1\text{ms}}{100} = 0.06\ \text{ms}$

$T_{ON} = 0.06\ \text{msec}$

Also $T = T_{ON} + T_{OFF}$

$T_{OFF} = T - T_{ON} = 0.1 - 0.06 = 0.04\ \text{msec}$

We know, $T_{OFF} = 0.693\, R_B \times C$

Assuming, $C = 0.1\,\mu F$

$R_B = \frac{T_{OFF}}{0.693 \times C}$

$R_B = \frac{0.04 \times 10^{-3}}{0.693 \times 0.1 \times 10^{-6}} = 577\,\Omega$

Also

$T_{ON} = 0.693(RA+RB)*C$

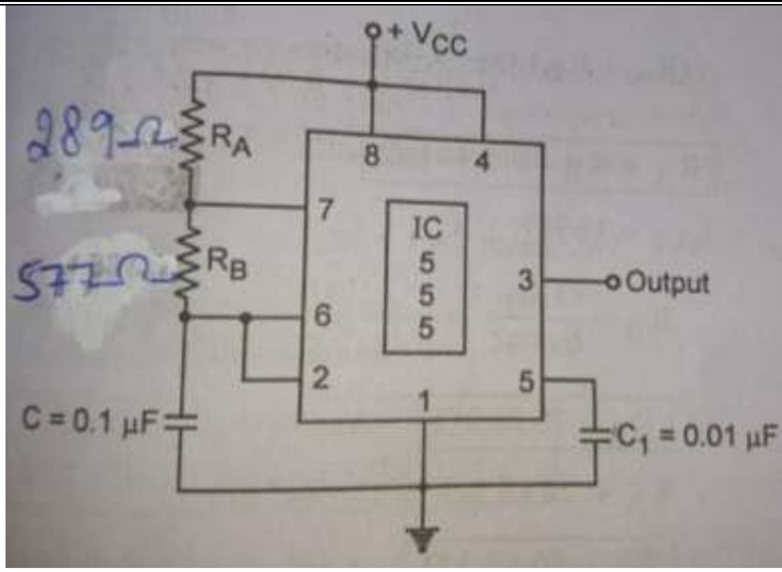
TON= 0.693RA*C+0.693 RB*C

0.06msec= 0.693 RA*C+ 0.04 msec

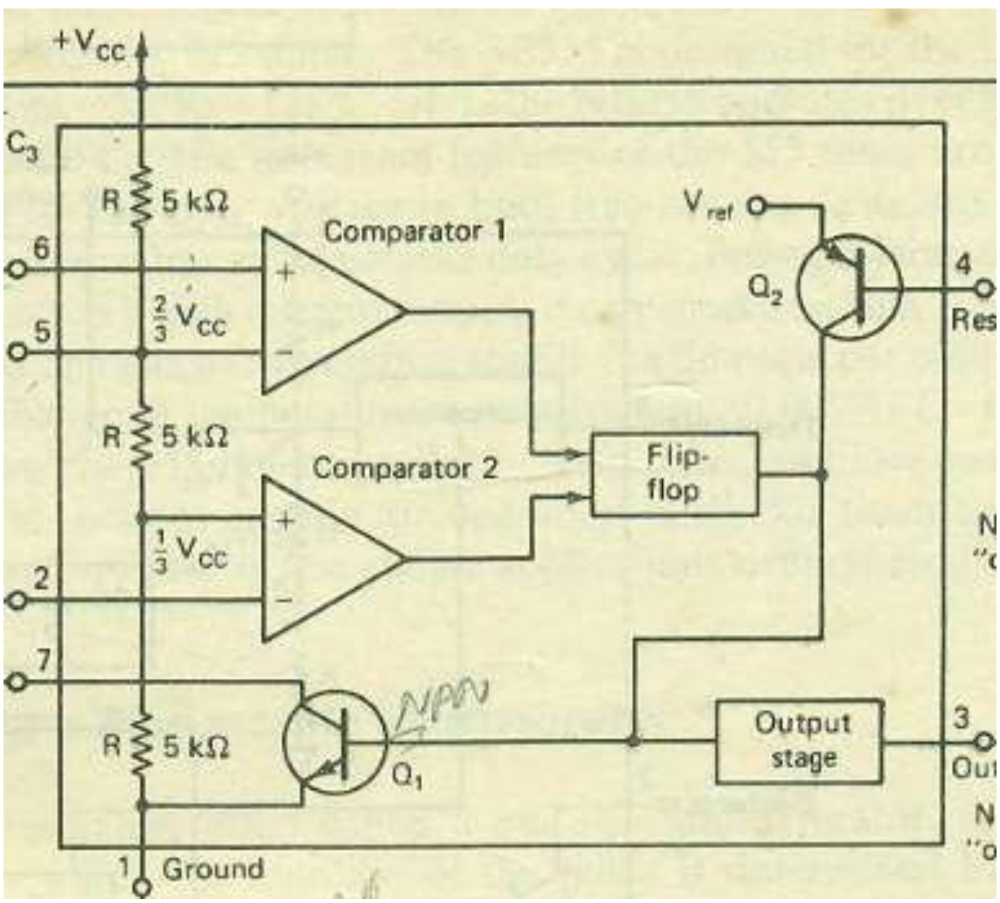
Solving

RA= 289 Ω

So the designed circuit is as shown-



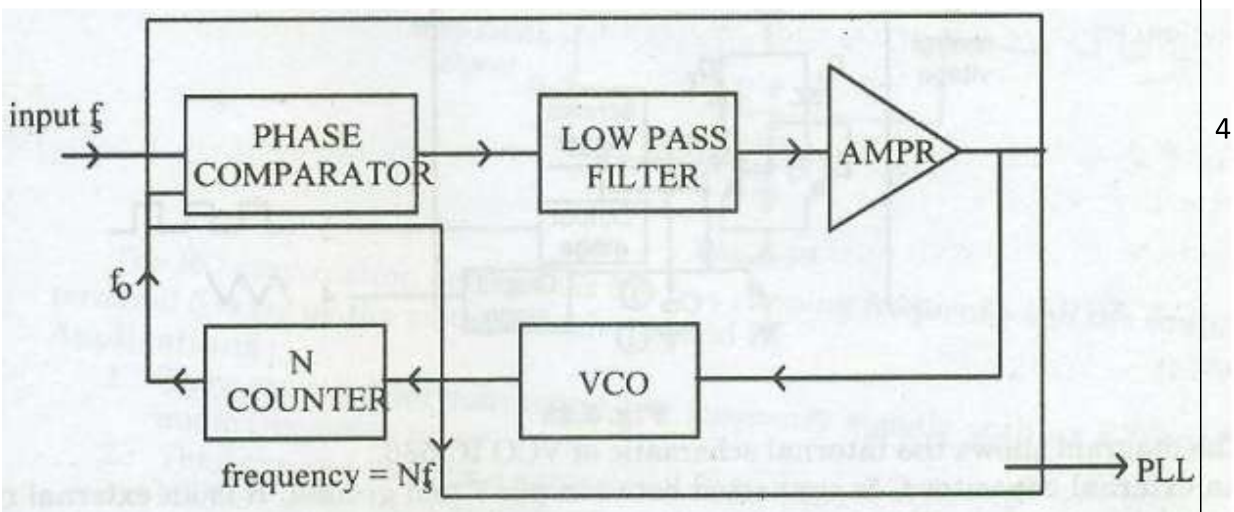
c) Draw block diagram at IC 555. Explain the use of pin 2 and 6. 4



Function of pins –

2- Trigger:- The o/p of timer depends on the external trigger pulse applied to this pin. When

		a trigger pulse of amplitude > 1/3 VCC is applied to this pin , o/p of timer changes from low to high 6- Threshold:- When a trigger pulse of amplitude > 2/3 VCC is applied to this pin , o/p of timer changes from high to low.	
	d)	Explain operation of PLL as multiplier. Ans:-(Diagram- 2 mks, explanation- 2 mks)	4

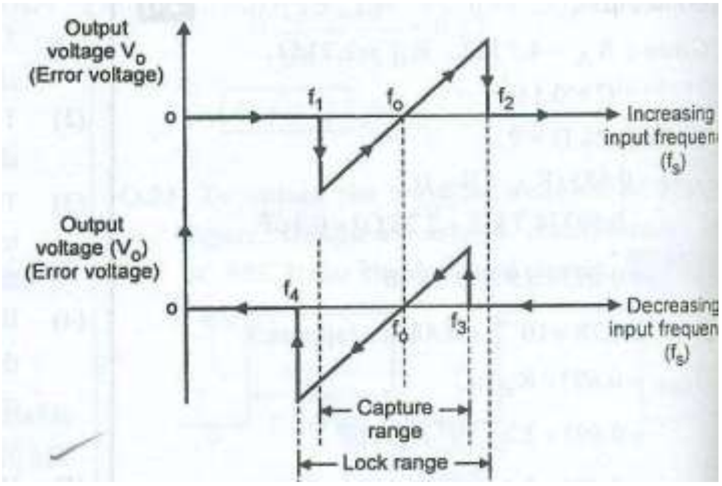


- A divide by N network whose scaling factor can be externally programmed is inserted between the VCO and the phase comparator.
- When the system is in lock, the two inputs to phase comparator are at the same frequency. At this condition, the VCO frequency is given by Nf_s is the incoming frequency.
- Thus, the VCO output frequency is a multiple of the input frequency.
- The multiplying factor being governed by scaling factor of the divide N counter.

	e)	Explain the operation of VCO (Voltage Controlled Oscillator) block in IC 565. Ans:- (only operation/ function – 4 mks) **Role of Voltage controlled oscillator (VCO):** The control voltage V_C is applied at the input of a VCO The output frequency of VCO is directly proportional to the dc control voltage V_C. The VCO frequency F_O is compared with the input frequency F_S by the phase detector and it (VCO frequency) is adjusted continuously until it is equal to the input frequency F_S i.e. $F_O=F_S$.	4
	f)	Draw PLL transfer curve. Explain (i) Capture range	4

(ii) Lock range

Ans:- (Transfer curve- 2 ks, explanation- 1 mks each)



Lock range: the range of frequencies over which the PLL can maintain the phase lock with the incoming signal Fs, is defined as the lock in range.

Lock range = $f_L - 2\,\Delta f_L$

Where $f_L = 8 f_0 / V$

Capture range : it is defined as the range of frequencies over which the PLL can acquire lock with the input signal Fs

Capture range = $2\,\Delta f_c$

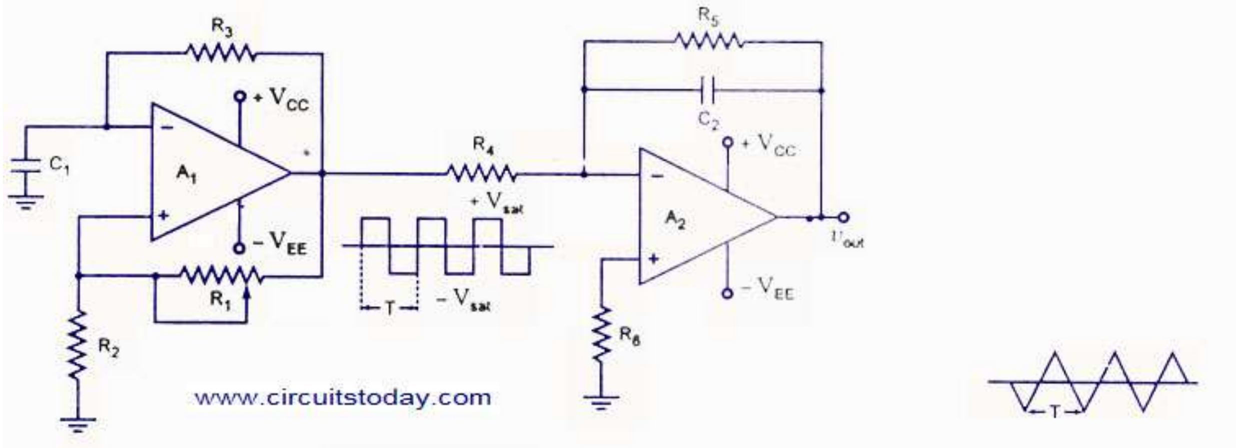
Where $f_c = f_L / (2\pi * 3.6 * 10^3 * C)$

6 **Attempt any FOUR of the following:** 16

a) Draw triangular wave generator. Draw its waveform of it.

Ans:- (diagram along with waveforms -2 mks each) 4

As shown a Schmitt trigger circuit(or comparator) as square wave generator followed integrator provides generation of triangular waveforms.



(a) Basic Circuit

(b) Output Waveform

Triangular Waveform Generator

b) Give advantages and disadvantages of wein bridge oscillator. 4

Ans:- Advantages-(any two- 2mks)

1) Suitable for low frequency oscillations

2) simple circuit and frequency can be easily adjusted.

Disadvantages (any two – 2 mks)

1) Not suitable for high frequency applications

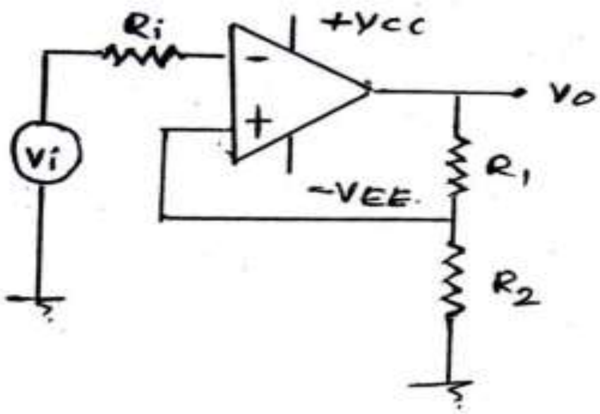
2) Problem of frequency unstability.

c) Explain working of square wave generator using op-amp, with proper circuit. 4

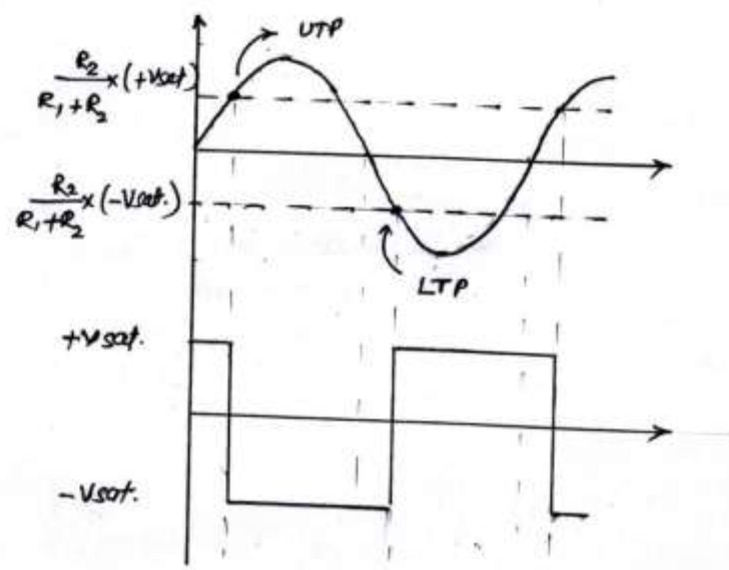
Ans:- (diagram – 2mks, waveforms- 1 mks, explanation- 1 mks)

Schmitt trigger circuit is one which converts any waveform into square wave.

(any other square waveform circuit can be explained here)



Waveform:-



Explanation-

Figure shows an inverting comparator with positive feedback. The circuit converts an irregular shaped waveform to a square wave or pulse. This circuit is known as Schmitt trigger.

The input voltage triggers the output, every time it exceeds certain voltage level called upper threshold voltage V_{ut} and lower threshold voltage V_{lt}.

The threshold voltage is obtained by the divider circuit $R_1 - R_2$. The voltage across R_1 is variable reference threshold voltage, that depends on the value and polarity of the output voltage V_o.

When $V_o = +V_{sat}$ the voltage across R_1 is called the upper threshold voltage V_{ut}. The input V_{in} is greater than V_{lt} and this causes V_o to switch from $+V_{sat}$ to $-V_{sat}$. As long as

$V_{in} < V_{ut,}$ V_0 is $+V_{sat}$ and

$$V_{ut} = \frac{R_1}{R_1 + R_2}(+V_{sat})$$

On the other hand, when $V_o = -V_{sat}$, the voltage across R_1 is referred to as lower threshold voltage V_{lt}. V_{in} must be slightly more negative than V_{lt} in order to cause V_o to switch from $-V_{sat}$ to $+V_{sat}$. Hence for $V_{in} > V_{lt}$, $V_o = -V_{sat}$ and

$$V_{lt} = \frac{R_1}{R_1 + R_2}(-V_{sat})$$

Thus, if the threshold voltage V_{ut} and V_{lt} are made larger than the input voltages, the positive feedback will eliminate the false output transition. Also, the positive feedback, because of its regenerative action, will make V_o switch faster between $+V_{sat}$ and $-V_{sat}$ and $ROM = R_1 \| R_2$ compensate the offset voltage.

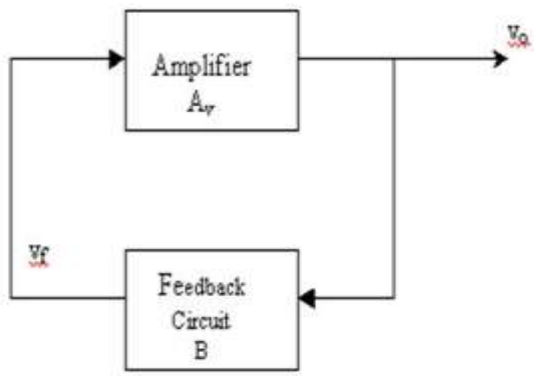
d) Explain principle of oscillator with block diagram.

Ans:- (Block diagram- 2 mks, explanation- 2 mks)

An electronic **oscillator** is an electronic circuit that produces a periodic, oscillating electronic signal, often a sine wave or a square wave. **Oscillators** convert direct current (DC) from a power supply to an alternating current (AC) signal and works with positive feedback principle.

An oscillator is a type of feedback amplifier in which part of the output is fed back to the input via a feedback circuit. If the signal fed back is of proper magnitude and phase, the circuit produces alternating currents or voltages. 4

$$\frac{v_o}{v_i} = \frac{A_v}{1 - A_v B}$$



$v_{in} = 0$ and v_o ∗ 0 implies that

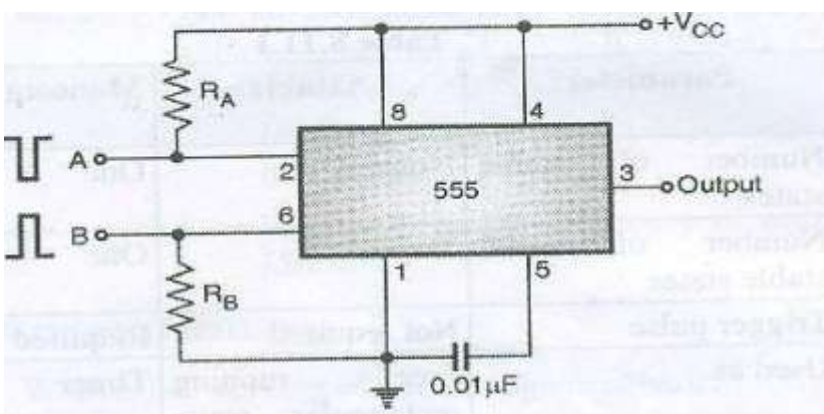
- $A_v B = 1$
- Expressed in polar form,
- $A_v B = 1$ ∗ 0^0

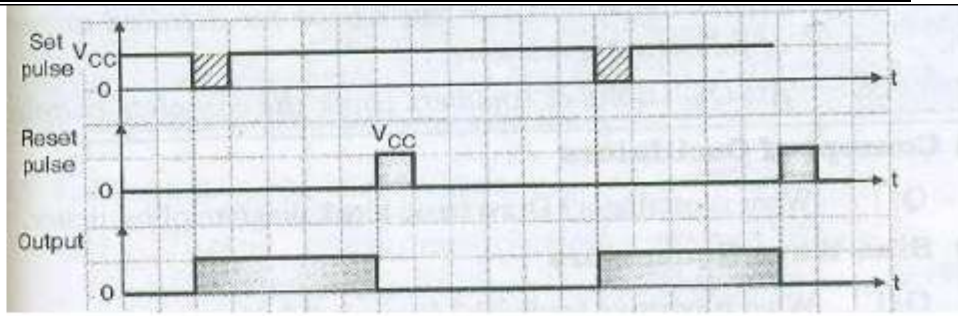
In order to satisfy the above criterion, the oscillator must be able to achieve positive feedback at some frequency w_0 where the magnitude of the loop gain is exactly unity. <**Barkhausen Criterion**>

e) Draw and explain bistable multi-vibrator.

Ans:- (bistable multivibrator can be explained using op-amp or timer IC 555)

(Diagram – 2 mks, waveforms – 1 mks, explanation - 1mks) 4





Operation- The IC 555 also provides a direct relay driving capability. In the figure, the negative pulses are applied to the trigger input that sets the flip flop. The output goes high with the positive pulse applied to the threshold resets the flip flop and the output goes low. Thus with the help of trigger, the output is forced to go from one stable state to the other.

f) Explain working of monostable multivibrator using op-amp. 4

Ans:- (diagram- 2 mks, waveforms- 1 mks, explanation- 1 mks)

Op-amp Monostable Multivibrator (one-shot multivibrator) circuits switching circuits that have only one stable state, producing an output pulse of a specified duration T. An external trigger signal is applied for it to change state and after a set period of time, either in microseconds, milliseconds or seconds, a time period which is determined by RC components, the monostable circuit then returns back to its original stable state were it remains until the next trigger input signal arrives.