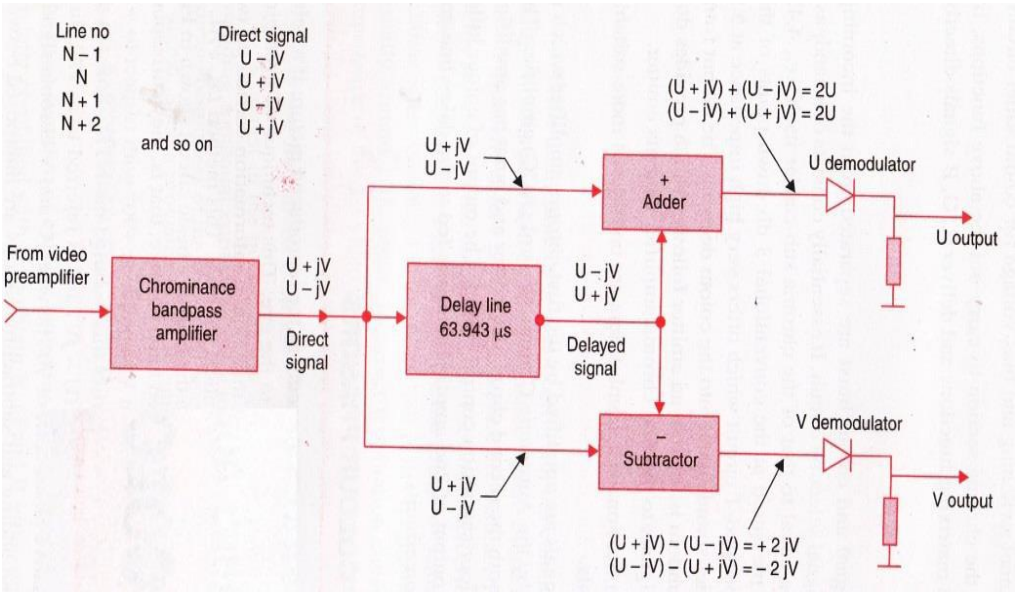
MODEL ANSWER

WINTER– 17 EXAMINATION

Subject Title: T V Receiver Subject Code: 17547

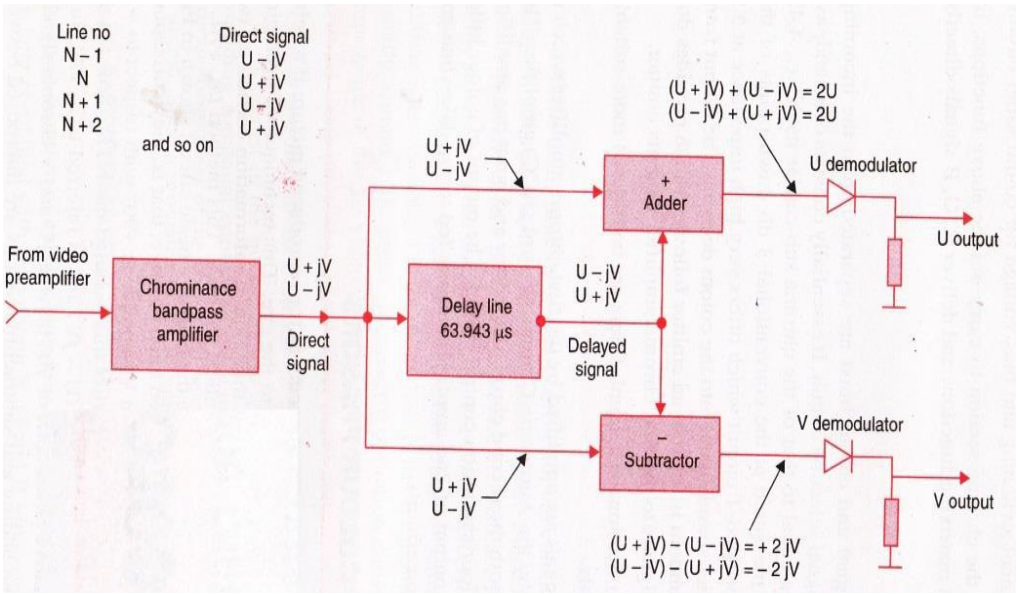
Important Instructions to examiners:

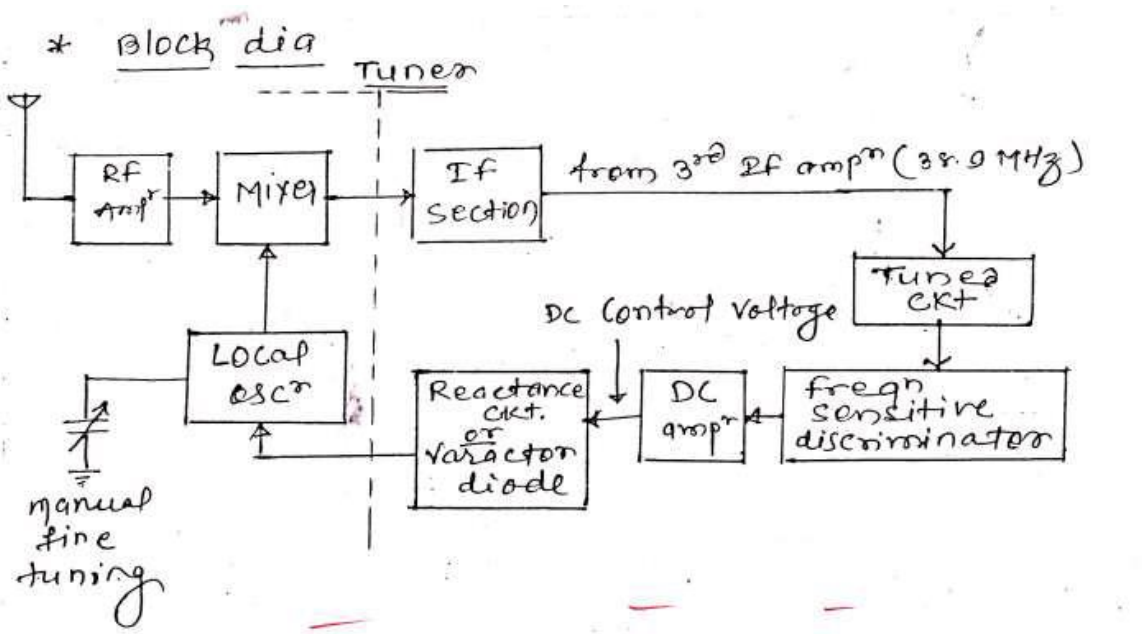
1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q.N.	Answer	Marking Scheme
Q.1 A)		**Attempt any three**	12-Total Marks
	a)	**Describe generation of U and V signals in TV Receiver.**	4M
	Ans:	**Diagram-** 	2M

Explanation:-

- A delay line and adding and subtracting circuits are interposed between the chrominance amplifier and demodulators.

		• The object of delay line is to delay the chrominance signal by almost one line period of 64us. • The chrominance amplifier feeds the chrominance signal to the adder, the subtracter and the delay line. • The delay line in turn feeds its output to both the adder and subtracter circuit. • The adder and the subtracter circuits, therefore, receive the two signals simultaneously. These may be referred to any given time as the direct line and delay line signals. • The adder yields a signal consisting of U information only but with twice amplitude (2U) • Similarly, the subtraction circuit produces a signal consisting only of V information, with an amplitude twice that of the 'V' modulation product.	**2M**
b)		**State necessity of adder and subtracter circuit in PAL –D decoder.**	**4M**
Ans:		**<u>Necessity of adder and substracter circuit:</u>**  • The adder and the subtracter received the two signals to any given time as the direct line and delay line signals. • Adder adds (U+jv)+(U-jv) or (U-jv)+(U+jv) signal to get 2U and after demodulation to getting U signal. • Substracter subtract U+jv)-(U-jv) or (U-jv)-(U+jv) signal to get 2V and after demodulation to getting V signal.	**2M** **2M**
c)		**Why micro controller is used in TV Receiver.**	**4M**
Ans:		**<u>Use of microcontroller in TV reciver.</u>** • Auto seek programming • Manual programming • Digital 'LED' display of the selected channel • Operation with or without remote control	**(Any 4 point- 1/2 M Each)**

	• AFT control and • Audio mute during channel hunting.	
d)	**With neat block diagram explain working of AFT in colour TV .**	**4M**
Ans:	**Diagram-**  * Block dia Tuner RF Ampr Mixer IF section from 3rd IF amp^{n} (38.9 MHz) Tuned ckt DC Control Voltage Local oscr Reactance ckt. or varactor diode DC ampr freqn sensitive discriminator manual fine tuning **Explaination-** The AFT circuit is actually automatic frequency control (AFC) on the local oscillator in the tuner. This control aims at obtaining a picture IF frequency of exactly 38.9MHz at the converter output. To achieve this, the IF frequency is obtained from the IF amplifier section is measured by a discriminator that forms part of the AFT control circuit. **Frequency sensitive Discriminator :-** Its output is a DC correction voltage that indicates deviation of IF frequency from its exact value of 38.9MHz. since this frequency depends on the oscillator input to the mixer, the AFT voltage indicates error in the local oscillator frequency. The AFT control voltage is zero at balance i.e. when the IF frequency is exactly 38.9MHz for frequency deviations on either side of 38.9MHz, the net dc correcting voltage is either positive or negative depending on whether the frequency is above or below the correct value. **Reactance circuit or Varactor diode:** The DC control voltage thus developed is applied to a reactance circuit or to a varactor diode that forms part of the local oscillator tank circuit. The junction capacitance of the varactor diode varies with the applied dc control voltage and thus changes resonant frequency of the oscillator tuned circuit to shift the frequency to its correct value.	**2M** **2M**
B)	**Attempt any one:**	**6M**
a)	**What is meant by auto strereoscope method of 3D TV? Write its one advantages. Name the different methods and describe any one.**	**6M**
Ans:	**Auto stereoscopic Method in 3DTV:-**	**1M**

Auto stereoscopic is a method of displaying stereoscopic images (adding binocular perception of 3D depth) without the use of glasses on the part of the viewer, it is also called "glasses-
free 3D" or "glasses-less 3D" system

Advantage:-

- No need to were glasses to observe 3 D picture **½ M**

Methods:

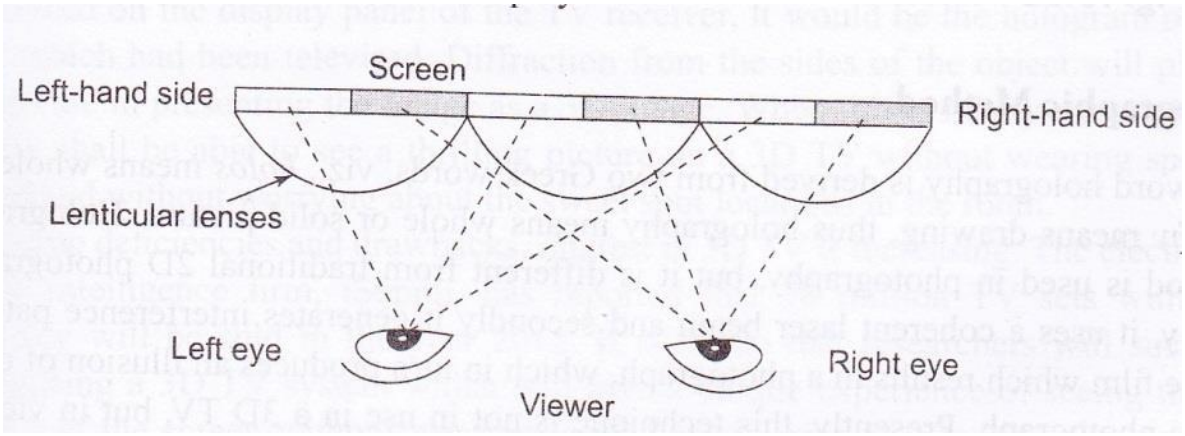
- Lenticular method
- Parallax method **1.5M**
- Holographic method

Explanation:-

Note: Any one method is to be considered

i) Lenticular Method:-

Diagram:-



1.5M

Explanation:-

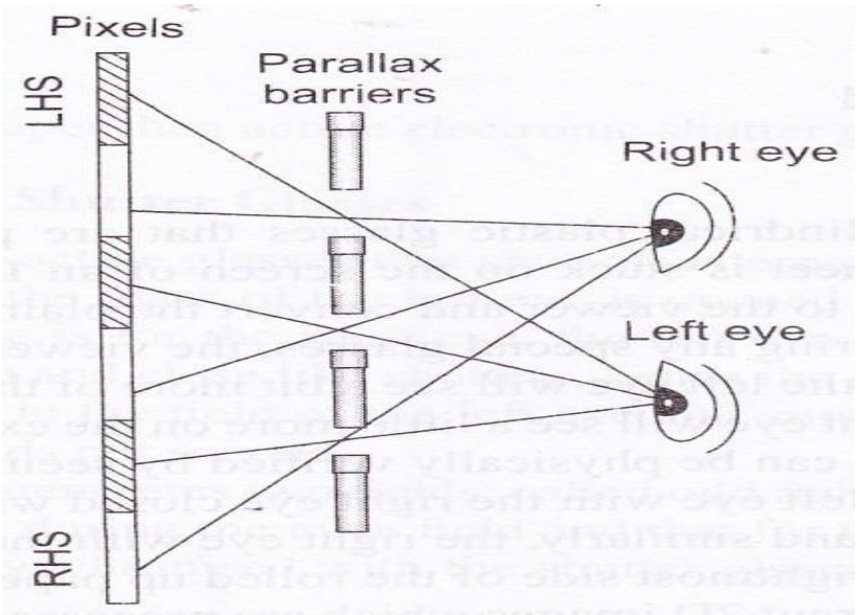
Lenticular lenses are cylindrical plastic glasses that are pasted in an array on a transparent sheet. **1.5M**

- Thus sheet is struck on the screen of an LCD TV. The cylindrical lenses magnify the image to the viewer and convert the plain image into a cylindrical image.
- Now, without wearing any special glasses, the viewer's two eyes will see two slightly different images. The left eye will see a bit more of the display on the extreme left hand side, and the right eye will see a little more on the extreme right – hand side as shown in fig.
- This method gives a good quality 3D view of the image, the view is greatly dependent on the position when the viewer is sitting.

OR

ii)Parallax Barrier:-

Diagram:-

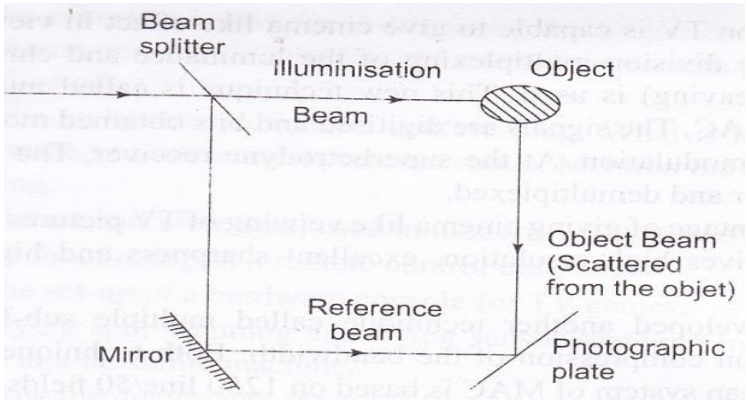


- The Parallax barrier is a fine grating of liquid crystal with slits in it. When placed over a screen, the slits corresponds to certain column of pixels on the TV's screen.
- When a small voltage is applied to the parallax barrier, the slitted grating allows two slightly different images to reach the left and the right eye, as shown in the fig. the brain processes these two images to produce 3D images.
- The parallax barrier can be switched on and off easily, allowing the TV to be used as a traditional 2D or A new 3D set. While it offers good quality contents, it is sensitive to the position of the viewer, resulting in well-defined sweet spot . This aspect hampers its general acceptability.

OR

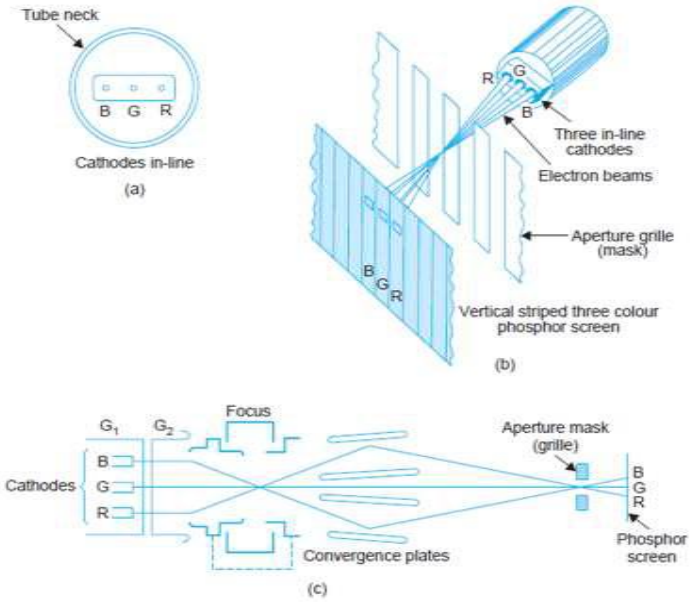
iii) Holographic Method:-

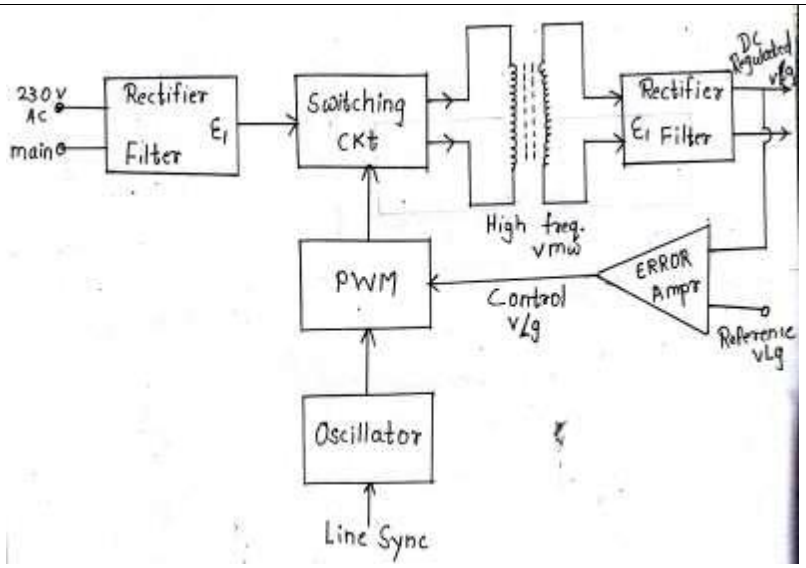
Diagram:-



- A laser beam from a suitable source, say an LED is split into two beams by a prism or a special mirror one beam goes to the object and is scattered from innumerable points of the object and reaches the film.
- The other beam from the splitter goes directly to the film without encountering the object. This is called "reference beam."
- As all the points of the object are not equidistant from the film, the scattered beam coming from non-equidistant point will have phase difference with respect to the reference beam from some point it would be in phase while from some other points out of phase.
- The phase, and weakening when they meet in an opposite phase. The interference pattern so obtained will produce the effect of depth. This is how holograms are prepared
- In case of TV, a 3D image will be registered on the surface of the target plate of the TV Camera by using holographic techniques.
- When this image is transmitted and reproduced on the display panel of the Tv receiver, it would be the hologram of the scene which this image is transmitted and reproduced on the display panel of the TV receiver, it would be the hologram of the scene which had been televised

b)	**Draw construction of trinitron picture tube and describe its working.**	**6M**
Ans:		

		Diagram:  (a) gun structure(b) electron beams, vertical-striped three colour phosphor screen (c) constructional, focus and convergence details **Explanation:** • The Trinitron or three in-line cathodes color picture tube was developed by 'SONY' Corporation of Japan around 1970. It employs a single gun having three in-line cathodes. This simplifies constructional problems since only one electron gun assembly is to be accommodated. • The three phosphor triads are arranged in vertical strips as in the P.I.L. tube. Each strip is only a few thousandth of a centimeter wide. A metal aperture grille like mask is provided very close to the screen. • It has one vertical slot for each phosphor triad. The grille is easy to manufacture and has greater electron transparency as compared to both delta-gun and P.I.L. tubes. The beam and mask structure, together with constructional and focusing details of the Trinitron are shown in Fig. • The three beams are bent by an electrostatic lens system and appear to emerge from the same point in the lens assembly. Since the beams have a common focus plane a sharper image is obtained with good focus over the entire picture area. All this simplifies convergence problems and fewer adjustments are necessary.	**3M.** **3M**
Q 2		**Attempt any four :**	**16M**
	a)	**Draw block diagram of SMPS . State the function of each block.**	**4M**
	Ans:	**Diagram-**	



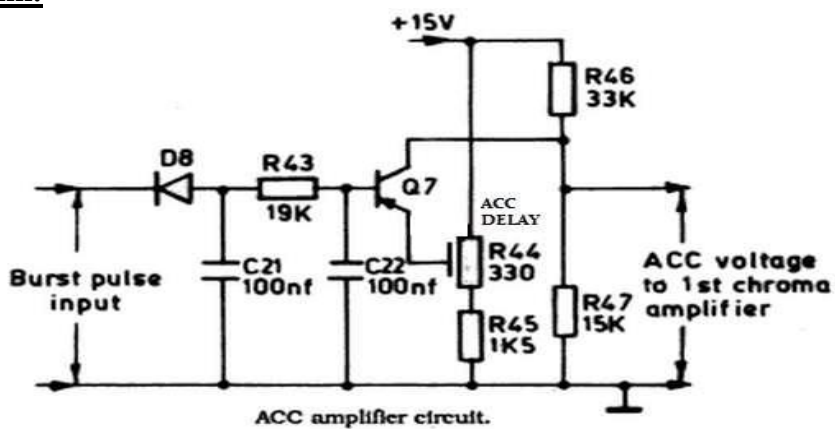
2M

SMPS is the non dissipative regulator which operates by chopping the regulated DC supply voltage, at high frequency 15,625KHZ by using switching transistors. And when filtered by high voltage rectifier and capacitors.

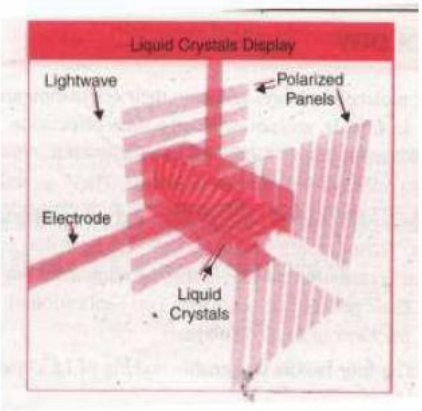
Working:-

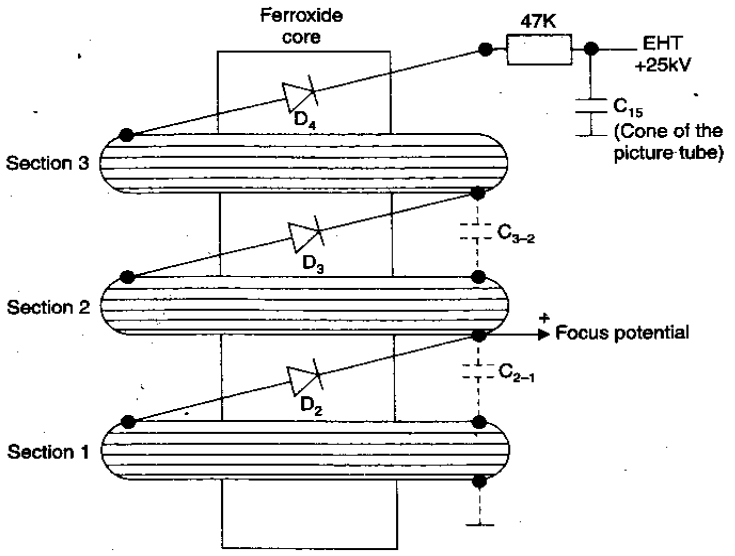
1. The unregulated DC voltage is applied to the switching circuit .
2. The switching circuit consist of a transistor driven by pulse width modulation(PWM). It chops the input DC voltage at the high frequency.
3. The chop DC voltage is applied to the rectifier circuit through the high frequency transformer.
4. The transformer may be step up or step down or coupling transformer.
5. The amplifier samples the input voltage & controls the pulse width of the PWM.
6. The PWM in turn controls the switching time of transistor & proportionally varies the outputvoltage.

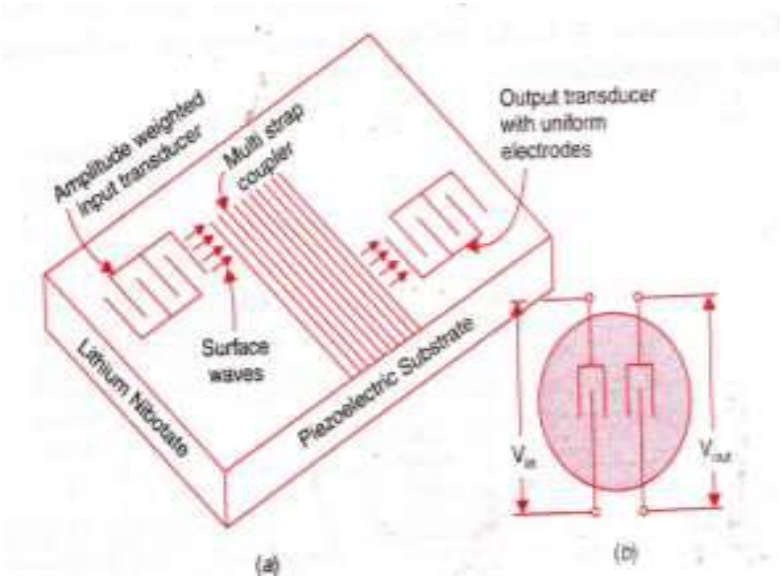
2M

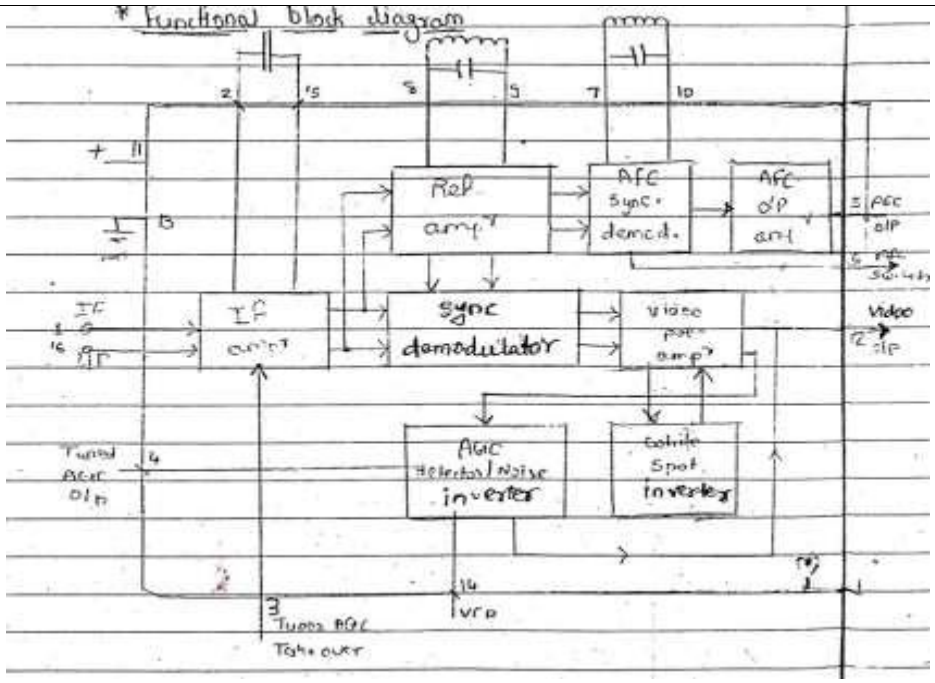
b)	**Draw ckt. Diagram of ACC amplifier and describe its working.**	**4M**
Ans:	• The amplified burst signal that become available at the output of gated burst amplifier is also fed to diode D8 of the automatic colour control amplifier circuit as shown in fig. **Diagram:**  ACC amplifier circuit.	**2M**

		Explanation: • The diode together with filter (C21, R43, and C22) acts as a HWR-cum-filter to develop a negative going dc voltage at the base of Q7, which is proportional to the strength of received signal. • As stated C21, R43 & C22 from a LPF to smooth any 4.43MHz variations present in the rectified signal. The output voltage at the collector of transistor Q7 is a positive voltage which increases or decreases with the strength of Chroma signal. • This positive voltage is typically 7V under normal signal strength conditions. The resistor R44 provides an adjustable reverse bias for Q7 to delay its conduction until the Chroma signal exceeds a given threshold. • The potentiometer formed by resistors R46 & R47 is used to obtain correct steady bias for the first Chroma amplifier. It is also necessary for making the collector of transistor Q7, negative w.r.t. its emitter.	**2M**
	c)	**State purpose of remote control system in TV. Write its advantages and disadvantages(any two of each).**	**4M**
	Ans:	***Note:-(Any other relevant advantages and disadvantages should be considered)*** **Explanation:** Based on the design of the remote control unit and type and make of the receiver, it is possible to control as many as five different functions. These include volume-up and on-off, volume-down, channel selection, color-up, color-down etc. Though a variety of remote control television system are in use. **Advantages:** • Audio muting option is available. • TV can be programmed by remote control system. • User can make their own set of selected channels. **Disadvantages:** • It requires line of site. • Range of IR sensor is less compared to any other wireless communication components. • Latest Tv do not have power on/OFF button on the Tv so if remote is faulty Tv cannot be stay off condition means it goes in standby mode which ultimately cause loss of power.	**(2M for Purpose,1M Advantage and 1M disadvantage)**
	d)	**List any eight major control available in plasma TV. State function of any two controls.**	**4M**
		Controls available in plasma TV (ANY EIGHT) i. Change viewing modes ii. Use picture-in-picture (PIP) mode iii. Use picture-on-picture (POP) mode iv. Change plasma TV tuner settings v. Set the sleep timer vi. Adjust sound controls	**2M**

		vii. Use the V-Chip (Parental Guide) controls viii. Adjust the picture ix. Change on-screen display (OSD) settings x. View signal frequency information **1**. **<u>Changing widescreen and normal viewing modes</u> Plasma** TV has several widescreen and normal viewing modes you can use: 4:3 viewing mode produces a square image similar to a standard TV.Panorama viewing mode stretches only the sides of the image to fill the screen, leaving the center of the image unmodified.16:9 viewing mode produces a widescreen image similar to the screen at a movie theater. When you are in 16:9 mode, you can select one of three zoom modes. **2. <u>picture-in-picture (PIP) mode</u>** When the picture-in-picture (PIP) mode is active, one picture is displayed on the full screen and the other picture is displayed in a small window. The OSD in the upper-right corner of your screen lists the programs displayed on the full screen and in the window. When the PIP button on the remote control is pressed once to turn on PIP mode. A small window appears in one corner of the screen. The picture on the full screen is the main picture. The picture in the window is the sub-picture. **3. <u>Picture-on-picture (POP) mode</u>** When the picture-on-picture (POP) mode is active, the screen is divided into two equal parts with a picture displayed on each side. The OSD in the upper-right corner of your screen lists the video input source displayed on each side of the screen. When press the PIP button on the remote control twice to turn on POP mode. The screen is split into two pictures. The picture on the left side of your screen is the main picture. The picture on the right side of the screen is the sub-picture. **4. <u>Changing TV tuner settings</u>** One can set the desired tuner setting on plasma TV by using tuner control available on remote. **5. <u>Setting up a favorite channel</u>** One can change the favorite channel settings using the remote control or the OSD. **6. <u>Locking channels</u>** If one do not want a channel to be accessible, he can set the channel lock for that channel. When anyone tune to a locked channel, they are prompted to enter your password.	**2M**
e)		**Describe orientation of liquid crystal form of matrix of picture planels in TV.**	**4M**
Ans:		**<u>Diagram:</u>**  	**2M**

		Explanation:- **Formation of a matrix of picture pixels:** • As any incident light strikes the first glass filter it is polarized. The molecules in each layer of the applied nematic crystals then guide the light they receive to the next layer. • As the light passes through the liquid crystal layers, its molecules also change the light's plane of vibrations to match their own angle. • Then light reaches the far side of the liquid crystal substance, it vibrates at the same angle as the final layer molecules. If the final layer is matched up with the second polarized glass filter then the light will pass through. • If an electric charge is applied to liquid crystal molecules they untwist. On straightening out they change the angle of light passing through them so that it no longer matches the angle of the top polarized filter. • Consequently, no light can pass through that area of LCD, which makes it darker than the surrounding area.	**2M**
	f)	**Draw diode splite technique for generation of EHT.**	**4M**
	Ans:	**Diagram:**  **Explanation:-** • The Diode split technique is three layer secondary windings are shown wound round the ferroxide core of the L.O.T While the three section are shown separately, in actual practice these are wound one above the other and are thus concentric. Each winding is identical to the other and has the same number of turns. The same magnitude of voltage will therefore be induces in each section every time the flyback derived input pulse gets applied to the primary windin . • Because of the close proximity of individual layers, an inter-layer capacitance exists between each of them. It is indicated in the diagram by capacitors in dotted – chain form because these are no physical capacitors. If a diode is connected between the end of the layer of winding and the start of the next, the ac voltages induced in each layer can be	**2M** **2M**

		made to charge up all the inter-layer capacitances to the same voltage. Since the capacitances are effectively in series, the total voltage, appearing at the output terminal is the sum of all the voltages appearing across all of them. The diodes shown connected in series between the layers are physically embedded in the winding and form an integral part of the transformer. • The three winding are so designed that voltage induced in each layer form the flyback transformer in 8.33KV. This makes the total potential equal to 25KV and forms the EHT supply source. IN some designs, four layers of windings are used and each layer provides a voltage equal to 6.8KV	
Q. 3		**Attempt any four:**	**16M**
	a)	**Draw and describe basic structure of SAW filter.**	**4M**
	Ans:	**Diagram-**	**2M**
		 **Figure: Construction diagram of SAW filter**	
		Explanation:- • The SAW filter uses two crystal, which have piezo-electric properties. When a varying electrical signal is applied across two surface of such a crystal, mechanical vibration are produced across the other opposite set of faces and vice versa. This characteristic has been made use of in the SAW filter. • The transducing crystal is cut into segments, called fingers. All fingers are of the same length in the input transducer. Equal length of the fingers make it a broad band transducer	**2M**
	b)	**Draw schematic diagram of IC-CA-7607 and state its function.**	**4M**
	Ans:	**Diagram-**	**2M**

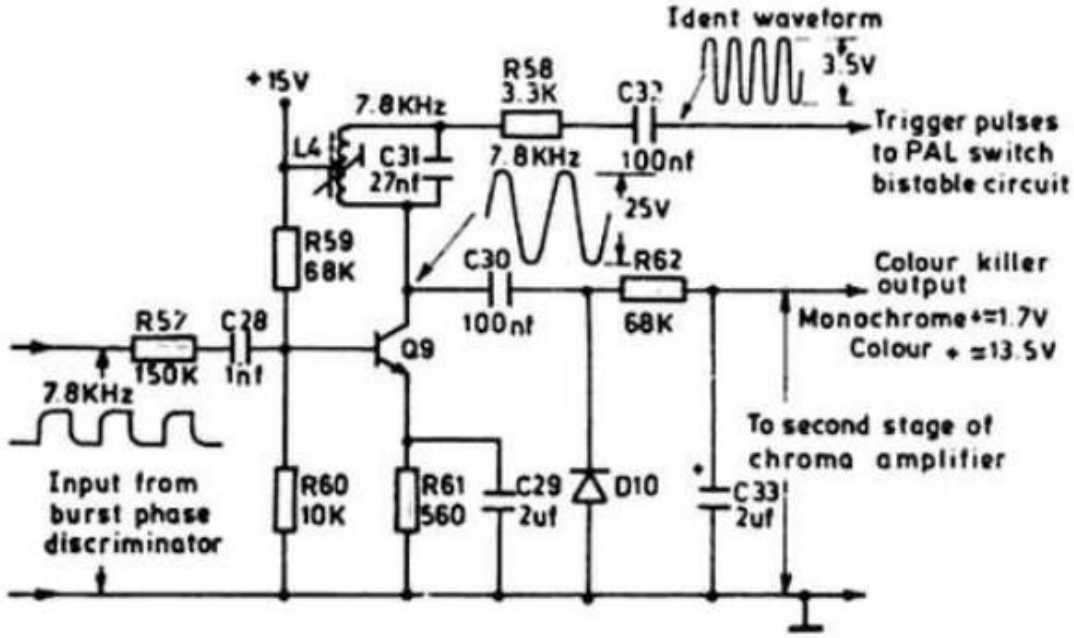


Explanation:

- **Gain Control of IF amplifier:** The gain control of IF amplifier is a cascade of 3 stage wide band amplifier. It amplifies IF output received from the SAW filter to a suitable level. The maximum overall gain of the IF amplifier is kept about 60dB to obtain sensitivity of 100mV at 38.9 MHz. The gain of IF amplifier is controlled by the AGC controlled voltage which is applied to the 3rd stage of IF amplifier.
- **Synchronous Demodulator:** A synchronous demodulator is used for detecting composite video signal. It requires a dual modulated IF signal and a reference signal for detection. It consists of 2 dual differential amplifiers and 2 modulated transistors that work in push pull configuration to detect video signal output.
- **Video Pre- Amplifier:** The video pre-amplifier with noise cancellation circuit is used as a buffer stage for impedance matching and feeding of signal to the succeeding stages. The bandwidth of this amplifier is slightly greater than 5MHz.
- **White spot inverter:** White spots on the screen are caused by excessive current due to overmodulated signal. This circuit faithfully detects the noise signal and plans them to safe amplitude.
- **AGC detector & noise inverter:** AGC circuit generates control voltage to limit the video signal amplitude during both positive and negative noise spikes and when the voltage of the signal is low. The noise inverter circuit cancels the noise signal by adding inverted noise pulses detected by white spot inverter.

2M

c)	**Draw schematic diagram of Colour killer circuit and state its function.**	**4M**
Ans:	**Diagram-**	**2M**



Explanation:-

- The dc operating voltage to Q9 is supplied via center tap on L4. Such a connection causes L4 to function as a tuned autotransformer & enables a waveform of about 25V peak-to-peak to be developed at the collector of Q9. **2M**
- This is fed via C30 to diode D10 which functions as a HWR. The components R62 & c33 form a LPF which provides a steady dc level of about 13.5V as the output. This is the color killer voltage which is used to control conduction of the second stage of Chroma signal amplifier.
- When a black and white picture is being received, there is no output from the burst discriminator & hence, no input to burst phase indent amplifier.
- Under this condition the color killer output fails to less than 2V which is not enough to forward bias transistor of the Chroma amplifier. Thus the second Chroma amplifier stage is inhibited.
- This prevents application of any signal to the Chroma delay line & to the U & V demodulators. Thus any stray coloring signals are prevented from reaching RGB amplifier & hence, no colour noise appears on the black & white picture during monochrome receptions.

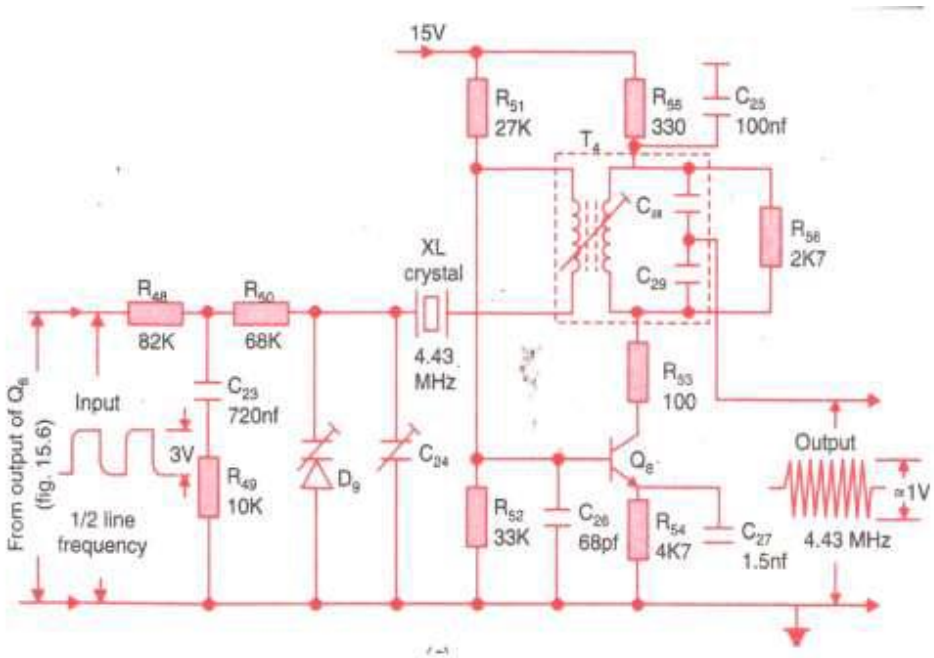
d)	**Compare plasma and LCD display technology (any four points).**	**4M**
Ans:		**(1M Each)**

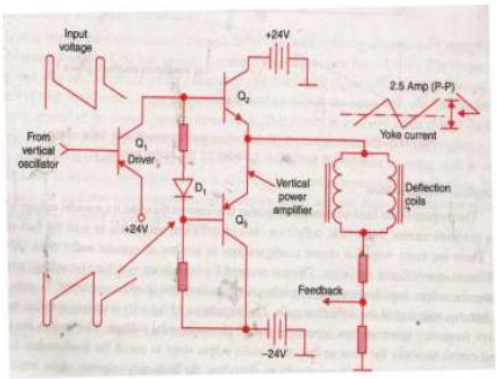
Comparison:

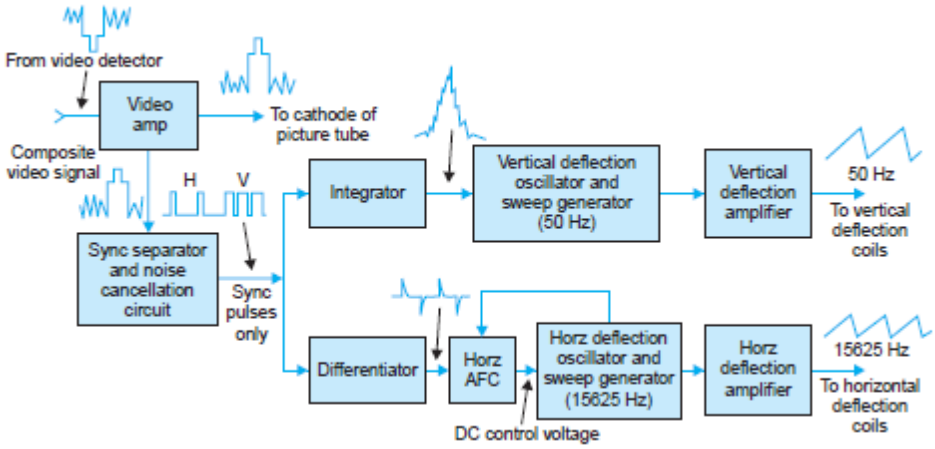
Parameter	Plasma Display	LCD Display
Brightness	Very poor in direct sunlight without reflective design (battery powered devices);	Some panels are highly reflective, should be used in a dark environment for optimum picture quality
Contrast	Over 1,000:1	Over 20,000:1
Color	Good on most newer models	Excellent
Ghosting & Smearing	Display motion blur on models with slow response time, and the elimination technique (strobing backlight) can cause eye-strain	None even during fast motion, advancements in 3D have eliminated phosphor trailing due to the use of fast-switching phosphors
Response Time	1–8 ms typical (according to manufacturer data), older units could be as slow as 35 ms	Sub-millisecond
Environmental influences	Low temperatures can cause slow response, high temperatures can cause poor contrast	High altitude pressure difference may cause poor function or buzzing noises
Aging	Yes	Yes
Weight	Light	Heavy, however, less weight gain per size increase

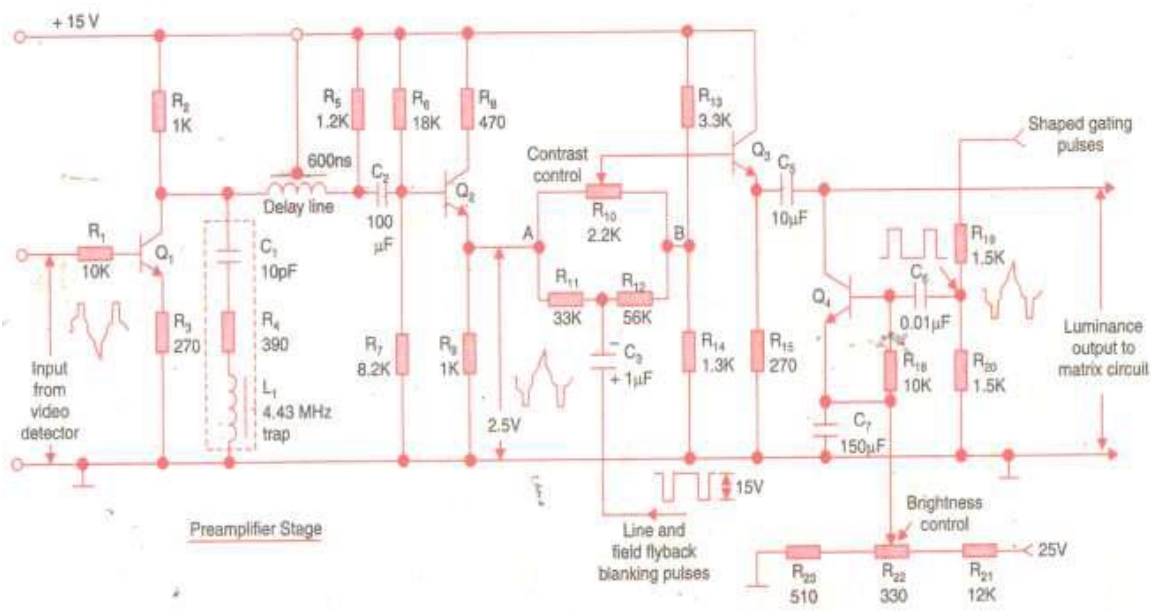
e) Draw ckt diagram of reference oscillator and state its need in PAL-D decoder. 4M

Ans: Diagram- 2M



		Need of reference oscillator in PAL- D decoder: • The U and V Chroma signals are separately produced at the transmitting end by what is known as double- balanced suppressed-carrier modulator.Thus it is necessary to regenerate the subcarrier in the receiver to affect demodulation of colour difference signal. • The reference oscillator circuit that generates a sinusoidal output at 4.43MHz is shown in figure above. • The frequency is determined by the center-resonant frequency of the crystal (XL) which in this circuit is approximately 4.43MHz.	**2M**
Q. 4	A)	**Attempt any Three.**	**12M**
	a)	**State need of AGC in Colour Tv Receiver.**	**4M**
	Ans:	**Need of AGC:** • Automatic Gain Control (AGC) circuit varies the gain of a receiver according to the strength of the signal picked up by antenna. • Useful signal strength at the receiver input terminals may vary from 50μV to 0.1V or more, depending on the channel being received and distance between transmitter and receiver. • The AGC bias is a DC voltage proportional to the input signal strength. It is obtained by rectifying the video signal as available after the video detector. • The AGC bias is used to control the gain of RF and IF stages in the receiver to keep the output at the video detector almost constant despite changes in the input signal to the tuner.	**4M**
	b)	**Draw ckt diagram of vertical output amplifier and describe its working.**	**4M**
	Ans:	**Diagram:** (Diagram-2 Marks; Working- 2 Marks) Ans: **Diagram:**  **Figure: Circuit diagram of vertical output amplifier** **Working:** • The output transistor Q2 and Q3 operate under class 'B' and are alternately driven in to conduction by a common trapezoidal input signal. • When Q2 is ON and Q3 is OFF, current flows through the yoke from the positive 24V supply. On the alternate half of the input signal when Q3 is ON and Q2 is OFF, current flows in the opposite direction from the negative 24V supply. • This amounts to an AC current flow through yoke. Diode D1 is forward biased and voltage drop across it provides suitable bias to Q2 and Q3 thereby preventing any crossover distortion. • The conduction of diode D1 also ties the bases of Q2 and Q3 allowing signal output from	**2M** **2M**

		the driver Q1 to feed both of them simultaneously.	
	c)	**Draw the block diagram of sweep section and elaborate the function of any two blocks.**	**4M**
	Ans:	**Diagram-**  **Explanation:-** • The synchronizing pulses generally called 'sync' are part of the composite video signal as the top 25 percent of the signal amplitude. • The sync pulses include horizontal, vertical and equalizing pulses. There are separated from the video signal by the sync separator. • The clipped line (horizontal) and field (vertical) pulses are processed by appropriate line-pulse and field pulse circuitry. The sync output thus obtained is fed to the horizontal and vertical deflection oscillators to time the scanning frequencies. • As a result, picture information is in correct position on the raster. The sequence of operations is illustrated in Fig. by a block schematic diagram.	**2M** **2M**
	d)	**Draw Luminance signal processing ckt diagram and describe its working.**	**4M**
	Ans:	**Diagram-**	**2M**

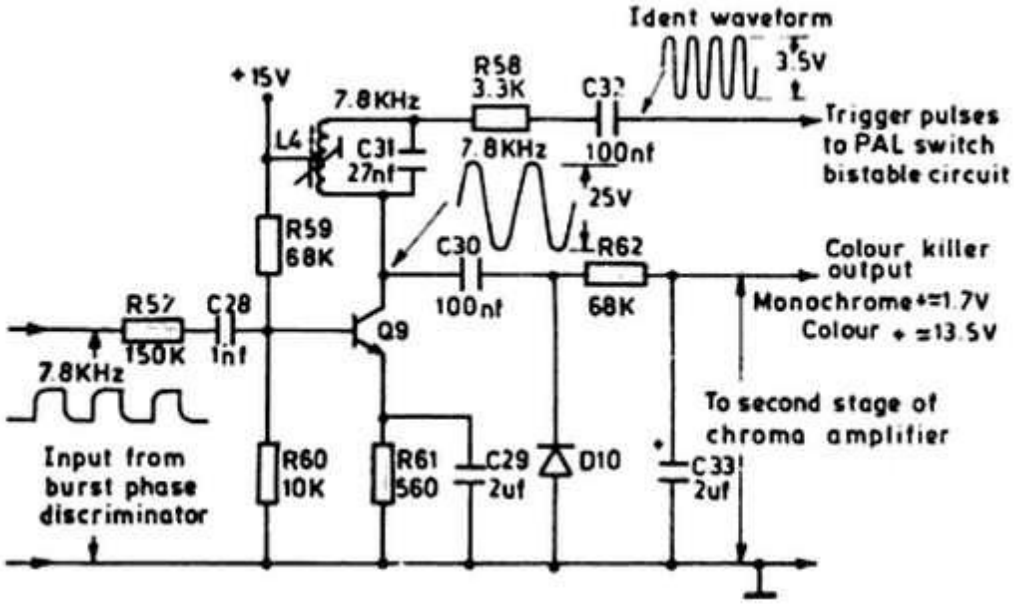


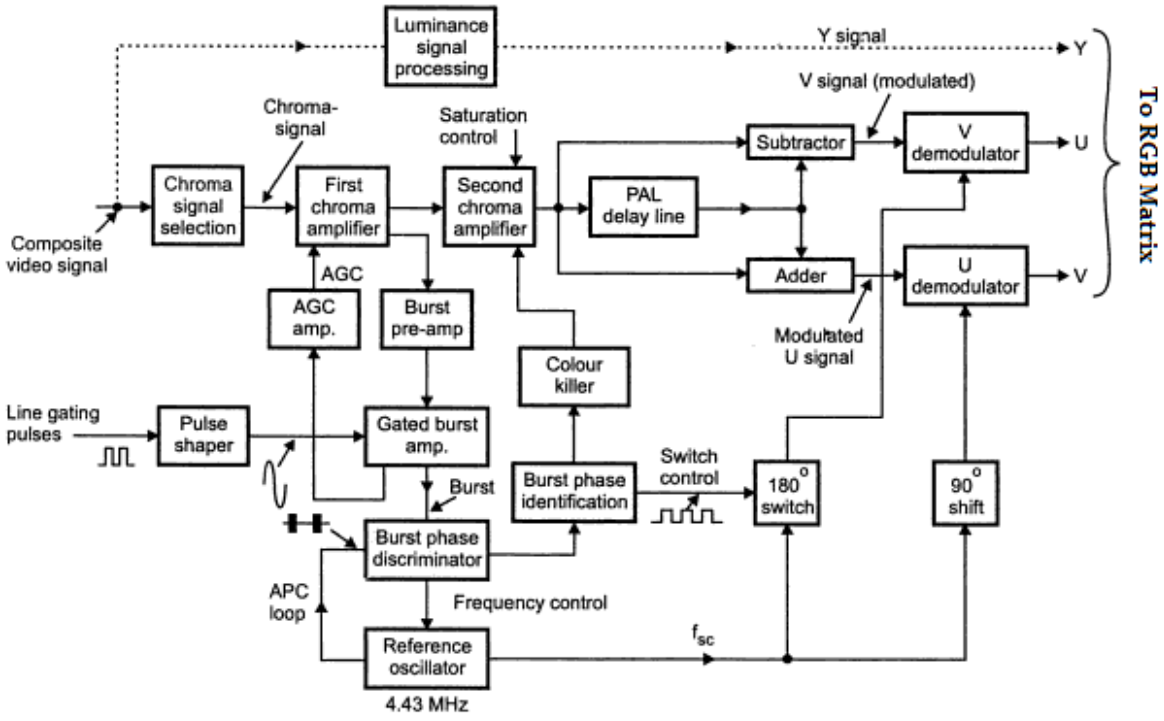
Working:

- Transistor Q1 constitutes the preamplifier and it designated to provide impedance match to the delay line on its output side and video detector on the input side.
- The amplified and inverted signal that becomes available at the collector of Q1 is fed via delay line at the base of Q2. The in between series trap formed by C1, R4 and L1 is to bypass Chroma signal.
- The contrast control elements R10, R11 and R12 form a part of a bridge circuit where potentials at point A and B are at the same level. The dc voltage at point A is nearly 3V and therefore values of R13 and R14 are so chosen that voltage at point B is also equal to 3 volts.
- The clamping voltages are applied directly to the emitter of Q4 which is connected to operate as an electronic switch. During picture content periods of the Y signal, the transistor is held in nonconducting state by resistor R18 connected between base and emitter.
- During back porch intervals of the video signal, Q4 is momentarily forced into full conduction by the arrival of positive going line frequency rate pulses applied to its base via capacitor C6.
- The amplified video (luminance) signal obtained at the output of luminance channel is either passed on to a suitable stage in the Chroma IC or to the discrete R,G &B output stage.

2M

	B)	**Attempt any one of following:**	**6M**
	a)	**Illustrate with suitable ckt diagram how the IDENT and Killer o/p's are obtained from the burst phase discriminator output.**	**6M**
	Ans:	**Explaination-** The dc operating voltage to Q9 is supplied via center tap on L4. Such a connection causes L4 to function as a tuned autotransformer & enables a waveform of about 25V peak-to-peak to be developed at the collector of Q9.	**3M**

		• This is fed via C30 to diode D10 which functions as a HWR. The components R62 & c33 form a LPF which provides a steady dc level of about 13.5V as the output. This is the color killer voltage which is used to control conduction of the second stage of Chroma signal amplifier. • When a black and white picture is being received, there is no output from the burst discriminator & hence, no input to burst phase indent amplifier. **Diagram-**  • Under this condition the color killer output fails to less than 2V which is not enough to forward bias transistor of the Chroma amplifier. Thus the second Chroma amplifier stage is inhibited. • This prevents application of any signal to the Chroma delay line & to the U & V demodulators. Thus any stray coloring signals are prevented from reaching RGB amplifier & hence, no colour noise appears on the black & white picture during monochrome receptions.	**3M**
	b)	**Draw neat diagram of PAL decoder and state the function of each block.**	**6M**
	Ans:	**Diagram-**	**3M**



Block diagram of PAL-D decoder

Explanation:-

Chroma signal selection:

Its function is to select Chroma and colour burst signal from the incoming CCVS signal. It essentially consist of band pass circuit whose center frequency is chosen to be equal to that of Chroma sub-carrier itself i.e.4.43MHz.

1st Chroma amplifier:

The Chroma and burst signals are amplified by first Chroma amplifier which is controlled by DC voltage developed by the Automatic Chroma Control (ACC) amplifier.

2nd Chroma amplifier*:*

The second Chroma amplifier incorporates colour saturation control circuit. The output of colour killer also feeds into it.

PAL delay line (separation of U and V colour phasors*):*

This network separated U and V signals with are then fed to respective demodulator.

Gated burst amplifier*:*

The gated burst amplifier separates the burst pulses and amplifies them a level suitable to operate the burst phase discriminator.

Automatic Chroma Control (ACC*):*

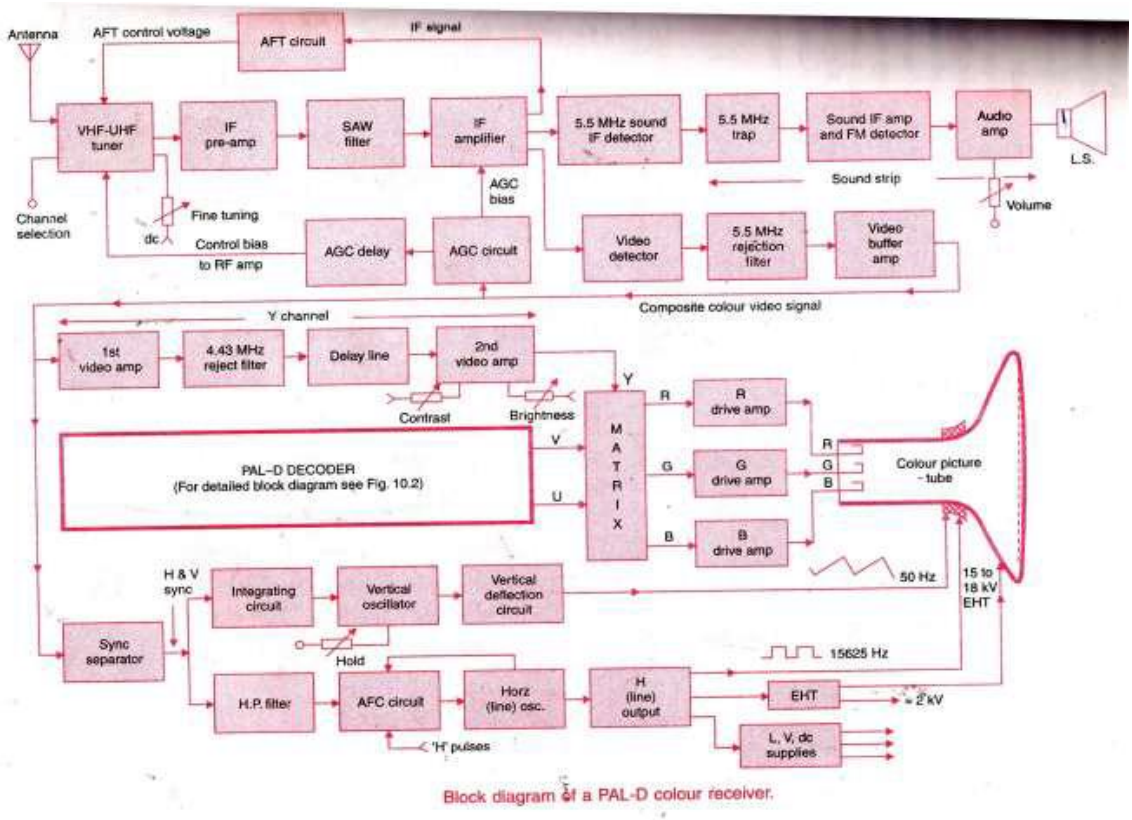
The magnitude of the voltage so fed back is proportional to the magnitude of the burst and therefore to the amplitude of Chroma signal itself. This voltage is used to control the first stage of Chroma amplifier in such way to ensure constant Chroma signal amplitude.

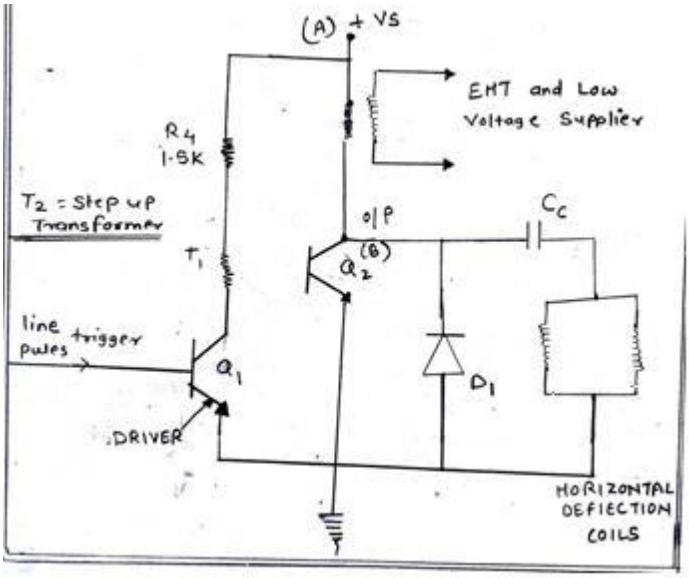
Burst phase discriminator*:*

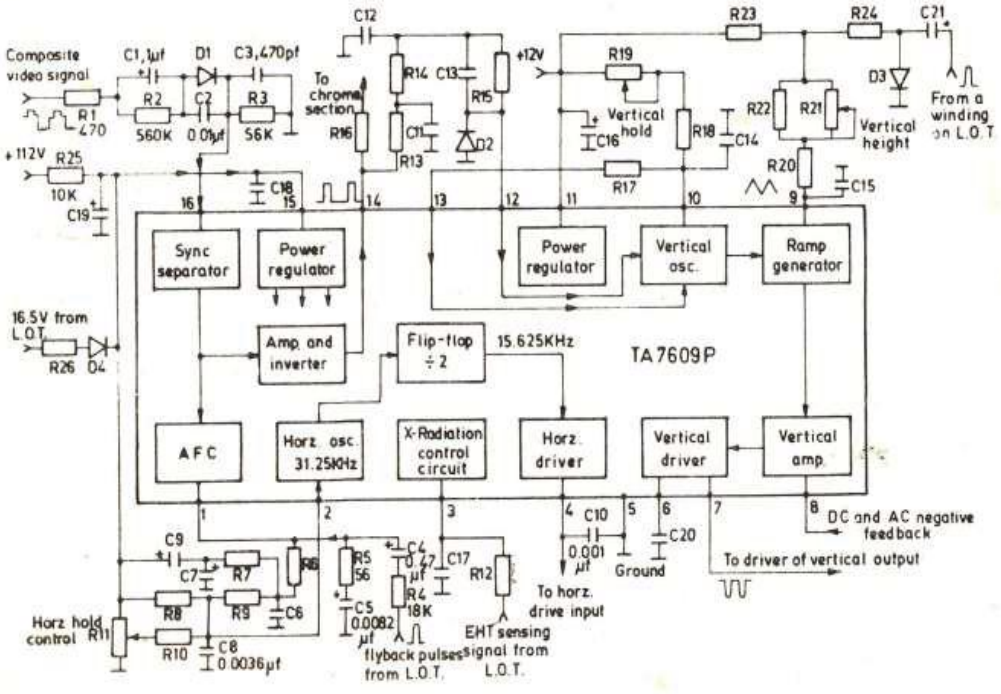
It is sensitive to burst pulses and is designed to detect any differences which might exist between the phase of burst pulse and that of the reference oscillator. It produces at its output a dc voltage whose magnitude and polarity are proportional to the magnitude and direction of the detected phase difference.

Burst phase identifier*:*

3M

		This circuit is able to identify the phase relationship of the colour burst. **180º switch:** This switch is used to periodically invert the waveform fed to the v-signal demodulator. **Colour killer control:** This is just a half wave rectifier which produces a steady dc potential from the succession of burst pulses. During black and white transmission the dc potential is absent and hence biases the 2nd Chroma amplifier to cut off state.	
Q.5		**Attempt any two.**	**16M**
	a)	**Draw neat block diagram of colour TV receiver and state function of each block.**	**8M**
	Ans :	**Diagram-**  Block diagram of a PAL-D colour receiver. **Explaination-** **IF amplifier & Saw filter:-** The saw filter is used for V_{SB} correction. It is necessary to provide IF amplifier to compensate for the large uniform attenuation of the signal that occurs in the saw filter. **AGC stage:-** AGC circuit varies the gain of the receiver according to the strength of the signal picked up by the antenna. The AGC bias is used control the gain of RF & IF stage in the receiver to keep the output at the video detector almost constant despite changes in the input signal to the tuner. **Video Detector:-** Modulated IF signals after due to amplification in the IF section are fed to the video detector. The detector is designed to recover composite video signal and to transform the	**4M** **4M**

		sound signal to another lower carrier frequency. This is done by rectifying the input signal & filtering out unwanted frequency components. A diode is used which is suitable polarized to rectify either positive or negative peaks of the inputs. **Luminance Section:-** This section blocks the chroma signal and one (1MHz) side bands. Here delay line is used, because luma signal processing requires less stages than chroma signal processing and hence delay of 0.6μs is provided to luma signal and hence they are needed at the same time in RGB matrix and hence synchronization is maintained. The contrast and brightness control is also provided in this stage. **PAL – D Decoder:-** The PAL – D decoder performs the following function: • Chroma signal separation and amplification. • Separation of U and V signal phasor by employing delay line technique. • Demodulation of U & V phasor to recover colour difference signals • Generation of suitable sub-carrier for the two demodulators. • To develop ident signal for V channel switching & biased voltage for colour killer circuit. **RGB Matrix, RGB driver stage & picture tube:-** The RGB matrix consist of demodulated U & V signals along with Y signal at the output, we get separate R,G,B signal. RGB driver stage amplify the RGB signal to sufficient level to drive it to picture tube. Picture tube consist of three separate cathodes for primary colours R,G,& B signals. It also consist of three different control signals.	
b)	**Draw neat circuit diagram of horizontal output amplifier and describe its operation.**		**8M**
Ans :	**Diagram-**  **Working :-** • The principle of diode spilt addition is illustrated in fig where three layers of secondary winding are shown wound round the feeroxide core of LOT while the three sections are shown separately. In actual practice, these are wound one above	**4M** **4M**

		the other and are thus concentric. Each winding is identical to other and has the same no of turns. • The same magnitude of voltage will be induced in each section every time the fly back derived input pules gets applied to primary winding. • Because of close proximity of individual layers and interlayer capacitance exist between each of them . • It is indicated in the diagram by capacitor in dotted chain form become these are not physical capacitor of a diode is connected between the end of layers of winding and start of the next the Ac voltage induced in each layers can be made to change. • Up all the interlayer capacitance to the same voltage since the capacitance are effectively in series. • The total voltage appearing at the output terminal is the sum of all voltage appearing across all of them. • The diode shown connected in series between the layers are physically embedded in winding from an interlayer part of Transformer The three winding are so designed that voltage induced in each layer form the fly back Transformer is 8.33 Kv. • This makes total potential equal to 25Kv and forms the EHT supply source.	
c)	**Draw schematic diagram of IC 7609 and state the function of each block.**		**8M**
Ans :	**Diagram-**  **Explaination-** **SYNC Separator:-** A transistor with double time-constant leak-bias input circuit is used as sync separator to prevent blocking g strong noise pulses. As shown in the figure, negative going composite colour video signal obtained either from a pin of the vision IF IC. The line sync pulses being of much shorter duration (high frequency) pass through the small value capacitor **C2** to cause base current and hence produce sync output. The charge that	**4M** **4M**

builds across C_2 quickly discharges through D_1 when each sync pulse passes away. The double time-constant circuit also prevents any noise pulses from holding the device at cut-off for longer periods. The transistor operates with a small Vcc supply and large load resistance so that it bottoms quickly to provide clean sync pulses. The sync output (see Fig. 13.1) is fed directly to the AFC circuit and after amplification to the vertical and chroma sections of the receiver from pin 14.

AFC Circuit:-

A single ended discriminator similar to the AFC detector is built in the IC to prevent any phase or frequency deviation of the line oscillator. The two inputs to this circuit are the sync pulses and line flyback pulses. The flyback pulses are shaped into sawtooth shape by the integrating capacitor **C_5** before feeding from pin 1 to the AFC circuit. On any frequency deviation, control voltage from the AFC circuit is in the form of pulses at the oscillator rate. It is smoothened by the external filter networks R_6-C_6 (pin 1) and R_7-C_7 before applying through **R_9** to the line oscillator at pin 2.

Horizontal Oscillator:-

The line oscillator circuit is around an operational amplifier where the feedback network is for sustained oscillation and input circuitry to determine frequency. The capacitor **C_8** at pin 2 forms part of this circuit. The frequency is set at the correct value by varying dc voltage to the oscillator circuit (pin2)from the 12V dc rail through **R_8, R_{10}** and R_{11}. Thus potentiometer R_{11} acts as 'hold' control for the linedeflection frequency.

The oscillator is operated at 31.25 KHz (twice of 15.625 KHz) and then a flip-flop circuit divides it by 2 to obtain the desired 16525 Hz rate. The reason for fixing the oscillator frequency at 31250 Hz instead of 15625 Hz is twofold. Firstly, the divide circuit indirectly prevents any variations in the width Of output pulses thus minimizing dispersion effects in the line output circuit. Secondly, the magnetic oninduction effect from line to frame oscillator in the ICs is identical during both fields of a frame thereby ensuring good interlaced scanning than when alternate fields are affected differently with oscillator operating at 15625 Hz.

X- Ray Radiation Control:-

X-ray radiation prevention circuit is designed to disable the line oscillator should the EHT voltage a exceed limit that can cause radiation from the screen face. The signal to sense this is obtained from a section of the line output transformer and fed to the control circuit at pin 3 through R12 and C17.

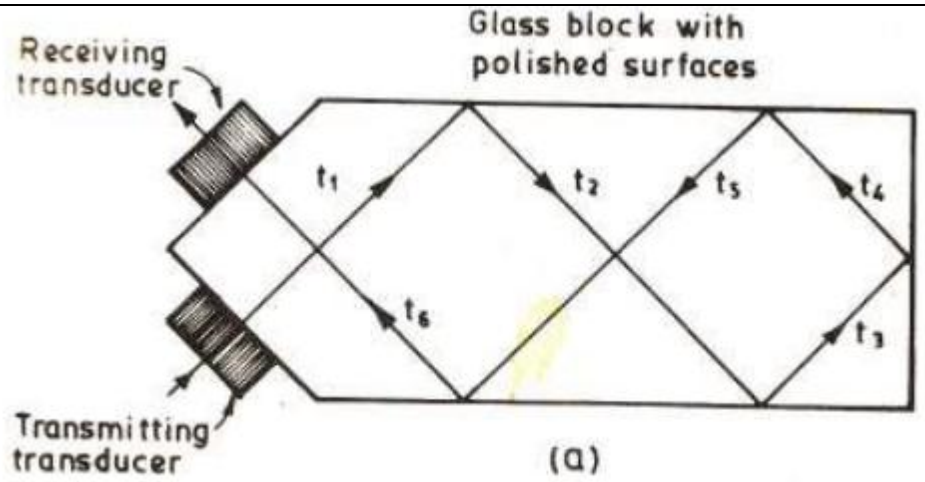
Horizontal Driver:-

The .driver that is fed from the flip-flop output is a single-ended differential amplifier which besides wave shaping amplifies line drive pulses. The capacitor C10 (0.00111F) connected at pin 4 is for wave shaping as necessary. The output from the driver amplifier is fed to the line output stage from pin 4 as shown in the figure.

Vertical Oscillator:-

Vertical oscillator is a multivibrator circuit triggered by vertical sync pulses. These pulses on obtaining from pin 14 are passed through a two stage integrating network comprising of R13-Cii and R14-C12. The output is then wave shaped by R15-C13 and diode D2 before feeding to the oscillator control circuit. The differential amplifier of the multivibrator circuit performs current switching function and generates a positive going output of constant amplitude at a frequency of 50 Hz. A negative feedback through R17 connected between pins 10 and 13 is to stabilized the oscillator operation. The time-constant circuit formed by C14, R18, R19 and connected at pin 10 from the 12V source determines frequency of

		oscillations. Thus potentiometer R19 acts as the vertical 'hold' control. **Ramp Generator:-** A ramped shaped drive is necessary for the vertical deflection amplifier. It is generated by charging C15 through a transistor driven by oscillator's output pulses. The charge and discharge i.e., retrace and traced periods are controlled by the external R-C network connected at pin 9. With a positive pulse of constant width at the base of ramp generating transistor, capacitor C15 charges quickly to provide the retrace period. As the input pulse drops/ the transistor turns-off enabling the capacitor to discharge through resistive network formed by R20, R21, R22, i23 and input resistance of dc supply. The time-constant of this discharge path is large enough to provide a near linear trace period. The amplitude of ramp thus generated can be controlled by changing magnitude of dc voltage applied at pin9. This as shown in the figure, is done by varying R21. It is necessary to maintain width to height ratio of the raster constant at 4:3. Any change in dc voltage to the line output stage will affect width of the reproduced picture. It then become necessary to cause corresponding change in height of the picture to maintain the aspect ratio at 4:3. This is obtained by alternating height of the ramp in an interesting way. Any deviation in the amplitude of line output pulses is sampled from a section of the winding on the line output transformer. These positive going pulses are rectified by diode D3 to produce a proportionate dc voltage across C21. The negative end of this voltage is connected to R21via R24 at the point where de supply is connected to it. Any change in the magnitude of negative voltage caused by line pulse amplitude variations will affect net dc voltage applied to the ramp capacitor. **Vertical Amplifier:-** This is a single ended differential amplifier designed to amplify ramp output to a level necessary to drive the vertical output stage. Negative feedback, both dc and ac is applied to it from different points in the output stage amplifier to obtain correct centering and linear deflection in the vertical direction. **Vertical Driver:-** It is an emitter follower for current gain and impedance matching between the drive amplifier and vertical output stage. The capacitor C20 at pin 6 is for decoupling purposes in the vertical dreiver section of the IC. **DC –Supply:-** As shown in the figure, dc supply to the IC is from two sides. A dc supply at 12V from the L.O.T side feeds at pin 11 to a regulator that feeds vertical section blocks in the integrated circuit. Another dc voltage from L.O.T. at 16.5V is connected to a different dc rail via voltage dropping resistor R26 and diode D4. This is paralleled with a source obtained from ac mains side at 112V and dropped through R25 to obtain nearly 10V dc on the dc rail. This common dc rail is connected through pin 15 to another voltage regulator for supplying dc voltages to various line oscillator blocks in the IC. This improves efficiency of the line output stage and decreases power drain from ac mains.	
Q.6		**Attempt four of following:**	**16M**
	a)	**Draw construction of croma delay line and describe its working.**	**4M**
	Ans:	**Diagram-**	**2M**



Working:

- The electrical signal from the chroma amplifier with a mean frequency of 4.43MHz is coupled into the transmitting transducers where it is converted into an equivalent ultrasonic signal having the same mean frequency & pattern of amplitude variations. The signal travels through the glass block in a multiple path due to reaction from the polished surface before it reaches the receiving transducer. **2M**
- In the figure it is converted back into the original electrical form but delayed in time with respect to the signal at the input of transmitting transducer.
- The delay of signal is caused by low velocity of the ultrasonic signal as it passes through glass of the delay line. This is typically 3mm per μs as compared to the hundreds of thousands of mm per μs transferred by an electrical signal passing along a length of wire.

b) What is 3D TV Technology? Why it is necessary to use special glasses for watching 3D programmers? **4M**

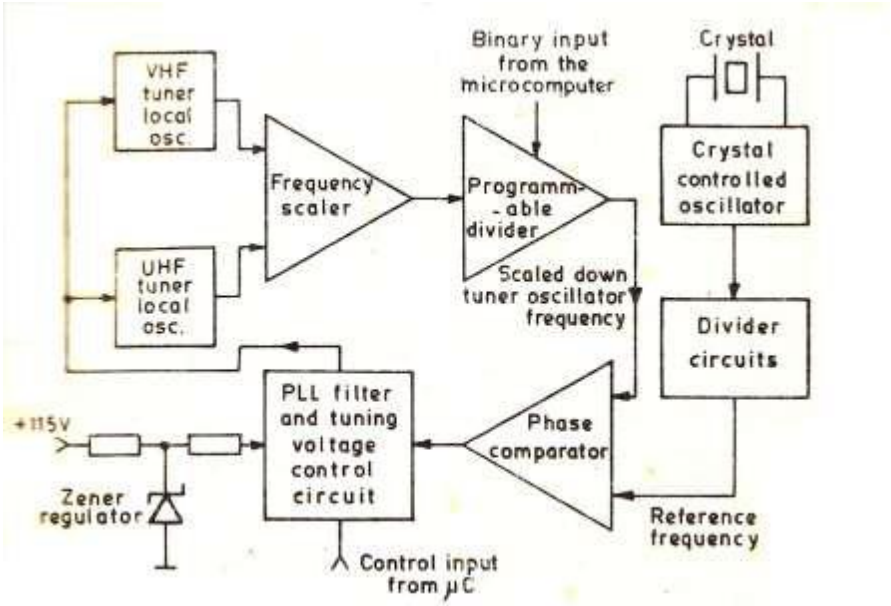
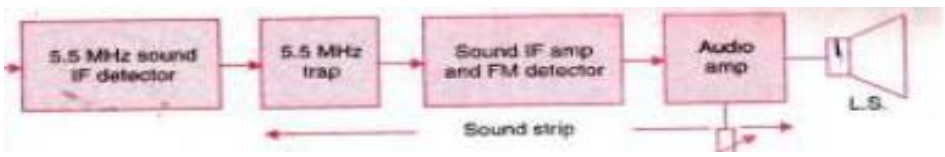
Ans:

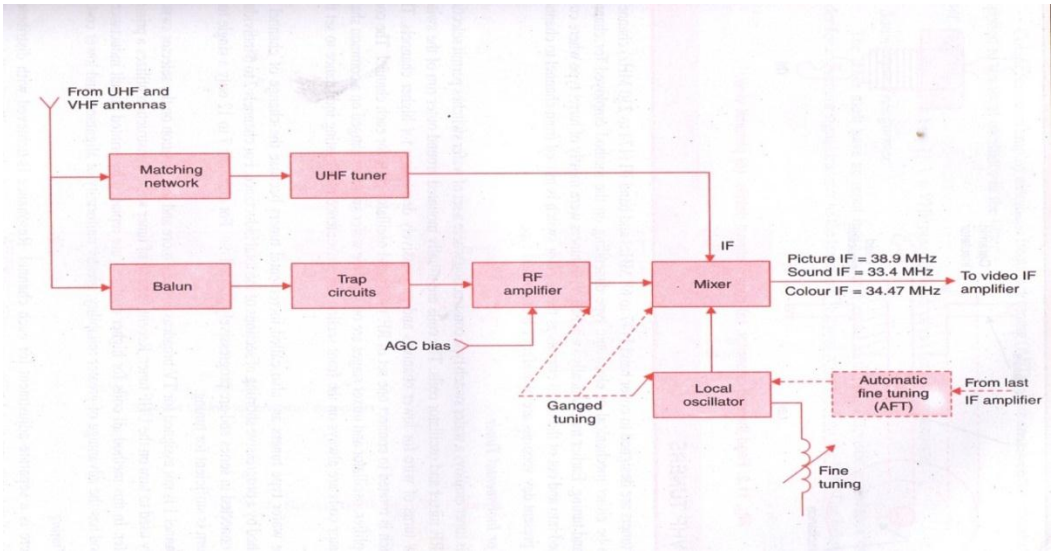
Explanation: **2M**

The 3D system relies on a visual process called STEREOPSIS which enables 3D perception. This comes out of the fact that the eyes of an adult human lie about 2.5 inches (≈6.5cm) apart which lets each eye see objects from slightly different angles. The combined effect of this on the viewer's mind is that of a three dimensional picture. This ability of our eyes is used in 3D TVs by showing the same object from difference angles on the screen to cause the same the same 3D perception.
Everyone sitting around 3D TV must wear special glasses to see the 3D effect.
Without glasses the image on the TV screen will appear doubled, distorted and for most practical purposes unwatchable. Currently there is no technology that enables watching 2D and 3D content simultaneously without glasses.

Necessary of glasses:- **2M**

The technique used in 3D TV receiver for display of pictures on screen were based on the use of two video signals in different ways to create the illusion of 3D pictures when viewed with special glasses. In 3D the phosphor strips of green colour of picture tube are excited by G video signal originated at one of the two cameras. Similarly all red phosphor strips are excited by R video signal generated by another camera and blue phosphor strips are not excited at all. Therefore special filter glasses are needed to be worn while watching 3D

		picture on TV screen.	
	c)	**Illustrate with diagram woeking of frequency synthesizer tunning.**	**4M**
	Ans:	**Explanation:** The reference oscillator is crystal and its frequency is reduced to 1KHz by divider circuits. The aim being to reduce the frequency to a range that can be proceed and counted by standard logics circuit. The output of prescaler feeds into a programmable divider, the divide ratio of which is determined by microcomputer. The output of programmable divider is compared with reference frequency by phase comparator. The inputs to the comparators are of same frequency, the dc error voltage developed by PLL filter is zero and no correction is applied. **Diagram:**  If there is mismatch in the input of comparator the correct voltages are generated by PLL filter i.e, the comparator senses the difference and develops appropriate error voltage which gets added to the applied tuning voltage with proper polarity that the oscillator is forced to return to the correct frequency. The PLL circuit continuously monitors the local oscillator frequency and applynecessary corrections.	**2M** **2M**
	d)	**Draw neat block diagram of sound section of TV and explain it.**	**4M**
	Ans:	**Block Diagram:**  **Sound IF detector:** It detect the 5.5 Mhz sound IF band from IF amplifier (ie. IF band)	**2M** **2M**

		Sound IF amplifier and FM detector: It amplify the incoming sound IF signal and FM detector detect the original sound signal from modulated IF signal. **Audio amplifier:** Audio amplifier amplify the incoming audio signal to drive the loudspeaker.	
	e)	**Draw block diagram of hyper band tunner state different types of tunning.**	**4M**
	Ans:	**Diagram-**  **Types of tuning:** 1) Mechanical tuning. 2) Electronic tuning.	**2M** **2M**