

Subject Name: System Programming

MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION

(Autonomous) (ISO/IEC - 27001 - 2013 Certified)

WINTER-17 EXAMINATION

Model Answer Subject Code:

17517

Important Instructions to examiners:

- 1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
- 2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
- 3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
- 4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
- 5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
- 6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
- 7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q.	Sub	Answer	Marking
No.	Q. N.		Scheme
1.	a)	Attempt any three:	Marks 12
	1)	Define the following terms: i) Overlays ii) Subroutine linkages.	4M
	Ans:	 i) Overlays: Many modern computers use virtual memories that make it possible to run programs larger than physical memory either one program or several programs can be executed even if total size is greater than entire memory available. When a computer does not use virtual memory, running a larger program becomes a problem. One solution is overlays(or chaining). Overlays are based on the facts that many programs can be broken into logical parts such that only one part is needed in memory at any time. The program is divided by the programmer, in to main part (overlay root), that resides in memory during the entire execution and several overlays, (links or segments) that can be called, one at a time, by the root, loaded and executed. The subroutines of a program are needed at different times Subroutine linkage: It is a mechanism for calling another subroutine in an assembly language. The scenario for subroutine linkage. 	(Overlays :2marks, Subroutin e linkages: 2marks)

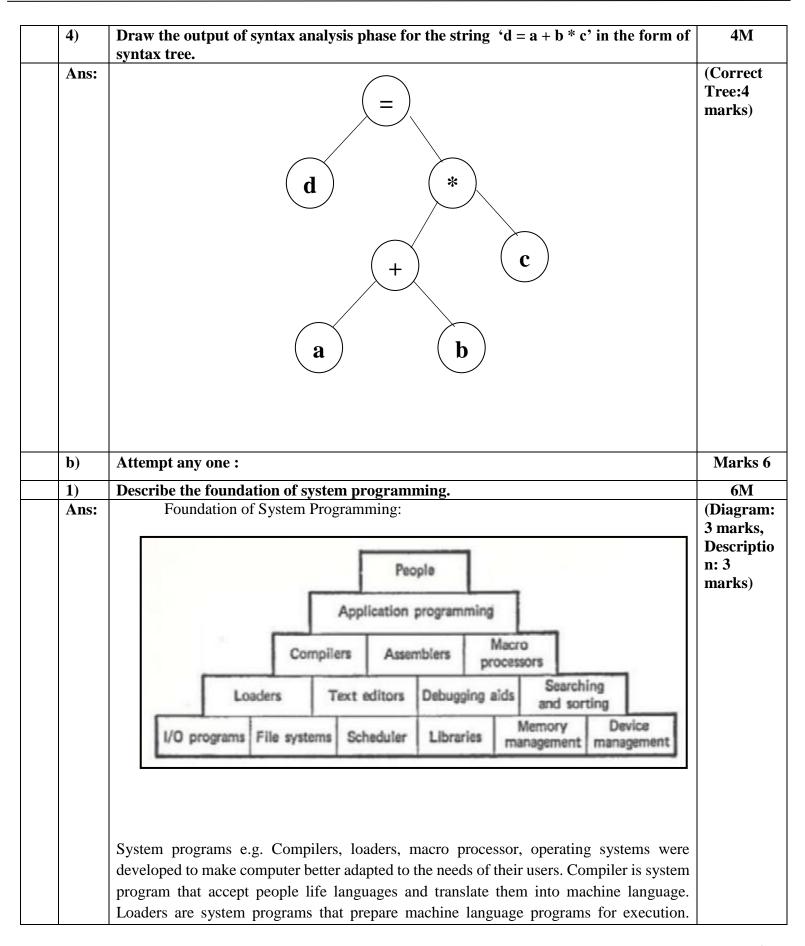
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1. A main program a wishes to transfer to subprogram B. 2. The programmer in program A, could write a transfer instruction. Eg (BA L, 14,B) to subprogram B. 3. But assembler does not know the value of this transfer reference and will declare it is an error. 4. To handle this situation a special mechanism is needed. 5. To handle it mechanism is typically implemented with a relocation or direct linking loader. Subroutine linkage uses following special pseudo ops: **ENTRY EXTRN** It is used to direct or to suggest loader that subroutine followed by ENTRY are defined in this program but they are used in another program. For example: the following sequence of instruction may be a simple calling sequence to another program. **MAIN START EXTRN SUBROUT** L 15=A(SUBROUT).....CALL SUBROUT BALR 14,15 **END** The above sequence of instructions first declares SUBROUT as an external variable, that is a variable referenced but not defined in this program. The load(L) instruction loads the address of that variable in to register 15. 2) What is operating system? Enlist the features of operating system as a system **4M** software. An Operating System (OS) is an interface between a computer user and computer (Definatio Ans: n:2marks, hardware. An operating system is a software which performs all the basic tasks like file any four features:2 management, memory management, process management, handling input and output, and marks) controlling peripheral devices such as disk drives and printers



	Features of operating system:							
	1. Assemblers							
	2. Computers, such as FORTRAN, COBOL, and PL/I							
	3. Subroutine libraries, such as SINE, COSINE, SQUARE ROOT.							
	4. Linkage editors and program loaders that bind subroutines together and prepare							
	programs for execution							
	5. Utility routines, such as SRT/MERGE AND TAPE COPY							
	6. Application packages, such as circuit analysis or simulation							
	7. Debugging facilities, such as program tracing and "core dumps"							
	8. Data management and file processing							
	9. Management of system hardware.							
	7. Wanagement of system nardware.							
3)	State and explain Binary search method with example.	4M						
Ans:	Binary Search Algorithm: A more systematic way of searching an ordered table. This	(Descri						
71115.	technique uses following steps for searching a keywords from the table.	n:2mar						
	1. Find the middle entry (N/2 or (N+1)/2)	Examp						
	2. Start at the middle of the table and compare the middle entry with the keyword to	marks)						
	be searched.							
	3. The keyword may be equal to, greater than or smaller than the item checked.							
	4. The next action taken for each of these outcomes is as follows If equal, the symbol is found							
	If equal, the symbol is found If greater, use the top half of the given table as a new table search							
	If smaller, use the bottom half of the table.							
	Example:							
	The given nos are: 1,3,7,11,15							
	To search number 11 Indexing the numbers from list [0] up to list[5]							
	Pass 1							
	Low=0							
	High = 5							
	Mid = (0+5)/2 = 2							
	Mid= $(0+5)/2 = 2$ So list[2] = 3 is less than 11							
	Mid= $(0+5)/2 = 2$ So list[2] = 3 is less than 11 Pass 2							
	Mid= $(0+5)/2 = 2$ So list[2] = 3 is less than 11 Pass 2 Low= $(Mid+1)/2$ i.e $(2+1)/2 = 1$							
	Mid= $(0+5)/2 = 2$ So list[2] = 3 is less than 11 Pass 2							







	2) Ans:	Macro processors allow programmers to use abbreviations. Operating system and file system allows flexible to bring and retrieval of information. The productivity of each computer is heavily dependent upon the effectiveness, efficiency and sophistication of the system programs. Draw flowchart of pass-I of two pass macroprocessor. Pass 1 — processing macro definitions MDTC<-1 MOTC<-1 Read next Source card Write copy of source card The productivity of each computer is heavily dependent upon the effectiveness, efficiency and sophistication of the system programs. Pass 1 — processing macro definitions Read next Source card Read next Source card Write copy of source card The productivity of each computer is heavily dependent upon the effectiveness, efficiency and sophistication of the system programs.	6M (Correct Flowchart: 6 marks)
2.		Prepare argument list array Enter macro name card into MDT MDTC <- MDTC + 1 MEND pseudo-op? No Attempt any two:	Marks 16
	1)	Explain Address calculation sort with suitable example.	8M
	Ans:	This can be one of the fastest types of sorts if enough storage space is available. The sorting is done by transforming the key into an address in the table that "represents" the key. For example if the key were four characters long, one method of calculating the appropriate table address would be to divide the key by the table length in items, multiply by the length is a power of 2, then the division reduces to a shift. This sort would take only N* (time to calculate address) if it were known that no two keys would be assigned the same address.	(Descriptio n:4 marks, Example:4 marks)



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However, in general. This is not the case and several keys will be reduced to the same address.

Therefore, before putting an item at the calculated address it is necessary to first check whether that location is already occupied. If so, the item is compared with the one that is already there, and a linear search in the correct direction is performed to find the correct place for the new item.

If we are lucky, there will be n empty space in which to put the item in order. Otherwise, it will be necessary to move some previous entries to make room.

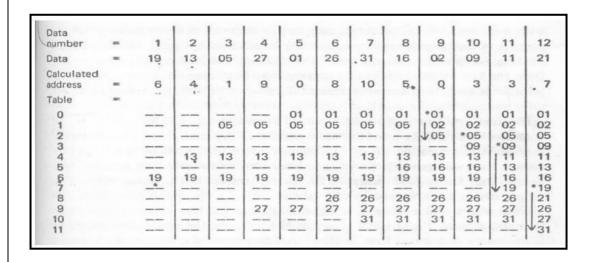


Figure: Example of address calculation sort

The table is of size 12; since it is known that maximum key is less than 36, the address transformation is to divide the key by 3 and take the integer part. A "*" indicates a conflict between keys, and the arrow indicates when a move is necessary and in which direction. The associated addresses calculated are given in the second row.

	The associated addresses calculated are given in the second row.	
2)	Explain format of databases in Assembler.	8M
Ans:	Pass 1 data bases	(Any 8 Datab ases : 1 mark each)



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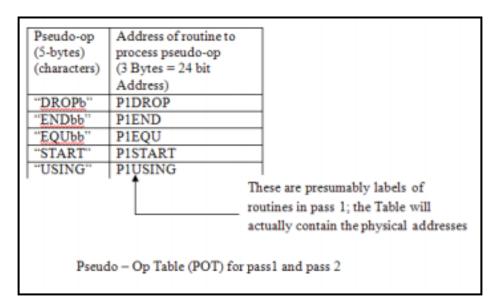
•		6-bytes per entry		
Mnemonic	Binary	Instruction	Instruction	Not used in this
Op-code	Op-code	Length	format	design
(4-bytes)	(1-byte)	(2-bits)	(3-bits)	(3-bits)
(characters)	(hexadecimal)	(binary)	(binary)	
"Abbb"	5A	10	001	
"AHbb"	4A	10	001	
"ALRb"	5E	10	0001	
"ARbb"	1E	01	000	
	1A	01	000	
"MVCb"				
	D2	11	100	

b~ represent the character "blank"

Codes:

Instructions length Instruction format 01 = 1 half-words = 2bytes 000=RR 10 = 2 half-words = 4bytes 001-RX 11 = 3 half-words = 6bytes 010 = RS 011 = SI100 - SS Machine - Op Table (MOT) for pass1 and pass 2

A POT (Pseudo operation Table)



A ST (Symbol Table)



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14-bytes per entry								
Symbol	Value	Length	Relocation					
(8 Bytes)	(4 Bytes)	(1 Byte)	(1 Byte)					
(Character)	(Hexadecimal)	(Hexadecimal)	(Character)					
"JOHNbbbb"	0000	01	"R"					
"FOURbbbb"	000C	04	"R"					
"FIVEbbbb"	0010	04	"R"					
"TEMPbbbb"	0014	04	"R"					
Symbol Table:								

• A LT (Literal Table)

Variable tables			
Symbol Table			
Symbol	Value	Length	Relocation
PRGAM	0	1	R
AC	2	1	A
INDEX	3	1	A
TOTAL	4	1	A
DATABASE	13	1	A
SETUP	6	1	R
LOOP	12	4	R
SAVE	64	4	R
DATAAREA	8064	1	R
DATA1	8064	4	R
Literal Table			
A(DATA1)	48	4	R
F'5'	52	4	R
F'4'	56	4	R
F,8000	60	4	R
-			

• A copy of the input to be used by pass 2

Pass 2 databases

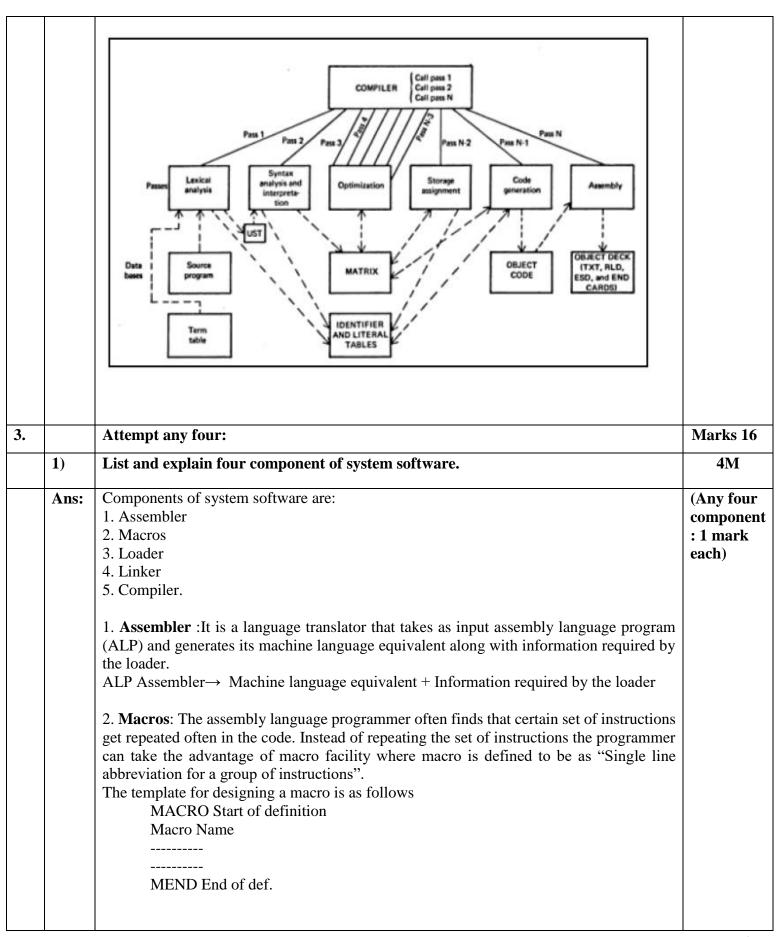
• Copy of source program input to pass 1

LC: Same as Pass IMOT: Same as Pass IPOT: Same as Pass I

• ST: Same as Pass I



	Av Y- N-	: "N" "Y" de= railability -register specified in US	Designated relative — address contents of base register (3-bytes = 24-bit address) (hexadecimal) 00 00 00 ING pseudo-op n USING pseudo-op or subsequently mad	15 entries te unavailable by the DROP	
3)	• Explain with	•	riew of passes of compiler.	oader	8M
Ans:	i. Pass 1 code ar	gical execution of this pass is correst ad creates an ident corresponds to syr	f the compilation process. ponds to lexical analysis phase ifier, literal and uniform symbolatactic and interpretation phase x and place information about	ool table. E. It scans the uniform symbol	/ Diagra 4 marks





	progra Functi a. Allo b. Lin c. Relo d. Loa Alloca execut Linkir Reloca Loadin 4. Lin object progra 5. Co progra	3.Loader: Loader is a system program which is responsible for preparing the object programs for execution and start the execution. Functions of loader a. Allocation b. Linking c. Relocation d. Loading Allocate the space in the memory where the object programs can be loaded for execution. Linking: Resolving external symbol reference Relocation: Adjust the address sensitive instructions to the allocated space. Loading: Placing the object program in the memory into the allocated space. 4. Linker: A linker which is also called binder or link editor, is a program that combines object modules together to form a program that can be executed. Modules are parts of a program. 5. Compiler: Compiler is a language translator that takes as input the source program(Higher level program) and generates the target program (Assembly language program or machine language program)								
		Source Program → Compiler → Target program								
2)	_	pare shell sort and Radix lexity.	Exchange sort on the ba	sis of space and time	4M					
Ans	:									
		Sort	Time Complexity	Space Complexity	complexity :2marks,					
		Shell Sort	O (n ²) to O(n* logn)	O(n)	Correct space complexity :2marks)					
		Radix Exchange Sort	O(nd)	O(k)						
2					4M					
3)	-	Explain in detail machine dependent optimization.								
Ans	Two types of optimization is performed by compiler, machine dependent and machine independent.									



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Machine dependent optimization is so intimately related to instruction that the generated. It was incorporated into the code generation phase. Whereas Machine independent optimization was done in a separate optimization phase.

Machine- independent optimization:

o When a subexpression occurs in a same statement more than once, we can delete all duplicate matrix entries and modify all references to the deleted entry so that they refer to the remaining copy of that subexpression as shown in following figure.

	operator	Operand1	Operand2	Matrix entries		operator	Operand1	Operand2	Matrix entries
1		START	FINISH	M1	1		START	FINISH	M1
2	*	RATE	M1	M2	2	*	RATE	M1	M2
3	*	2	RATE	M3	3	*	2	RATE	M3
4		START	FINISH	M4	4	-	START	FINISH	M4
5		M4	100	M5	5	-	M4	100	M5
6	*	M3	M5	M6	6	*	M3	M5	M6
7	+	M2	M6	M7	7	+	M2	M6	M7
8	=	COST	M7		8	=	COST	M7	

Matrix with common subexpressions Matrix with common subexpressions

Machine dependent optimization:

- If we optimize register usage in the matrix, it becomes machine dependent optimization.
- Following figure depicts the matrix that we previously optimized by eliminating a common subexpression (M4).
- Next to each matrix entry is a code generated using the operators.
- The third column is even better code in that it uses less storage and is faster due to a more appropriate mix of instructions.
- This example of machine-dependent optimization has reduced both the memory space needed for the program and the execution time of the object program by a factor of 2.
- Machine dependent optimization is typically done while generating code.



l	Г		Optimized Ma	atrix		First try		Improved	code				
					L	1, START	L	1, START					
		١.	START	FINISH	S	1, FINISH	s	1, FINISH	М1	→	R1		
	-	+			ST	1, M1	1-	-	+	\vdash	\vdash		
					L	1, RATE	L	3, RATE					
	:	2 *	RATE	M1	М	0, M1	MR	2, 1	M2	→	R3		
					ST	1, M2							
		4			T	1, =F'2'		5, = F'2'					
		3 *	2	RATE	L M	1,=F2* 0, RATE	L M	5, = F2 4, RATE	М3	→	R5		
					ST	1, M3							
	l F	4							-	\vdash	\vdash		
		+											
					L	1, M1							
		5 .	M1	100	S	1, =F*100'	s	1, =F'100'	M5	\rightarrow	R1		
					ST	1, M5							
		+	-		L	1,M3	LR	7,5	+	-	\vdash		
		6	M3	M5	M	0, M5	MR	6, 1	M6	→	R7		
	l F	*			ST	1, M6	-	-,-	-	-			
					L	1, M2							
		7 +	M2	M6	A	1, M6	AR	3, 7	М7	→	R3		
	-	+			L	1, M7 1, M7	ST	3, COST	+	-	\vdash		
		+			-	1, 111/	31	3, 0031	+	\vdash	\vdash		
		8 _	M7	COST	ST	1, COST							
					<u> </u>		<u> </u>						
4)	Expla	in fo	ur functi	on perfori	ned	by loader.							4M
	•			•		v							
	Loade	r Fui	nction : Th	ne loader p	erfo	orms the follo	wing	functions:					(Four
Ans:						ines and allo			memo	ry si	pace f	or the	functions
Ans:	[1] All	ocati	on The	iouaci act			Catos			J		-	
Ans:							cates	1					
Ans:	progra	m to	execute p	roperly.				_		ade i	n the	object	:1 ma
Ans:	progra	m to king	execute p	roperly.				nbolic referen		ade i	n the	object	
Ans:	progra 2) Lin modul	m to king es.	execute p The loa	oroperly. ader analys	ses a	and resolve t	he syn	nbolic referen	ices ma			-	:1 ma
Ans:	progra 2) Lin modul 3) Rel	m to king es. ocati	execute p The loa ion - The l	oroperly. nder analys oader map	ses a	and resolve to	he syn	_	ices ma			-	:1 ma
Ans:	progra 2) Lin modul 3) Rel newly	m to king es. ocati allo	execute properties on - The located mem	oroperly. nder analys oader map nory space	ses a s ar dur	and resolve to and relocates to ing execution	he syn he ado n.	nbolic referen	es to c	orre	spond	to the	:1 ma
Ans:	progra 2) Lin modul 3) Rel newly 4) Loa	m to king es. ocati alloo	execute process of the located memory of the	oroperly. ader analys oader map nory space oader actus	ses a os ar dur ally	and resolve to and relocates to ing execution loads the m	he syn he ado n. achine	nbolic reference code corres	es to cospondin	orre	spond the	to the	:1 ma
Ans:	progra 2) Lin modul 3) Rel newly 4) Loa	m to king es. ocati alloo	execute process of the located memory of the	oroperly. ader analys oader map nory space oader actus	ses a os ar dur ally	and resolve to and relocates to ing execution loads the m	he syn he ado n. achine	nbolic referen	es to cospondin	orre	spond the	to the	:1 ma
Ans:	progra 2) Lin modul 3) Rel newly 4) Loa	m to king es. ocati alloo	execute process of the located memory of the	oroperly. ader analys oader map nory space oader actus	ses a os ar dur ally	and resolve to and relocates to ing execution loads the m	he syn he ado n. achine	nbolic reference code corres	es to cospondin	orre	spond the	to the	:1 ma
Ans:	progra 2) Lin modul 3) Rel newly 4) Loa	m to king es. ocati alloo	execute process of the located memory of the	oroperly. ader analys oader map nory space oader actus	ses a os ar dur ally	and resolve to and relocates to ing execution loads the m	he syn he ado n. achine	nbolic reference code corres	es to cospondin	orre	spond the	to the	:1 ma
Ans:	progra 2) Lin modul 3) Rel newly 4) Loa	m to king es. ocati alloo	execute process of the located memory of the	oroperly. ader analys oader map nory space oader actus	ses a os ar dur ally	and resolve to and relocates to ing execution loads the m	he syn he ado n. achine	nbolic reference code corres	es to cospondin	orre	spond the	to the	:1 ma
Ans:	progra 2) Lin modul 3) Rel newly 4) Loa	m to king es. ocati alloo	execute process of the located memory of the	oroperly. ader analys oader map nory space oader actus	ses a os ar dur ally	and resolve to and relocates to ing execution loads the m	he syn he ado n. achine	nbolic reference code corres	es to cospondin	orre	spond the	to the	:1 ma
Ans:	progra 2) Lin modul 3) Rel newly 4) Loa	m to king es. ocati alloo	execute process of the located memory of the	oroperly. ader analys oader map nory space oader actus	ses a os ar dur ally	and resolve to and relocates to ing execution loads the m	he syn he ado n. achine	nbolic reference code corres	es to cospondin	orre	spond the	to the	:1 ma
Ans:	progra 2) Lin modul 3) Rel newly 4) Loa	m to king es. ocati alloo	execute process of the located memory of the	oroperly. ader analys oader map nory space oader actus	ses a os ar dur ally	and resolve to and relocates to ing execution loads the m	he syn he ado n. achine	nbolic reference code corres	es to cospondin	orre	spond the	to the	:1 ma
Ans:	progra 2) Lin modul 3) Rel newly 4) Loa	m to king es. ocati alloo	execute process of the located memory of the	oroperly. ader analys oader map nory space oader actus	ses a os ar dur ally	and resolve to and relocates to ing execution loads the m	he syn he ado n. achine	nbolic reference code corres	es to cospondin	orre	spond the	to the	:1 ma



5)	Draw the parse tree for the string 'acddf' using top down parsing approach.	4M
Ans:	String is "acddf" Assume: S→ xyz aBC B → c cd C → eg df Steps Assertion 1: acddf matches S Assertion 2: acddf matches xyz: Assertion is false. Try another. Assertion 3: cddf matches aBCi.ecddf matches BC: Assertion 4: ddf matches eg: False. Assertion 4: ddf matches df: False. Assertion 3: cddf matches cCi.edf matches C: Assertion 4: ddf matches df: False. Assertion 3: cddf matches cdCi.edf matches C: Assertion 4: df matches eg: False. Assertion 4: df matches df: Assertion 2 is true. Assertion 3 is true. Assertion 1 is true.	(Correct parse tree: 4marks)
	S S S S S S S S S S S S S S S S S S S	
	tree	

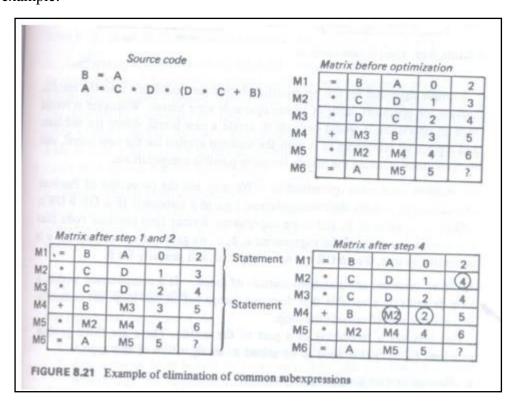


4.	a)	Attempt any three:	Marks 12				
	1)	Explain "compile and Go" loader scheme.	4M				
	Ans:	"Compile and go" loader: The instruction is read line by line, its machine code is obtained and it is directly put in the main memory at some known address. That means the assembler runs in one part of memory and the assembled machine instructions and data is directly put into their assigned memory locations. After completion of assembly process, assign starting address of the program to the location counter. The typical example is WATFOR-77, it's a FORTRAN compiler which uses such "load and go" scheme. This loading scheme is also called as "assemble and go".	, Diagram: 1mark)				
		Advantages:- 1. It is very easy to design and implementation. 2. Relocation can be perform by translator itself. 3. No object files are required. 4. It is suitable for experimental program language like Basic.					
		Disadvantages:- 1. For execute program it is necessary to compile a program every time. 2. It is very difficult to handle the multiple modules (Linking problem)					
		Source program deck Compile – & - Go Translator Program loaded a memory					
		Memory					
		Figure: Compile & Go Loader					
	2)	2) Explain any four optimization technique uses by compiler.					
	Ans:	The possible algorithm for four optimization techniques are as follows:- 1) Elimination of common sub expression 2) Compile time compute. 3) Boolean expression optimization. 4) Move invariant computations outside of loops. 1) Elimination of common sub expression: -The elimination of duplicate matrix entries	(Each technique: 1 mark)				
		can result in a more can use and efficient object program. The common subexpression must be identical and must be in the same statement.					



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- i. The elimination algorithm is as follows:-
- ii. Place the matrix in a form so that common subexpression can be recognized.
- iii. Recognize two subexpressions as being equivalent.
- Iv. Eliminate one of them.
- v. After the rest of the matrix to reflect the elimination of this entry. For example:-



2. Compile time compute:- Doing computation involving constants at compile time save both space and execution time for the object program.

The algorithm for this optimization is as follows:-

- i. Scan the matrix.
- ii. Look for operators, both of whose operands were literals.
- iii. When it found such an operation it would evaluate it, create new literal, delete old line
- iv. Replace all references to it with the uniform symbol for the new literal.
- v. Continue scanning the matrix for more possible computation.

For e.g.-

For e.g.- A = 2 * 276 / 92 * B

The compile time computation would be

Matrix Before optimization

M_1	*	2	276
M2	/	M_1	92
	*	M_2	В
M3			
	=	Α	M_3
M4			

Matrix After optimization

M_1			
M_2			
	*	6	В
M_3			
M_4	=	Α	M_3

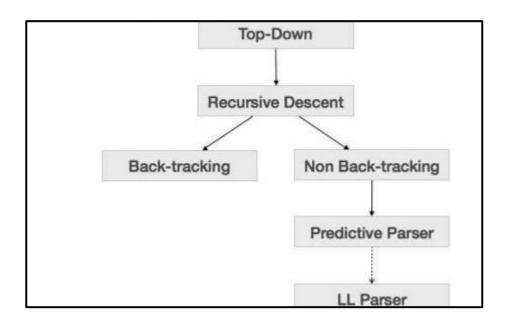
	3)Boolean expression optimization:- We may use the properties of boolean expression to shorten their computation.	
	e.g. In a statement	
	If a OR b Or c, Then when a, b & c are expression rather than generate code that will	
	always test each expression a, b, c. We generate code so that if a computed as true, then b	
	OR c is not computed, and similarly for b.	
	3) Move invariant computation outside of loops:- If computation within a loop depends on	
	a variable that does not change within that loop, then computation may be moved outside	
	the loop.	
	This requires a reordering of a part of the matrix. There are 3 general problems that need to be solved in an algorithm.	
	1. Recognition of invariant computation.	
	2. Discovering where to move the invariant computation.	
	3. Moving the invariant computation.	
	Original Code is:-	
	For y=0 to height-1	
	For $x=0$ to width-1	
	i=y*width+x	
	Process I	
	Next x Next y	
	here y*width is loop invariant not change in inner loop	
	Modified code is:-	
	For y=0 to height-1	
	temp= y*width	
	For x=0 to width-1	
	i=temp+x	
	Process i	
	Next x	
	Next y	
3)	Discuss memory allocation scheme used in compiler.	4M
Ans:	Storage Assignment: The purpose of this phase is as follows:-	(Explanati
	1. Assign storage to all variables referenced in the source program	on: 4
	2. Assign storage to all temporary locations that are necessary for intermediate result,	marks)
	e.g. the result of matrix lines. These storage references were reserved by the	
	interpretation phase and does not appear in the source code.	
	3. Assign storage to literals.	
	4. Ensure that the storage is allocated and appropriate locations are initialized	
	(literals and any variables with the initial attribute). Storage allocation phase does the following four steps:	
	1.Update the location counter with any necessary boundary alignment.	
	2. Assign the current value of the location counter to the address field of the variable.	
	3. Calculate the length of the storage needed by the variable.	
	4. Update the location counter by adding this length to it.	



4)	Explain predictive parsing with example.	4M	
Ans:	Predictive Parser: Predictive parser is a recursive descent parser, which has the capability to predict which production is to be used to replace the input string. The predictive parser does not suffer from backtracking. To accomplish its tasks; the predictive parser uses a look ahead pointer, which points to the next input symbols. To make the parser backtracking free, the predictive parser puts some constraints on the grammar and accepts only a class of grammar known as LL(k) grammar. Predictive parsing uses a stack and a parsing table to parse the input and generate a parse tree. Both the stack and the input contains an end symbol \$to denote that the stack is empty and the input is consumed. The parser refers to the parsing table to take any decision on the input and stack element combination. Exapmle:- Grammer: S → aBc B → bc b Input String: abc Fails, backtrack correct	(Description: 2marks, Example: 2 marks)	
b)	Attempt any one :	Marks 6	
1)	Explain four basic task of macroprocessor.	6M	
	The 4 basic task of Macro processor is as follows:- 1) Recognize the macro definitions. 2) Save the Macro definition. 3) Recognize the Macro calls. 4) Perform Macro Expansion. 1) Recognize the Macro definitions:- A microprocessor must recognize macro definitions identified by the MACRO and MEND pseudo-ops. When MACROS and MENDS are nested, the macro processor must recognize the nesting and correctly match the last or outer MEND with the first MACRO.	(List:2 marks, Each task descriptio n:1 mark)	

		MDT			
	Macro Definition Table & LAB INCR & ARG1,&ARG2,&ARG3				
	#0	A	& ARG1,&ARG2,&ARG3 1, #1		
	#0	A	2,#2		
		A	3,#3		
		MEND	2,2		
		e later required for ex	processor must save the macro inspanding macro calls.	structions	
		Macr	Name Table		
	1	"INCRbbbb"	15		
	•		•		
	•				
	•	•	•		
	•		•		
			ear as operation mnemonics in a prog		
	Index	Argume	nt		
	0		bb" (all Blank)		
	1	"Data31			
	2	"Data2h			
	3	"Data11	bb"		
	1	ponding arguments fr	cessor must substitute for macro com a macro call, the resulting symbol		
2)	Explain following p i) Top-down parsing ii) Bottom up parsin		letail.	6M	
Ans:	Top-down Parser: When the parser starts constructing the parse tree from the start symbol and then tries to transform the start symbol to the input, it is called top-down parsing. The types of top-down parsing are depicted Below:				

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Recursive Descent Parsing: Recursive descent is a top-down parsing technique that constructs the parse tree from the top and the input is read from left to right. It uses procedures for every terminal and non-terminal entity. This parsing technique recursively parses the input to make a parse tree, which may or may not require back-tracking. But the grammar associated with it (if not left factored) cannot avoid back-tracking. A form of recursive-descent parsing that does not require any back-tracking isknown as predictive parsing. This parsing technique is regarded recursive as it uses context-free grammar which is recursive in nature.

Backtracking: It means, if one derivation of a production fails, the syntax analyzer restarts the process using different rules of same production. This technique may process the input string more than once to determine the right production. Top-down parsing technique parses the input, and starts constructing a parse tree from the root node gradually moving down to the leaf nodes.

Top- down parsers start from the root node (start symbol) and match the input string against the production rules to replace them (if matched).

The following example of CFG:

 $S \rightarrow rXd|rZd$

X →oa|ea

Z →ai

For an input string: read, a top-down parser, will behave like this: It will start with S from the production rules and will match its yield to the left-most letter of the input, i.e. 'r'. The very production of S (S \rightarrow rXd) matches with it. So the top-down parser advances to the next input letter (i.e. 'e'). The parser tries to expand non-terminal 'X' and checks its production from the left (X \rightarrow oa). It does not match with the next input symbol. So the



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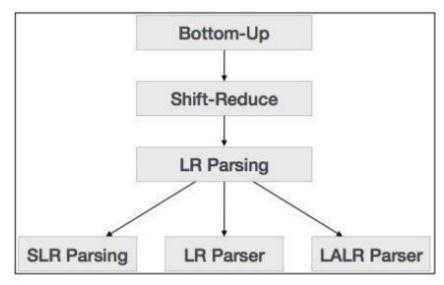
top-down parser backtracks to obtain the next production rule of X, $(X \rightarrow ea)$. Now the parser matches all the input letters in an ordered manner. The string is accepted.

Predictive Parser: Predictive parser is a recursive descent parser, which has the capability to predict which production is to be used to replace the input string. The predictive parser does not suffer from backtracking. To accomplish its tasks; the predictive parser uses a look-ahead pointer, which points to the next input symbols. To make the parser backtracking free, the predictive parser puts some constraints on the grammar and accepts only a class of grammar known as LL(k) grammar. Predictive parsing uses a stack and a parsing table to parse the input and generate a parse tree. Both the stack and the input contains an end symbol \$to denote that the stack is empty and the input is consumed. The parser refers to the parsing table to take any decision on the input and stack element combination.

LL Parser: An LL Parser accepts LL grammar. LL grammar is a subset of context-free grammar but with some restrictions to get the simplified version, in order to achieve easy implementation. LL grammar can be implemented by means of both algorithms namely, recursive-descent or table-driven. LL parser is denoted as LL(k). The first L in LL(k) is parsing the input from left to right, the second L in LL(k) stands for left-most derivation and k itself represents the number of look ahead. Generally k = 1, so LL(k) may also be written as LL(1).

Bottom-up Parser:

Bottom-up parsing starts from the leaf nodes of a tree and works in upward direction till it reaches the root node. Here, we start from a sentence and then apply production rules in reverse manner in order to reach the start symbol. The image given below depicts the bottom-up parsers available.



Shift-Reduce Parsing

Shift-reduce parsing uses two unique steps for bottom-up parsing. These steps are known as shift-step and reduce-step. Shift step: The shift step refers to the advancement of the input pointer to the next input symbol, which is called the shifted symbol. This symbol is pushed onto the stack. The shifted symbol is treated as a single node of the parse tree. Reduce step: When the parser finds a complete grammar rule RHS and replaces it to LHS.

Reduce step: When the parser finds a complete grammar rule RHS and replaces it to LHS, it is known as reduce-step. This occurs when the top of the stack contains a handle. To reduce, a POP function is performed on the stack which pops off the handle and replaces it with LHS non-terminal symbol.

		LR Parser The LR parser is a non-recursive, shift-reduce, bottom-up parser. It uses a wide class of context- free grammar which makes it the most efficient syntax analysis technique. LR parsers are also known as LR parsers, where L stands for left-to-right scanning of the input stream; R stands for the construction of right-most derivation in reverse, and k denotes the number of lookahead symbols to make decisions. There are three widely used algorithms available for constructing an LR parser: SLR1 – Simple LR Parser: o Works on smallest class of grammar o Few number of states, hence very small table o Simple and fast construction LR1 – LR Parser: o Works on complete set of LR1 Grammar o Generates large table and large number of states o Slow construction LALR1 – Look-Ahead LR Parser: o Works on intermediate size of grammar o Number of states are same as in SLR1	
5.		Attempt any two:	Marks 16
	1)	Explain design of direct linking loader.	8M
	Ans:	{**Note: Flow charts are optional**}	(Each step: 2marks)
		Direct Linking Loader generates relocatable loader and is most popular load scheme presently used.	
		Direct Linking loaderIt allow programmer to used multiple procedure and multiple data segments. This is possible due to assembler provides following information	
		A.The length of segment. B.List of symbol, define in one segment and call in other segment. C.List of symbol, not define in segment but call in segment. D.Information about address located in segment. E.Machine code of program and relative address assigned.	
		Step 1. Specification of problems Step 2. Specification of data structure Step 3. Format of data structure Step 4: Algorithm	
		 Specification of problems: There will be 4 different card format in a object desk. ESD:This card contain the information necessary for the building symbol table. TXT:This card contain instruction and data card called "text" of programe. RLD:Relocation and linking directory cards END:End card 	

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2. Specification of data structure:

Pass-1

- 1. Input object deck
- 2. IPLA-Initial Program Load Address supplied by program's or OS.
- 3. PLA-Program load address counter, to keep track of each segment
- 4. GEST-Global External Symbol Table, to store each external symbol & its corresponding core add.
- 5. A copy of program to be used by Pass-2.
- 6. LOAD MAP-Printed listing, that specifies each external symbol & it's assigned value.

Pass-2

- 1. Copy of object program inputted by Pass-1.
- 2. IPLA-Initial Program Load Address supplied by program's or OS.
- 3. PLA-Program load address counter, to keep track of each segment
- 4. GEST-Global External Symbol Table, to store each external symbol & its corresponding core add.
- LESA-Local External Symbol Array, which is used establish correspondences between ESD Id and Absolute address value.

3. Format of Data bases:

Format of databases is to specify the format and content of following data bases.

- 1. ESD
- 2. TXT
- 3. RLD
- 4. END
- 5. GEST
- 6. LESA

4. Algorithm:

Following are the steps of an Algorithm for direct linking loader

Pass1:

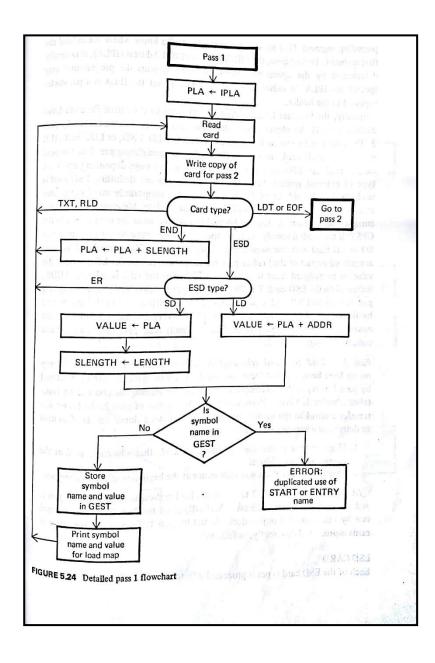
- a. Allocate Segments
 - i. Initial Program Load Address (IPLA)
 - ii. Assign each segment the next table location after the preceding segment.
- b. Define Symbols
 - i. SD
 - ii. LD
 - iii. ER

Pass2:

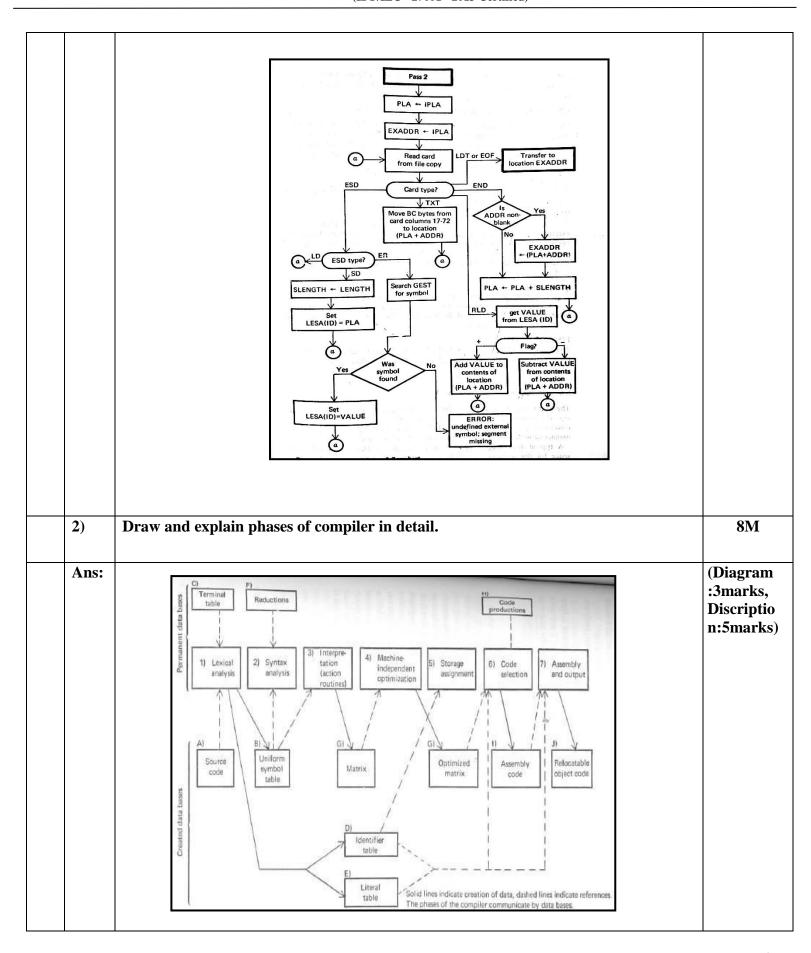
- a. ESD record types is processed differently.
- b. TXT is copied from the record to the relocated core location (PLA + ADDR).
- e. RLD value to be used for relocation and linking is extracted from the GEST.



- d. The relocated address of the address constant is the sum of the PLA and the ADDR field specified on the RLD record.
- e. END execution start address is relocated by the PLA
- f. The loader transfers control to the loaded program at the address specified by current contents of the execution



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1) Lexical Phase:-

- Its main task is to read the source program and if the elements of the program are correct it generates as output a sequence of tokens that the parser uses for syntax analysis.
- The reading or parsing of source program is called as scanning of the source program.
- It recognizes keywords, operators and identifiers, integers, floating point numbers, character strings and other similar items that form the source program.
- The lexical analyzer collects information about tokens in to their associated attributes.

2) Syntax Phase:-

- In this phase the compiler must recognize the phases (syntactic construction); each phrase is a semantic entry and is a string of tokens that has meaning, and 2nd Interpret the meaning of the constructions.
- Syntactic analysis also notes syntax errors and assure some sort of recovery. Once the syntax of statement is correct, the second step is to interpret the meaning (semantic). There are many ways of recognizing the basic constructs and interpreting the meaning.
- Syntax analysis uses a rule (reductions) which specifies the syntax form of source language.
- This reduction defines the basic syntax construction and appropriate compiler routine (action routine)to be executed when a construction is recognized.
- The action routine interprets the meaning and generates either code or intermediate form of construction.

3) Interpretation Phase:-

• This phase is typically a routine that are called when a construct is recognized. The purpose of these routines is to on intermediate form of source program and adds information to identifier table.

4) Code optimization Phase:-

 Two types of optimization is performed by compiler, machine dependent and machine independent. Machine dependent optimization is so intimately related to instruction that the generated. It was incorporated into the code generation phase.
 Where Machine independent optimization is was done in a separate optimization phase.

5) Storage Assignment:-

The purpose of this phase is as follows: -

- Assign storage to all variables referenced in the source program.
- Assign storage to all temporary locations that are necessary for intermediate results.
- Assign storage to literals.
- Ensure that storage is allocated and appropriate locations are initialized.

6) Code generation:-

• This phase produce a program which can be in Assembly or



	machine language.				
	This phase has matrix as input.				
	• It uses the code production in the matrix to produce code.				
	•				
	It also references the identifier table in order to generate address & code conversion.				
	7) Assembly phase:-				
	• The compiler has to generate the machine language code for computer to understand.				
	• The task to be done is as follows:-				
	o Generating code Resolving all references.				
	O Defining all labels.				
	Resolving literals and symbolic table.				
3)	Explain general design procedure of Assembler.	8M			
Ans:	Following are six steps for the General Design procedure of an Assembler.	(List:2			
	1. Specify the problem	marks,			
	2. Specify data structures	Explainat			
	3. Define format of data structures	on:			
	4. Specify algorithm	6marks fo			
	5. Look for modularity	all steps)			
	6. Repeat 1 to 5 on modules				
	1. Specify the problem.				
	This includes translating assembly language program into machine				
	language program using two passes of assembler. Purpose of two passes of				
	assembler are to determine length of instruction, keep track of location				
	counter, remember values of symbol, process some pseudo ops, lookup				
	values of symbols, generate instructions and data, etc.				
	2. Specify data structures.				
	This includes establishing required databases such as Location counter(LC),				
	machine operation table (MOT), pseudo operation table (POT), symbol				
	table(ST), Literal Table(LT), Base Table (BT), etc.				
	3. Define format of data structures.				
	3. Define format of data structures. This includes specifying the format and content of each of the databases – a				
	This includes specifying the format and content of each of the databases – a				
	This includes specifying the format and content of each of the databases – a task that must be undertaken before describing the specific algorithm underlying the assembler design.				
	This includes specifying the format and content of each of the databases – a task that must be undertaken before describing the specific algorithm				

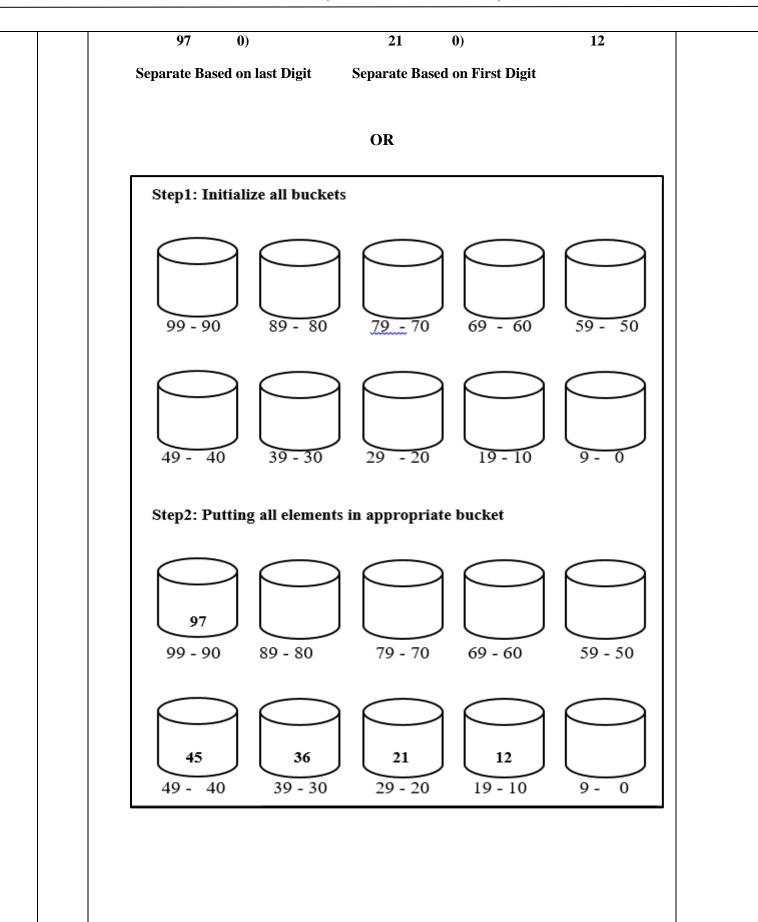


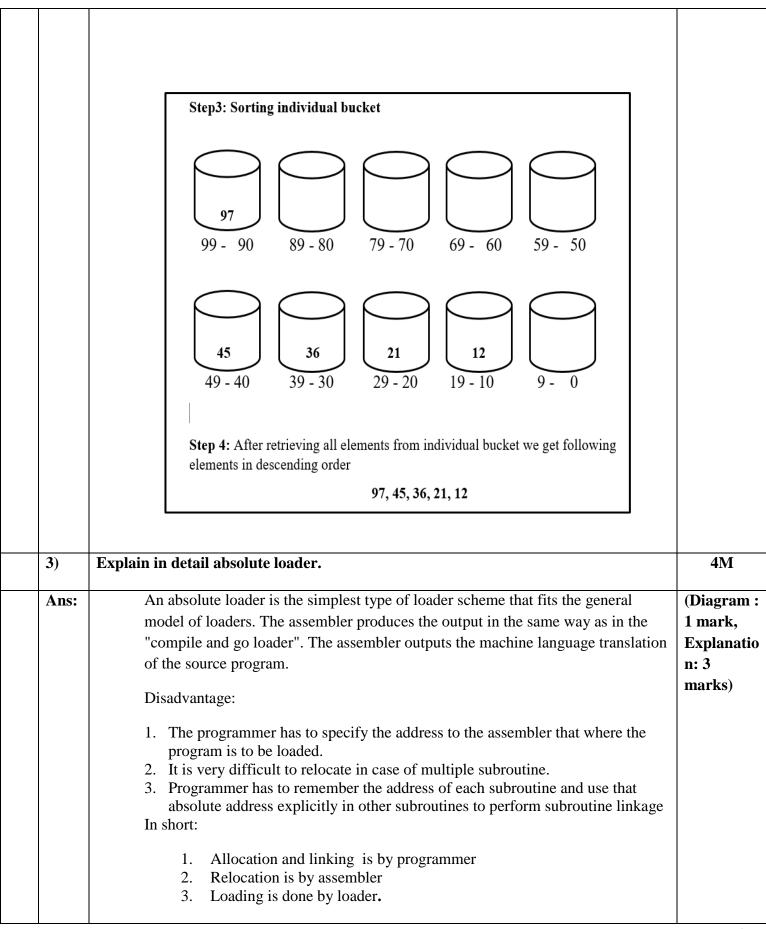
		5. Look for modularity. This includes review design, looking for functions that can be isolated. Such functions fall into two categories: 1) multi-use 2) unique.			
		6. Repeat 1 to 5 on modules.			
·		Attempt any four :	Marks 16		
	1)	Explain implementation of Macro call within Macro.	4M		
	Ans:	Macro calls are "abbreviations" of instruction sequences, it seems reasonable that such abbreviations should be available within other macro definitions. For example, MACRO ADD1 &ARG L 1, &ARG A 1, =F"1" ST 1, &ARG MEND MACRO ADDS &ARG1, &ARG2, &ARG3 ADD1 &ARG1 ADD1 &ARG2 ADD1 &ARG2 ADD1 &ARG3	(Explanation: 3 marks, Example: 1 mark)		
		MEND Macro Within the definition of the macro "ADDS" are three separate calls to a previously defined macro "ADD1". The use of the macro "ADD1" has shortened the length of the definition of "ADDS" and thus had made it more easily understood. Such use of macros result in macro expansions on multiple "levels".			

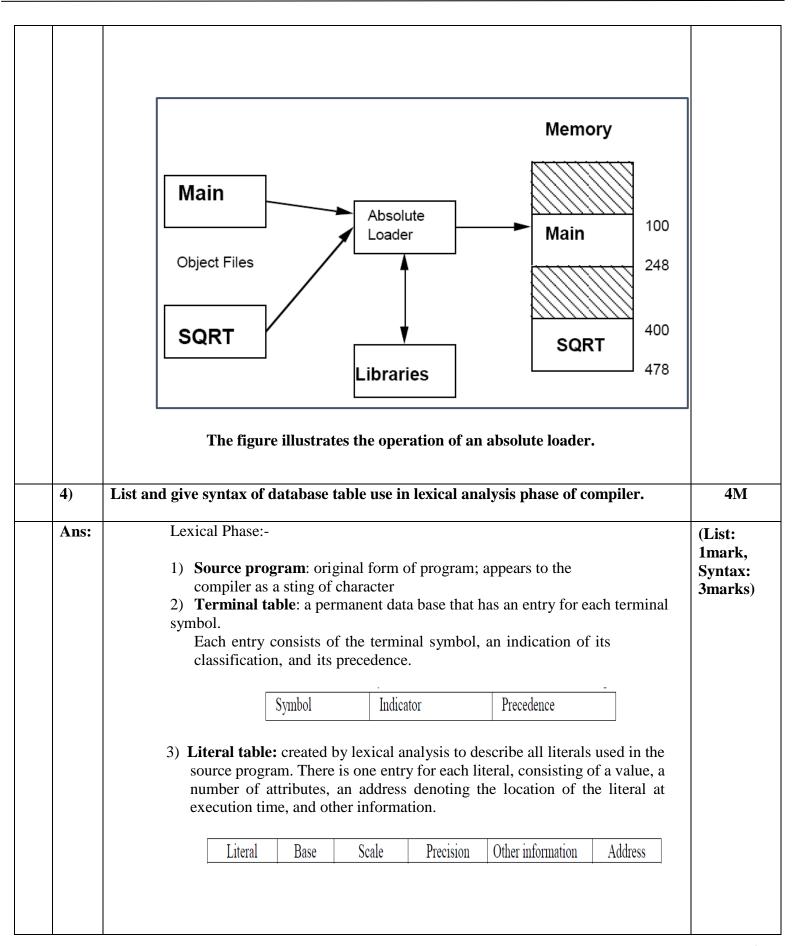


	A-D	MACRO ADD L 4ARG MEND ADD L 4ARG MEND ADD L 4ARG ADD L 4ARG MEND ADD L 4ARG MEND ADD L 4ARG MEND DATA 1 DC DATA 2 DC DATA 3 DC	1	nded source 1 evel 1) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Expanded si (Level2 Liparal A 1,=f'i', ST 1,DATA! Liparal Liparal Liparal Liparal Liparal A 1,=f'i' ST 1,DATA! DATA 1. DC DATA 2. DC	F ADD 1 2-3 13 P'r'	
2)	Sort the	following 6	element in descend	ling order usi	V DATA3 DC	F 151	4M
2) Ans:	45, 21, 1	2, 36, 97 Original	element in descend First Distribution	ling order usi	ing Bucker sort.	F 151	4M (Each distributio n :2marks)
	45, 21, 1	2, 36, 97	First Distribution		ing Bucker sort. Second Distribution	f'si.	(Each
	45, 21, 1	Original table	First Distribution 9)	Merge	ing Bucker sort. Second Distribution 9) 97	Final Merge	(Each distributio
	45, 21, 1	2, 36, 97 Original	First Distribution 9) 8)		Second Distribution 9) 97 8)	f'si.	(Each distributio
	45, 21, 1	Original table	First Distribution 9) 8) 7) 97	Merge 97	Second Distribution 9) 97 8) 7)	Final Merge	(Each distributio
	45, 21, 1	Original table	First Distribution 9) 8) 7) 97 6) 36	Merge	Second Distribution 9) 97 8) 7) 6)	Final Merge	(Each distributio
	45, 21, 1	Original table 45	First Distribution 9) 8) 7) 97 6) 36 5) 45	Merge 97	Second Distribution 9) 97 8) 7) 6) 5)	Final Merge	(Each distributio
	45, 21, 1	Original table	First Distribution 9) 8) 7) 97 6) 36 5) 45 4)	Merge 97 36	Second Distribution 9) 97 8) 7) 6)	Final Merge 97 45	(Each distributio
	45, 21, 1	Original table 45	First Distribution 9) 8) 7) 97 6) 36 5) 45	Merge 97 36	Second Distribution 9) 97 8) 7) 6) 5) 4) 45	Final Merge 97 45	(Each distributio









	4) Identifier Table: created by lexical analysis to describe all identifiers used in the source program. There is one entry for each identifier. Lexical analysis creates the entry and places the name of identifier into that entry. The pointer points to the name in the table of names. Later phases will fill in the data attributes and address of each identifier Name Data attributes address 5) Uniform Symbol table: created by lexical analysis to represent the	
	program as a string of tokens rather than of individual characters. Each uniform symbol contains the identification of the table of which a token is a member	
	Table Index	
5)	Explain the format of databases of loader.	4M
Ans:	 External Symbol Dictionary (ESD) record: Entries and Externals (TXT) records control the actual object code translated version of the source program. The Relocation and Linkage Directory (RLD) records relocation information The END record specifies the starting address for execution IPLA-Initial Program Load Address supplied by program's or OS. PLA-Program load address counter, to keep track of each segment GEST-Global External Symbol Table, to store each external symbol & its corresponding core add. LESA-Local External Symbol Array, which is used establish correspondences between 	Listing of latabases 2 marks, any two ormats: 2 marks)
	Symbol type Rel- symbol type location Length JOHN SD 0 64 RESULT LD 52 SUM ER — —	
	RLD record	
	Symbol Flag Length location JOHN + 4 48 SUM + 4 56	
	TXT record	