WINTER– 17 EXAMINATION

Subject Name: Principles of Digital Techniques **Model Answer** Subject Code: 17320

Important Instructions to examiners:

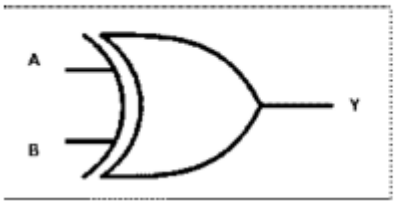
1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

1. a) Attempt any SIX of the following: **Marks 12**

(i) Draw symbol of EXOR gate and also write its truth table.

Ans:- (Symbol-1 mks, truth table- 1mks)

Symbol



$A \cdot \overline{B} + \overline{A} \cdot B$

Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(ii) Identify the functions of IC 0800 and IC 0809.

Ans:- (Functions-1 mks each)

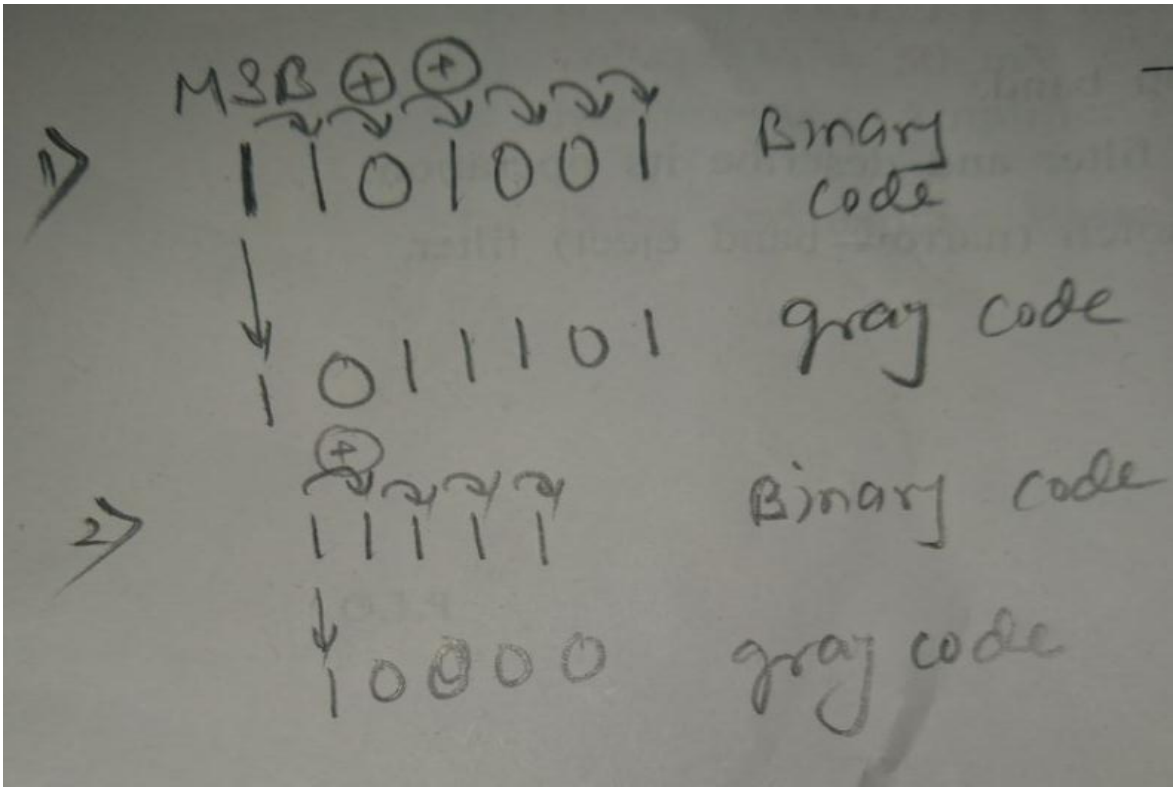
1) 0800-8 bit ADC IC
2) 0809-8 Bit DAC IC

(iii) Convert the following binary number to gray code:

1) 1101001

2) 11111

Ans:- (Each conversion - 1mks each)



(iv) What is the role of Present and clear terminal of flip-flop?

Ans:- (Role of each terminal, 1 mkseach)

In the Flip-flop when the power is switched ON, the state of the circuit is uncertain.
It may be set (Q=1) or reset (Q=0) state.
In many applications it is desired to initially set or reset the flip-flop i.e. the initial state of flip-flop is to be assigned. This is done by using preset (Pr) & clear (Cr) inputs.
There inputs may be applied at any time between clock pulses & are not in synchronism with the clock.
Truth Table with Preset & Clear I/P.

Input			Output	Operation
CLK	Cr	Pr	Q	preformed
1	1	1	Q_{n+1}	Normal FF
×	0	1	0	FF is reset
×	1	0	1	FF is set

So, the O/P of the flip-flop changes whenever a clock signal is applied, it is necessary to set the output or reset the output i.e. to start with some definite intial state,then two additional inputs Preset & Clear are used.
These inputs sets or resets the flip-flop independent of clock.

(v) Compare TTL and CMOS Logic families. (2 points)

Ans:-(Relevant 2points of comparison- 1 mks for each point)

Parameters	CMOS	TTL
Device used	P- Channel & N-Channel MOSFET	BJT (transistor)
Noise Margin	1.45 v	0.4v
Noise immunity	Better than TTL	Less than CMOS
Propagation delay	105 nsec	10 nsec
Switching speed	Less than TTL	Faster than CMOS
Power dissipation	Less 0.1 mW	More 10 mW
Fan out	50	10
Unused input	Connect to ground or VCC	Input can remain floating & treated as logic 1
Operating region	Ohmic & cutoff region	Saturation or cutoff region
Component density	Need Smaller space	Need more space than CMOS

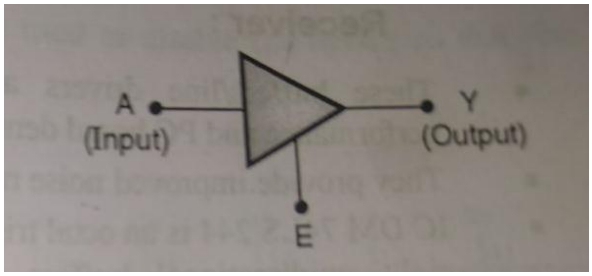
(vi) What is Tristate buffer? Draw its symbol.

Ans:- (Definition- 1 mks, symbol-1 mks)

Tristate logic :- A tristate logic is a logical circuit that has three possible output states ie.

1) Logic 0
2) Logic 1 and
3) High impedance state

Symbol



(vii) Define modulus of counter? How many flip flops are required for mod 5 counter?

Ans:- (Definition-1 mks, no. of flipflops required used -1 mks)

Modulus of a counter is defined as the no. of states or count through which the counter can progress. It depends on the no. of flipflops 'N' used . For 'N' no of flipflops used modulus or MOD is , MOD =2N .

$N \leq 2^m$ where N= no of states of counter

m= no of flip flops required.

$5 \leq 2^m$ ….. for mod 5 counter; N= 5

Therefore, m= 3

Ans: 3 flip flops are required for mod 5 counter.

(viii) State the necessity of multiplexer.

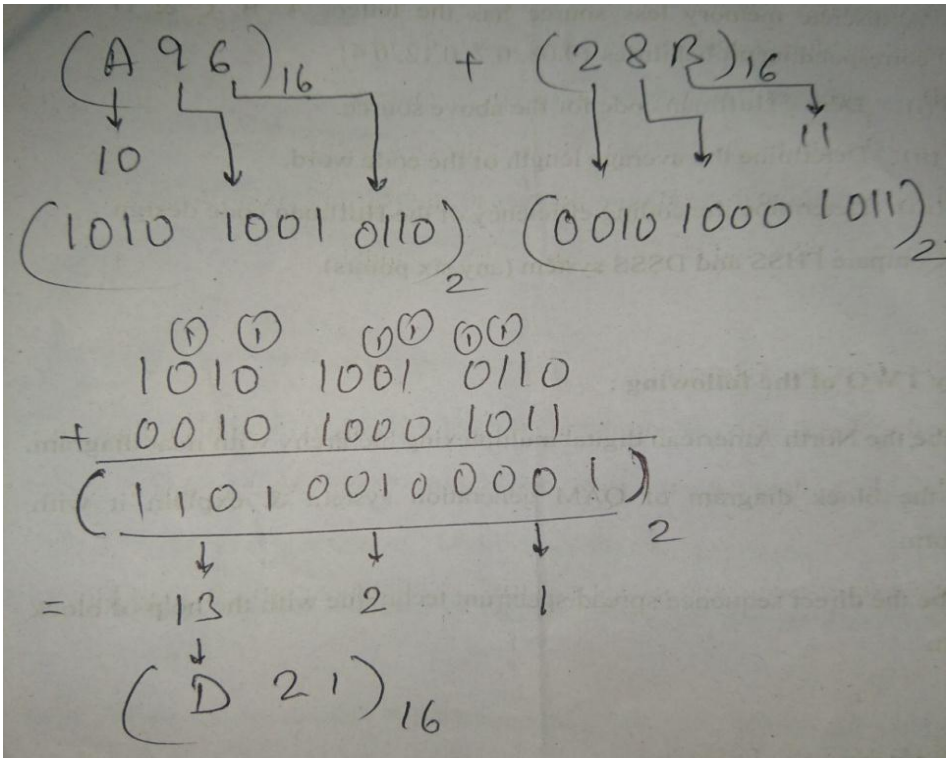
Ans:- (Need 2 points , 1 mks each)

- In most of the electronic systems, the digital data is available on more than one lines. It is necessary to route this data over a single line.
- Under such circumstances we require a circuit which select one of the many inputs at a time.
- This circuit is nothing else but a multiplexer which has many inputs, one output and some select inputs.
- Multiplexer improves the reliability of the digital system because it reduces the number of external wired connections.

b) Attempt any <u>TWO</u> of the following: **Marks 8**

(i) Convert the following into Binary and Add them $(A96)_{16} + (28B)_{16}$

Ans:- (Correct answer – 4 mks)



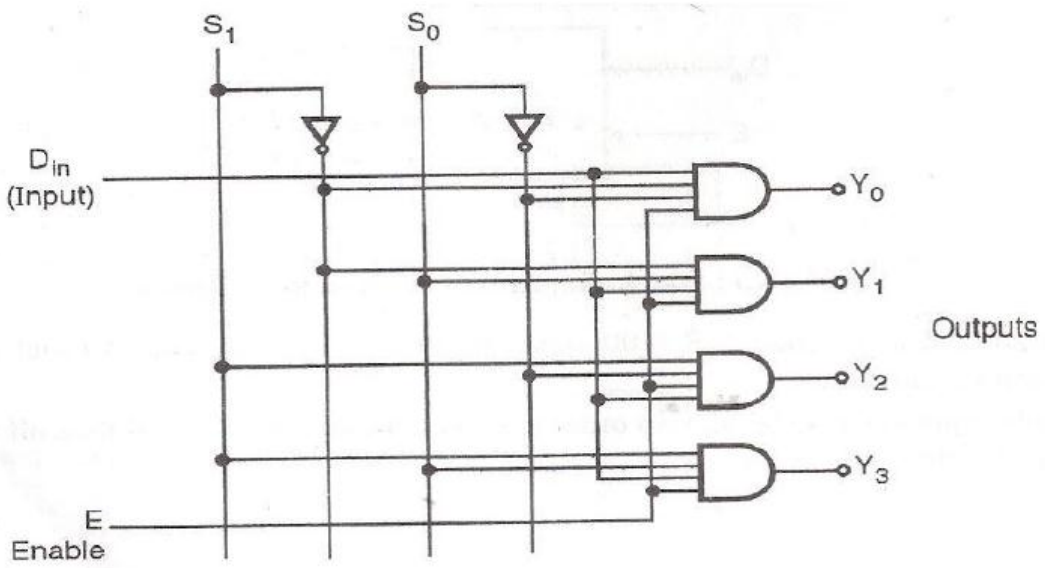
(ii) Differentiate between Synchronous and Asynchronous counter.

Ans:- (4 points of differentiation- 4 mks)

Parameters	Synchronous counter	Asynchronous counter
Definition	Clock pulses are applied simultaneously	Clock pulses are applied to first flipflop, output of first flipflop acts as clock pulses for next and so on.
Design Complexity	simple	complicated
Propagation Delay /speed	Less delay so more speed	More delay so less speed
Applications	High frequency applications	Low frequency applications
Problem of glitches	Absent	Present

(iii) Draw circuit diagram of 1:4. Demux using logic gate. Write its truth table.

Ans:- (Circuit diagram using gates-2 mks, truth table- 2 mks)



Truth table 1:4 demux

E	S0	S1	Y0	Y1	Y2	Y3
0	X	X	0	0	0	0
1	0	0	D	0	0	0
1	0	1	0	D	0	0
1	1	0	0	0	D	0
1	1	1	0	0	0	D

2. Attempt any <u>Four</u> of the following: **Marks 16**

a) Compare EPROM and flash memory.

Ans:- (4 points of comparison- 4 mks)

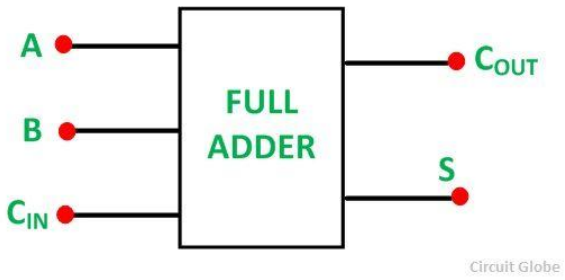
Sr.No	Parameter	EPROM	Flash
1	Type	Non- volatile	Non- Volatile
2	Erasing Technique	Exposure to UV rays	Electrically
3	Time for erasing	Long 10 to 15 min	Instantly
4	Need to remove memory from the circuit	It is necessary to remove EPROM from the circuit for erasing.	Not necessary to remove from the circuit for erasing
5	Way of erasing	All the data gets erased	Selective erasing is possible.
6	Applications	In computer to store the operating system	Cell phones, digital camera etc.

b) Describe operation of full adder with proper truth table and logical diagram.

Ans:- (Diagram- 2mks,truth table – 1mks, Theory/operation- 1mks)

A full adder is a combinational logic circuit that performs addition between three bits, the two input bits A and B, and carry C from the previous bit.

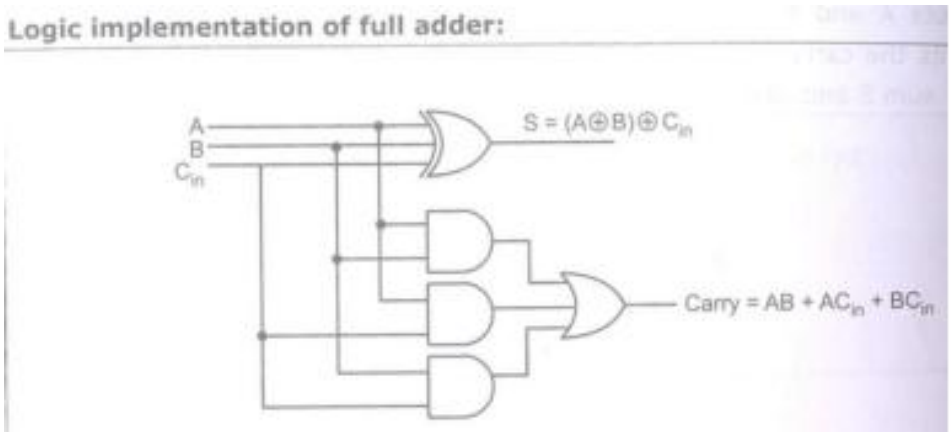
Block diagram



Truth Table

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Circuit diagram using gates

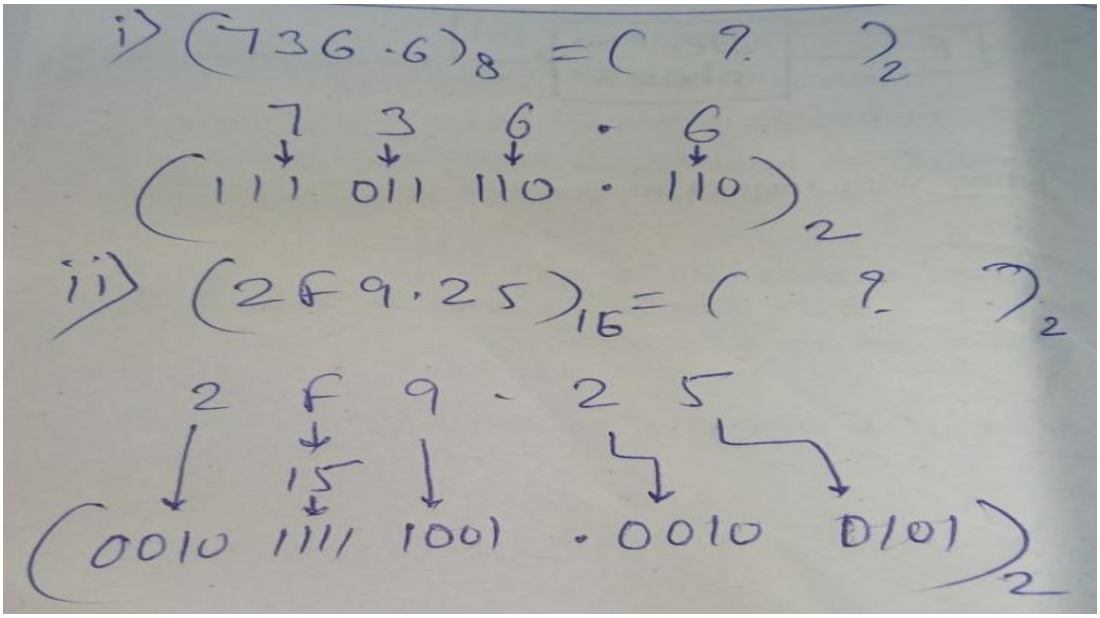


c) Convert the following number into Binary:

(i) $(736.6)_8$

(ii) $(2F9.25)_{16}$

Ans:- (Each correct conversion – 2 mks)



d) State and prove De Morgan's Theorems.

Ans:- (Each state and proof using table- 2 mks each)

i) $\overline{AB} = \overline{A} + \overline{B}$

It states that compliment of product is equal to sum of their compliments.

1	2	3	4	5	6
A	B	$\overline{AB}$	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

Column 03 = column 06

i.e. $\overline{AB} = \overline{A} + \overline{B}$

Hence proved

ii) $\overline{A+B} = \overline{A} \cdot \overline{B}$

It states that complement of sum is equal to product of their complements.

1	2	3	4	5	6
A	B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

Column 03 = column 06

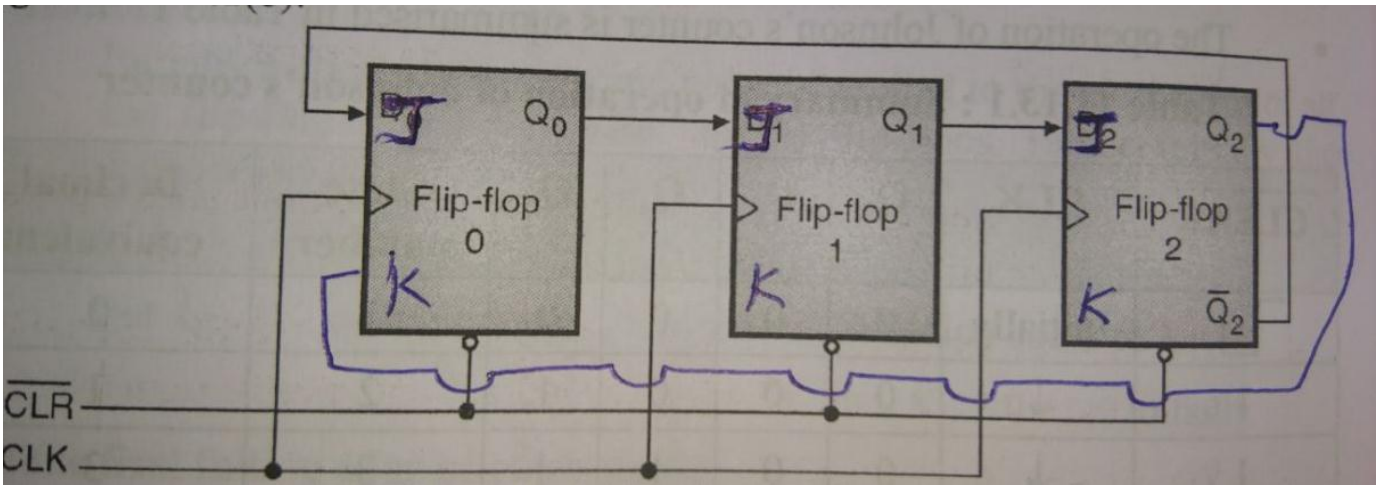
$\therefore \overline{A+B} = \overline{A} \cdot \overline{B}$

Hence proved.

e) Draw the diagram of 3-bit twisted ring counter using JK F/F. Also write its truth table. Draw waveforms.

Ans:- (Diagram- 2 mks, truth table-1 mks, waveforms-1 mks)

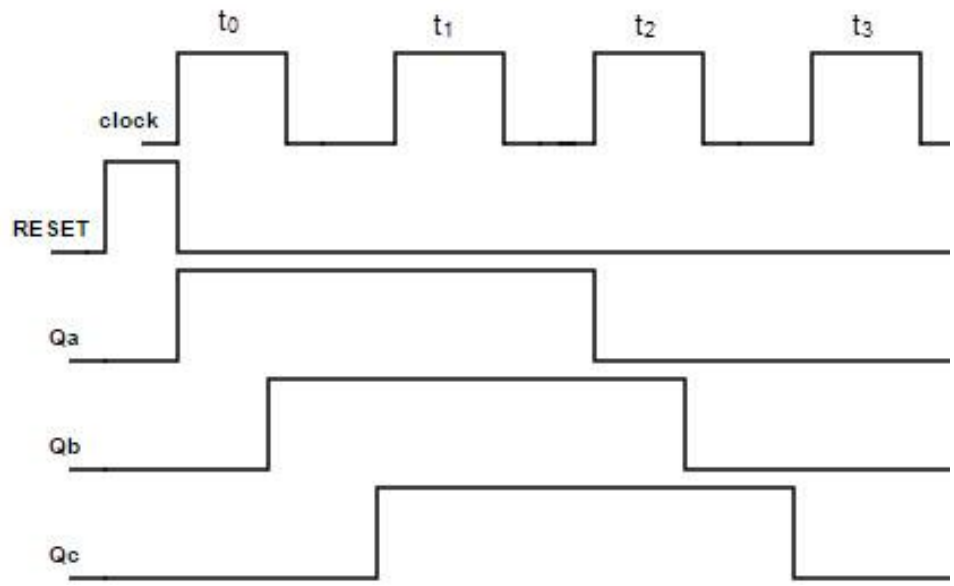
Diagram



Truth table

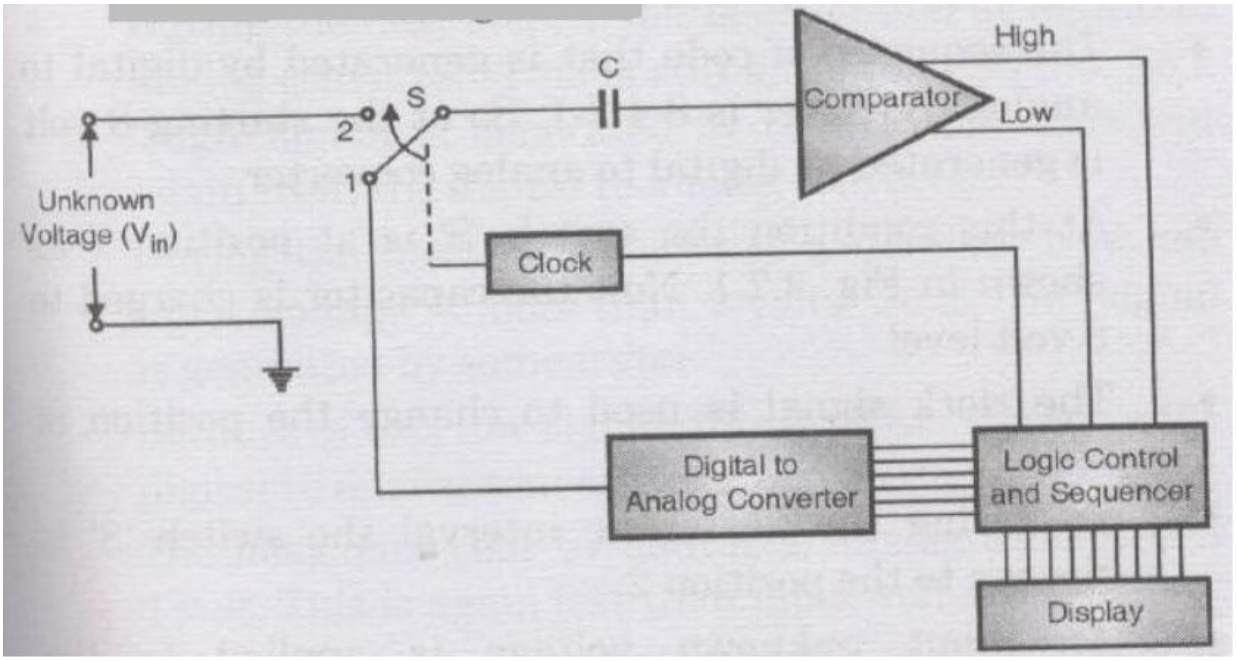
Clear	CLK	Q_2	Q_1	Q_0	$Q_0 = \overline{Q}_2$
⊓	Initially	0	0	0	1
1	↑	0	0	1	1
1	↑	0	1	1	1
1	↑	1	1	1	0
1	↑	1	1	0	0
1	↑	1	0	0	0
1	↑	0	0	0	1

Waveforms



f) Draw the block diagram of successive approximation type ADC and explain its working.

Ans:- (Block diagram- 2 mks, working- 2 mks)



DAC = Digital-to-Analog converterEOC = end of conversion
SAR = successive approximation register
S/H = sample and hold circuit
V_{in} = input voltage
V_{ref} = reference voltage

The successive approximation Analog to digital converter circuit typically consists of four chief sub circuits:

1. A sample and hold circuit to acquire the input voltage (V_{in}).
2. An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register(SAR).
3. A successive approximation register sub circuit designed to supply an approximate digital code of V_{in} to the internal DAC.
4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with V_{in}.

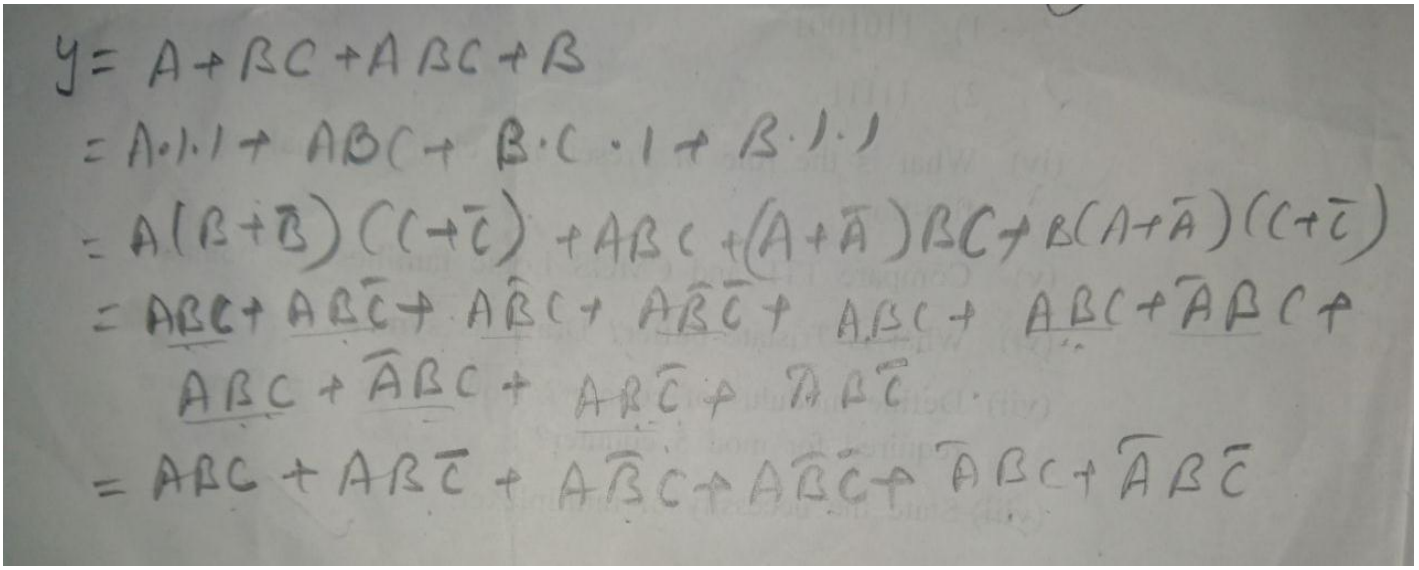
The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing

this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC).

3. Attempt any <u>Four</u> of the following: **Marks 16**

a) Convert the following expression into their standard SOP form Y – A + BC + ABC + B .

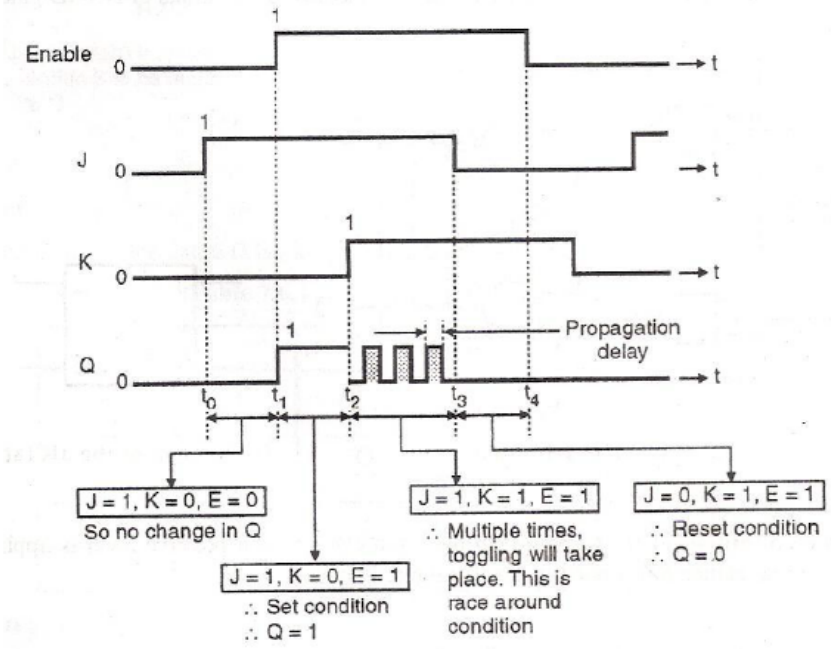
Ans:- (correct conversion- 4 mks)



b) What is Race around condition and how it is eliminated?

Ans:- (Race around condition- 2 mks, methods to eliminate – 2 mks)

Race around condition occurs in J K Flipflop only when J=K=1 and clock/enable is high (logic 1) as shown below-



Explanation:-In JK Flip-flop when J=K=1 and when clock goes high, output should toggle (change to opposite state) ,but due to multiple feedback output changes/toggles many times till the clock/enable is high. Thus toggling takes place more than once, called as racing or race around condition. Thus to avoid RAC following methods can be used-

1. Design the clock with time less than toggling time (this method is not economical)
2. Use edge triggering.
3. Use Master Slave J K Flip-flop.

c) Solve the following using 1^s and 2^s complement method.

(i) $(42)_{10} - (63)_{10}$

(ii) $(11010)_2 - (11100)_2$

Ans:- (Each conversion -1 mks)

i) $(42)_{10} = (101010)_2 = A$

$(63)_{10} = (111111)_2 = B$

(a) using 1's comp method

1) find 1's comp of B

111111 — 000000

2) add to A

$$\begin{array}{r} 101010 \\ +000000 \\ \hline 101010 \end{array}$$

3) As carry is not generated, result is negative, but in 1's comp form - so result is -

$101010 \rightarrow (010101)_2$

$= (-21)_{10}$

ii) $(42)_{10} = (101010)_2 = A$

$(63)_{10} = (111111)_2 = B$

(A) using 2's comp method

1) find 2's comp of B

$111111 \rightarrow 000000$

$+ \quad 1$

000001

2) add to A

101010

$+ 000001$

101011

2) As carry is not generated, result is negative, but in 2's comp form - so the result is -

$101011 \rightarrow 010100$

$+ \quad 1$

010101

ie $(-21)_{10}$

ii) $(11010)_2 - (11100)_2$

$A = (11010)_2$

$B = (11100)_2$

a) using 1's comp method

1) find 1's comp of B

11100 → 00011

2) add to A

$$\begin{array}{r} {\scriptstyle 1}\\ 11010 \\ +\ 00011 \\ \hline 11101 \end{array}$$

3) As carry is not generated result is negative but in 1's comp form. So the result is -

11101 → 00010

$-(2)_{10}$

(b) using 2's comp method

1) find 2's comp of B

$$11100 \rightarrow 00011$$
$$+\ 1$$
$$00100$$

2) add to A

$$\begin{array}{r} 11010 \\ +\ 00100 \\ \hline 11110 \end{array}$$

3) As carry is not generated, result is negative, but in 2's comp. form. So the result is -

$$11110 \rightarrow 00001$$
$$+\ 1$$
$$00010$$

d) What is priority encoder? Draw the truth and symbol table of decimal of BCD encoder.

Ans:- (Priority encoder definition- 1 mks, truth table -2 mks, symbol- 1 mks)

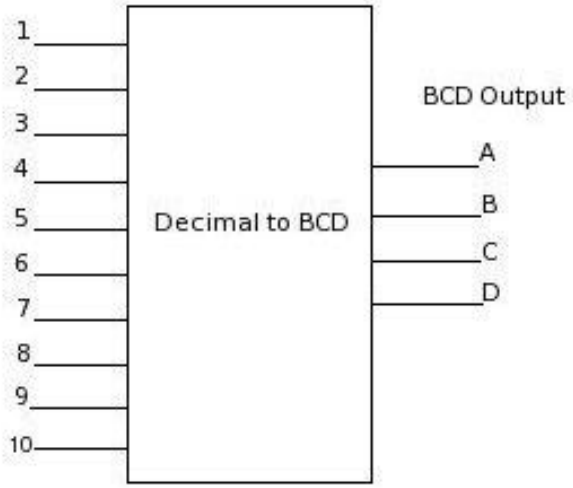
Encoder is a device which gives code corresponding to the active input. In priority encoder if two inputs active simultaneously output will be corresponding to the one which has higher priority.

E.g. IC 74147 Decimal to BCD priority encoder **OR** IC 74148 octal to binary priority encoder

I/P Decimal	O/P D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

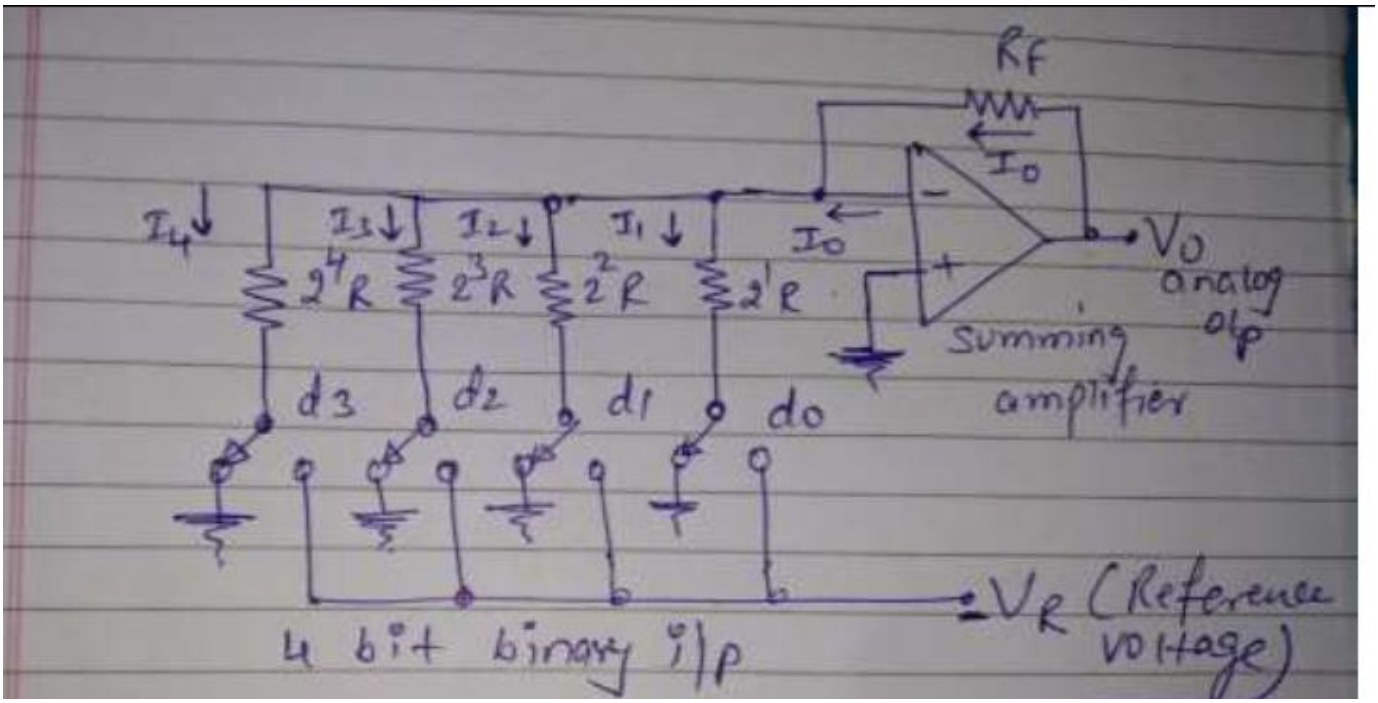
Fig: **truth table of decimal to BCD encoder**

symbol



e) Draw 4 bit weighted resistor DAC and give expression for output voltage.

Ans:- (Diagram-2mks,expression- 2 mks)



Expression for output voltage:

$$V_o = V_R [d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}]$$

Where, V_0= Analog output voltage

$d_1, d_2 \ldots\ldots d_n$ are n bit digital input word with d_1 as MSB and d_n as LSB.

V_R= Reference voltage.

f) Reduce the following Boolen expression using Boolen laws.

i) Y = AB + AB + AB + A B ii) Y = ABC + ABC + ABC

Ans:- (Each reduction- 2 mks)

i)

$A\overline{B} + \overline{A}B + AB + \overline{A}\,\overline{B}$

1) $A\overline{B} + \overline{A}B + AB + \overline{A}\,\overline{B}$

$= A\overline{B} + AB + \overline{A}B + \overline{A}\,\overline{B}$

$= A(\overline{B} + B) + \overline{A}(B + \overline{B})$ $\because B + \overline{B} = 1$

$= A + \overline{A}$

$= 1$ $\because A + \overline{A} = 1$

ii)

$Y = A\bar{B}C + \bar{A}BC + ABC$

$= A\bar{B}C + BC(\bar{A}+A)$

$= A\bar{B}C + BC$ $(\because \bar{A}+A=1)$

$= C(B + A\bar{B})$

$= C(B+A)(B+\bar{B})$ (distributive law)

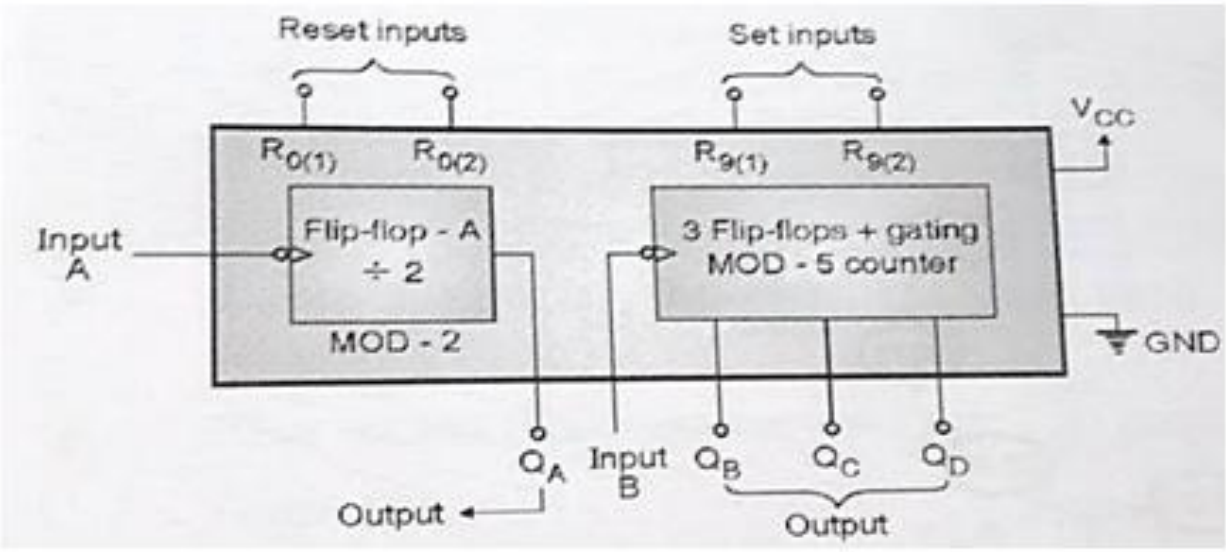
$= AC + BC$

4. Attempt any <u>Four</u> of the following: **Marks 16**

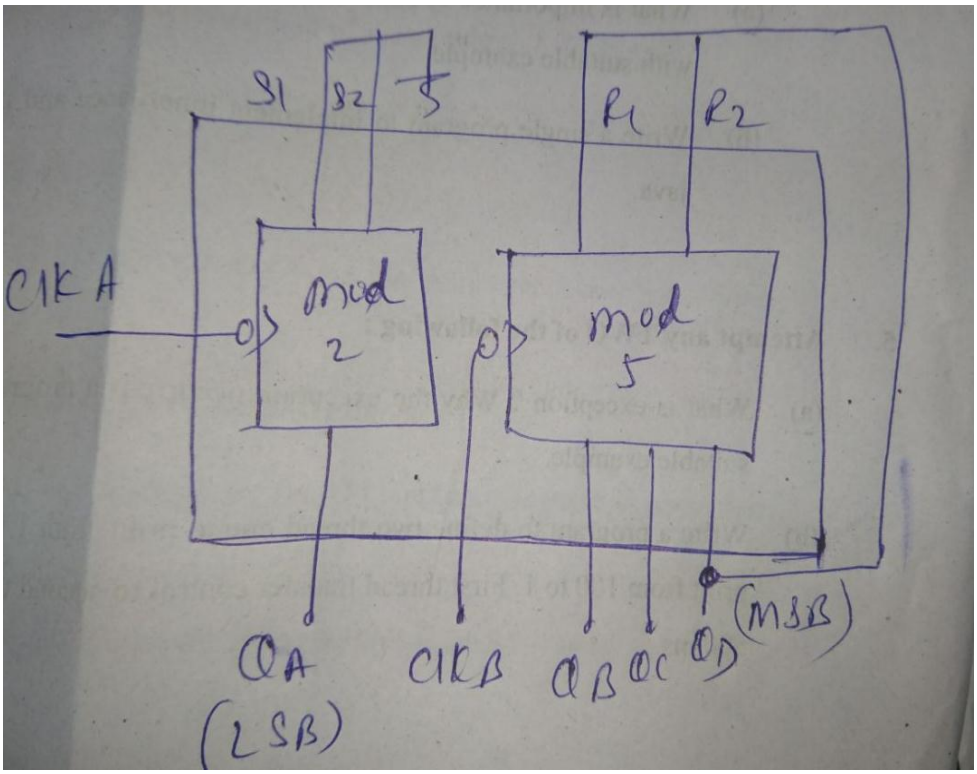
a) Draw the internal diagram of IC 7490. Design mod 8 counter using IC 7490.

Ans:- (internal diagram of IC 7490- 2 mks, mod 8 counter using IC7490- 2 mks)

Internal diagram

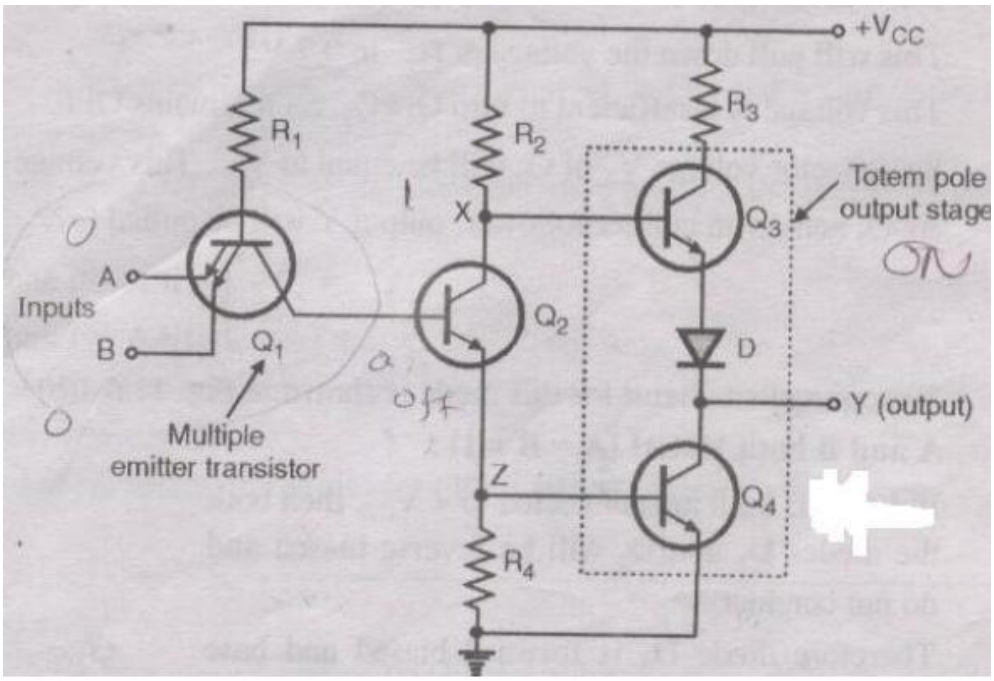


Mod 8 counter



b) Explain with circuit diagram, the principle of TTL gate (NAND) with totem pole.

Ans:- (Diagram- 2 mks, truth table – 1 mks, explaination- 1 mks)



Input		Output
A	B	$Y=\overline{A.B}$
0	0	1
1	0	1
0	1	1
1	1	0

Operating Principle:

1. A and B both LOW (A = B =0):

- If A and B both are connected to ground, then both the B- E junctions of transistors Q1 are forward biased.
- Hence diodes D1 and D2 will conduct to force the voltage at point C to 0.7 V.
- This voltage is insufficient to forward bias base emitter junction of Q2. Hence **Q2 will remain OFF.**
- Therefore its collector voltage Vx rises to Vcc.
- As transistor Q3 is operating in the emitter follower mode, output Y will be pulled up to high voltage.

Therefore, Y =1 (HIGH) …..
For A =B= 0 (LOW)

2

2. Either A or B LOW (A =0, B=1 or A=1, B=0):

- If any one input (A or B) is connected to ground with the other terminal left open or connected to +Vcc, the the corresponding diode (D1 & D2) will conduct.
- This will pull down the voltage at "C" to 0.7 V.
- This voltage is insufficient to turn ON **Q2. So it remains OFF.**
- So collector voltage Vx of Q2 will be equal to Vcc. This voltage acts as base voltage for Q3.
- As Q3 acts as an emitter follower, output Y will be pulled to Vcc.
- **Y= 1 ---- if A=0 and B=1**
- **-----if A=1 and B=0**

3. A and B both HIGH (A=B=1):-

- If A and B both are connected to +Vcc, then both the diodes D1 & D2 will be reverse biased and do not conduct.
- Therefore diode D3 is forward biased and base current is supplied to transistor Q2 via R1 and D3.
- As Q2 conducts, the voltage at X will drop down and **Q3 will be OFF,** whereas voltage at Z (across R3) will increase **to turn ON Q4.**
- As Q4 goes into saturation, the output voltage Y will be pulled down to a low voltage, **Y=0.**

c) Calculate analog output of 4 bit DAC and digital input is 1011. Assume V_{fs} = 5V.

Ans:- (Formula – 1 mks, correct problem solving- 3 mks)

Given : The 4 bit digital word is

$d_1\ d_2\ d_3\ d_4 = 1011$ with

$V_{FS} = 5$ volts

To find : $V_o = ?$

$$V_o = V_{FS}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4}\right]$$

$$V_o = 5[1 \times 2^{-1} + 0 + 1 \times 2^{-3} + 1 \times 2^{-4}]$$

$$= 5[0.5 + 0.125 + 0.0625]$$

$$= 3.4375 \text{ volts.}$$

$\therefore$ $\boxed{V_o = 3.4375 \text{ Volts}}$ **Ans.**

d) Compare sequential and combinational logic circuit. (Four points).

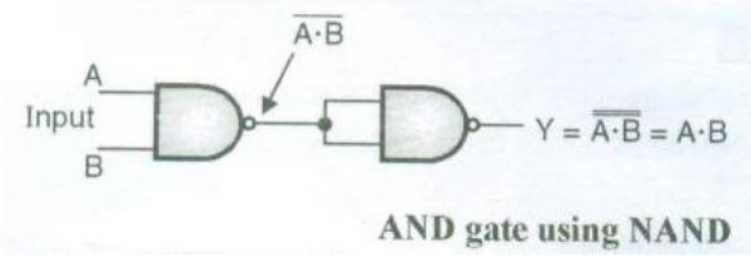
Ans:- (Relevant four points of comparison – 4 mks)

Sr no	Combinational ckt	Sequential ckt
1	The output at any instant of time depends upon the input present at that instant of time.	The output at any instance of time depends upon the present input as well as past input and output.
2	No memory element required in the circuit.	Memory element required to store bit
3	Clock not necessary	Clock is necessary
4	E.g. Adders, Subtractors ,Code converters , comparators etc.	E.g. Flip flop, Shift registers, counters etc,
5	Used to simplify Boolean expressions, k-map , Truth table	Used in counters & registers

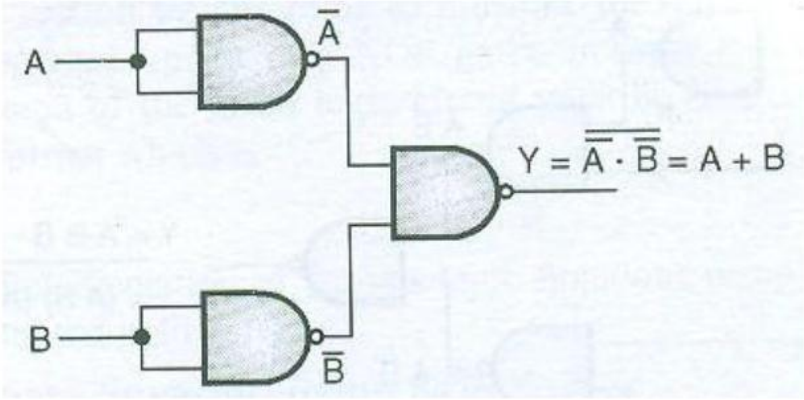
e) Implement OR gate and AND gate using NAND gate.

Ans:- (Each implementation – 2 mks)

AND gate using NAND



OR gate using NAND



f) Compare single slope and dual slope ADC.

Ans:- (Relevant 4points – 4 mks)

Single slope ADC	Dual slope ADC
Single-slope ADCs are appropriate for very high accuracy of high-resolution measurements where the input signal bandwidth is relatively low	Dual slope ADCs provides increased range, the increased accuracy and resolution, and the increased speed
Besides the accuracy these types of converters offer a low-cost alternative to others	Comparatively Dual slope ADCs are costlier
The name implies that single-slope ADC use only one ramp cycle to measure each input signal	Dual-Slope ADC operate on the principle of integrating the unknown input and then comparing the integration times with a reference cycle.
They provide less speed compared to dual slope	They provide increased speed compared to single slope.

5. Attempt any Four of the following: **Marks 16**

a) Compare R-2R and binary weighted register.

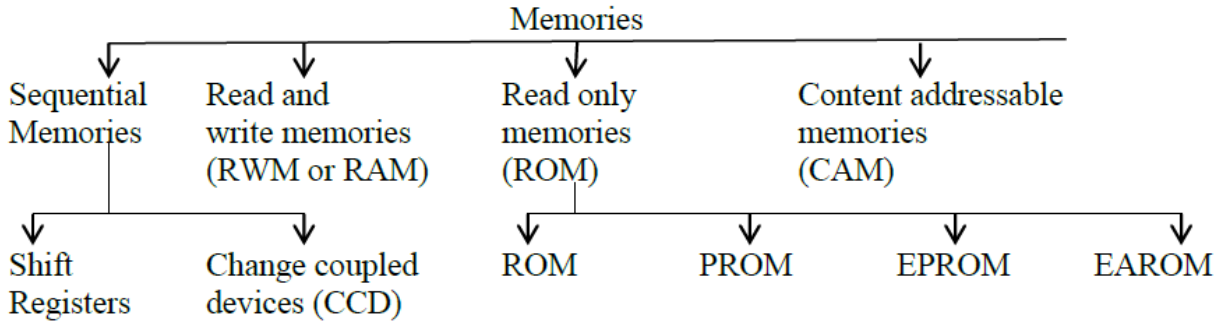
Ans:- (Relevant 4points – 4 mks)

Sr No.	Parameter	Weighted Resistor	R-2R Ladder Network
1.	Simplicity	Simple	Slightly complicated
2.	Range of resistor values	Wide range is required	Resistors of only two values are required
3.	Number of resistors per bit	One	Two
4.	Ease of expansion	Not easy to expand for more number of bits	Easy to expand

b) Define memory? Write down types of memory.

Ans:- (Definition- 1 mks, Types-= 3 mks)

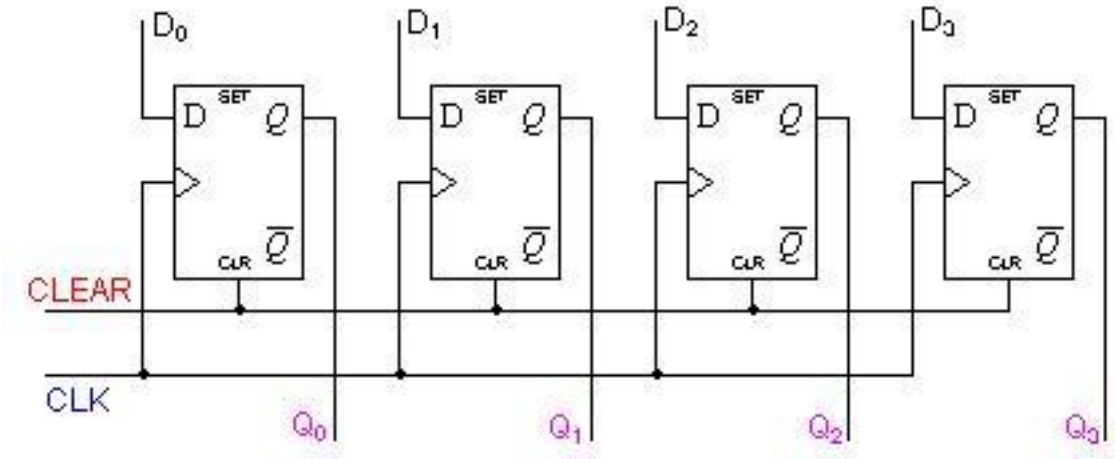
Memory- A sequential logic circuit and hence a group of flipflops that can store data in the binary form. .



c) Draw PIPO shift register. State applications of shift register.

Ans:- (Diagram – 2 mks, applications-any 2 – 2 mks)

4 bit PIPO is as shown-



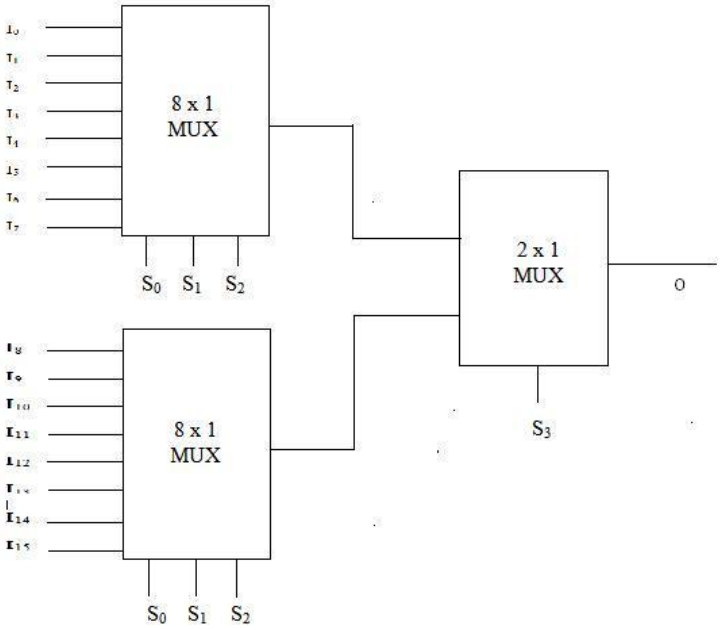
Applications – any 2

- There are so many applications of shift registers

i. To produce time delay,
ii. To simplify combinational logic
iii. To convert the serial data to parallel data.

d) Design 16:1 MUX using 8:1 MUX.

Ans:- (Correct andv relevant diagram- 4 mks)



e) Give any four characteristics of CMOS and ECL logic families.

Ans:-(Relevant 4 characteristics of each- 1/2 mks)

CMOS-(any 4 characteristics)

Lower static power dissipation
Higher noise margins
Higher packing density – lower manufacturing cost per device
High yield with large integrated complex functions

High input impedance (low drive current)
Scaleable threshold voltage
High delay sensitivity to load (fan-out limitations)
Low output drive current (issue when driving large capacitive loads)
Low transconductance, where transconductance, $g_{m \alpha} V_{in}$
Bi-directional capability (drain & source are interchangeable)
A near ideal switching device

ECL-any 4 chatacteristics

- Very fast switching with typical propagation delay of 360 ps—faster than TTL or CMOS.
- The standard ECL logic levels are nominally -0.8 V and 1.7 V for logical 1 and 0 respectively.
- Worst-case noise margins approximately 150 mV.
- ECL logic gates usually produce an output and its complement, eliminating the need for inverters.
- Current flow remains constant, eliminating noise spikes

f) Convert the following decimal numbera into excess-3 code

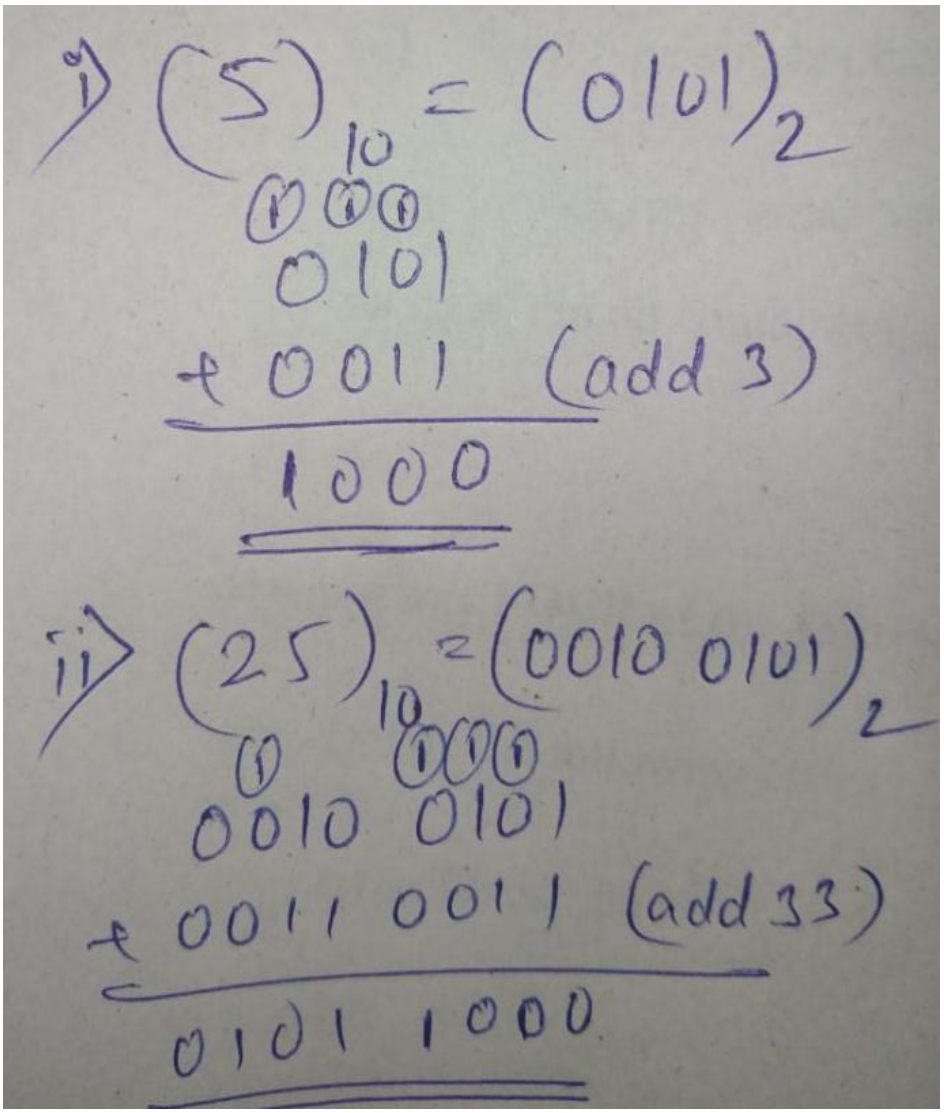
(i) $(5)_{10}$

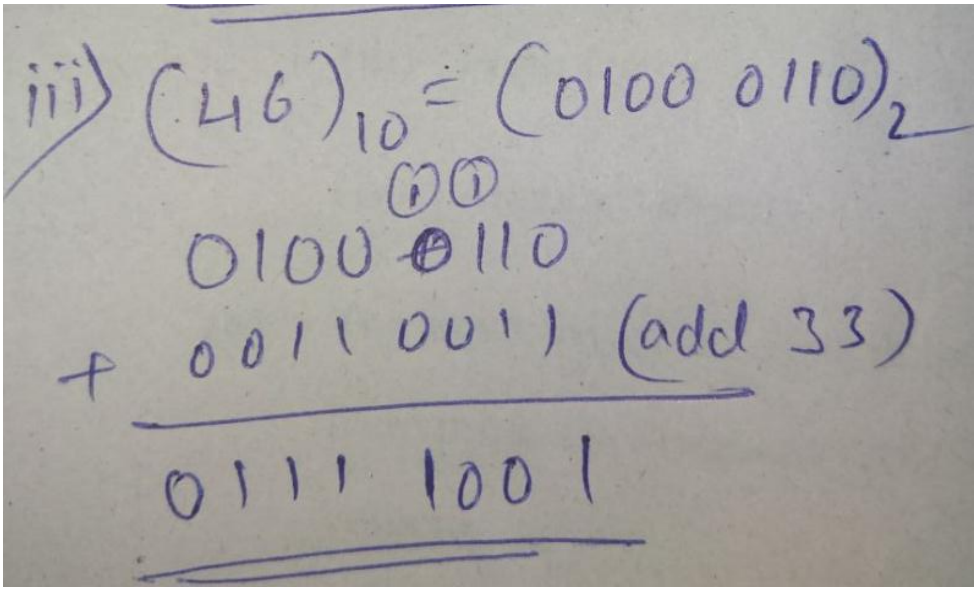
(ii) $(25)_{10}$

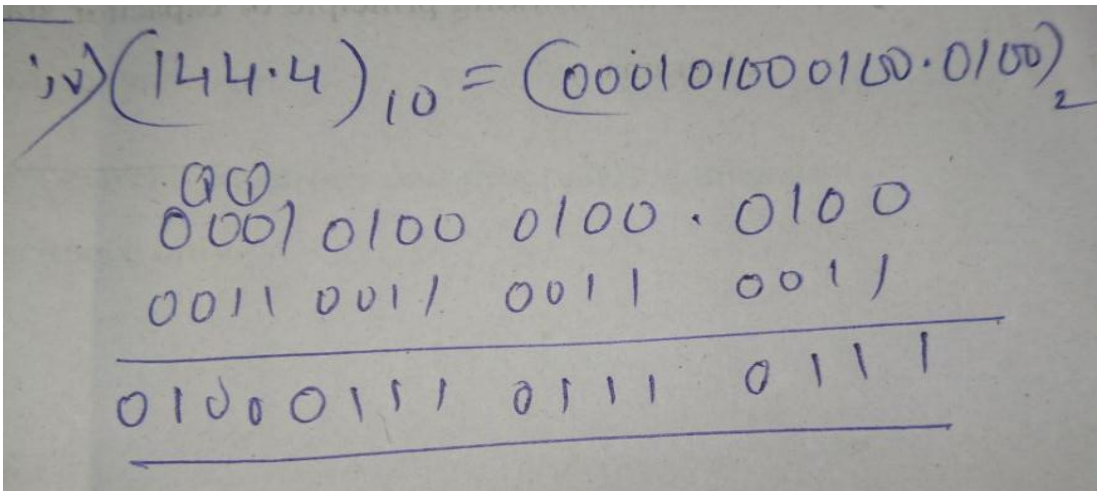
(iii) $(46)_{10}$

(iv) $144.4)_{10}$

Ans:- (Each correct conversion- 1 mks)


i) $(5)_{10} = (0101)_2$
0101
+ 0011 (add 3)
1000
ii) $(25)_{10} = (0010\ 0101)_2$
0010 0101
+ 0011 0011 (add 33)
0101 1000


iii) $(46)_{10} = (0100\ 0110)_2$
0100 0110
+ 0011 0011 (add 33)
0111 1001

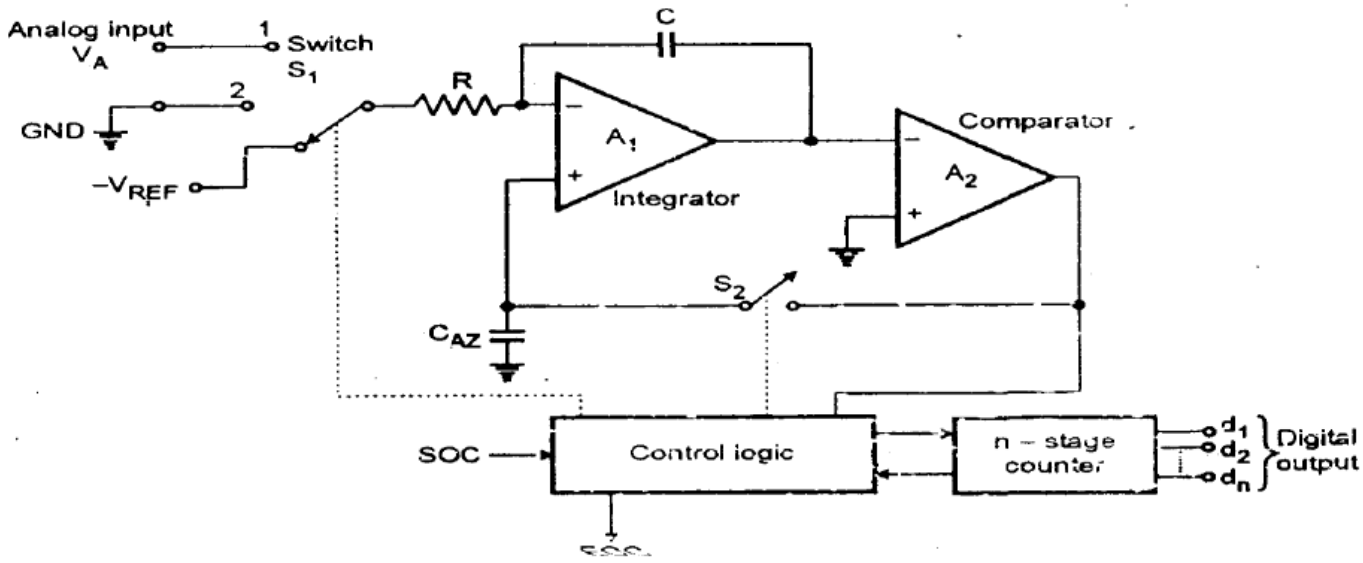


6. Attempt any <u>Four</u> of the following: **Marks 16**

a) Draw block diagram and explain working of dual slop ADC.

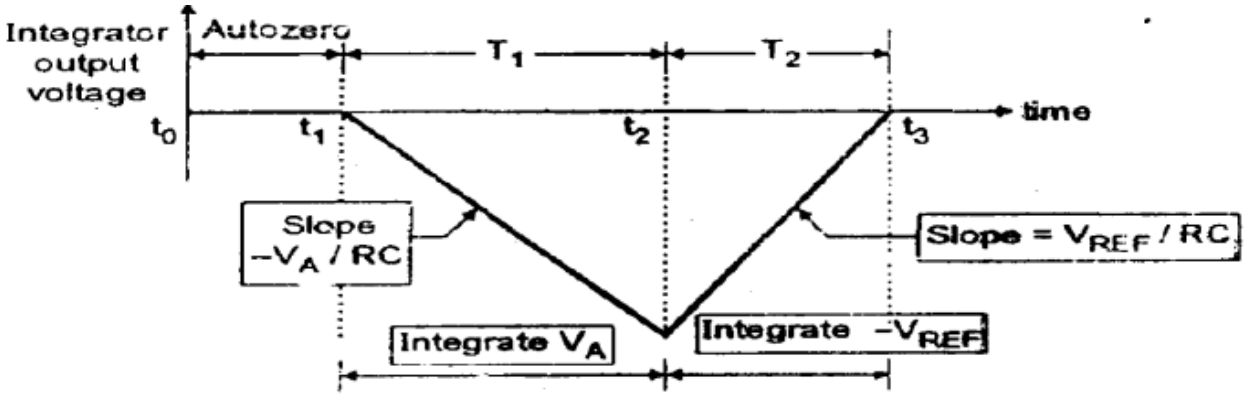
Ans:- (Block diagram- 2 mks, working – 2 mks)

The dual slope ADC consists of OPAMP's being used as integrator and comparator. The control logic accepts the SOC signal and generates EOC signal when the conversion is over. It also controls the two switches S1 and S2 out of which S1 is a single pole three way switch whose one terminal is connected to analog voltage VA, second one is connected to ground and the third one is connected to a negative reference voltage -VREF.



Operation:-At the out Initially assume that the integrator output voltage V0= 0 and the counter is in RESET condition i.e. counter
output is 00.

1. At t = t0 switch S1 is connected to ground and switch S2 is closed. The capacitor CAZ gets connected across the comparator output .
2. Any offset voltage present in the OP-AMPs will appear across the capacitor C. This will provide an automatic compensation for the input offset voltage of all the amplifiers. Therefore integrator output voltage is zero for the interval t0 to t1 .
3. At instant t1 the SOC command is given to the control logic. Switch S1 is connected to VA and Switch S2 is open circuited. CAZ acts as a memory to hold the voltage required to keep the offset zero. Hence CAZ is known as the auto zero capacitor.
4. From t1 to t2 ,this ADC will integrate the analog input VA, for a fixed duration of clock cycles. This time interval is requited for the counter to advance through all its possible output states, because for an n-bit counter there will be 2n possible output states.
5. The counter output then reduces to zero. The time duration t1 to t2 t is represented by T1.The integrator output during this period is given by,



$$V_o = -\frac{1}{RC}\int_{t_1}^{t_2} V_A\,dt = \frac{-V_A T_1}{RC}$$

6.This expression represents a straight line with a slope of - VA / RC. Thus we get a decreasing ramp. The time period T is thus represented by 2n clock cycles.
T = 2n x T where T = One clock cycle period

7. At the end of interval T1 the integrator input is connected to a fixed negative reference voltage (-V REF) via switch S1

8. The integrator output now starts increasing towards zero with positive slope. The slope of the line is VREF / RC for the duration t2 to t3.

9. The counter starts counting from 0. The integration will continue till the integrator output is non-zero. At instant t3 the integrator output reduces to zero then the comparator output goes from HIGH to LOW and the clock pulses given to the counter are stopped.

10. At t3. the counter output shows a number corresponding to N clock cycles it has counted during period t2 to t3.

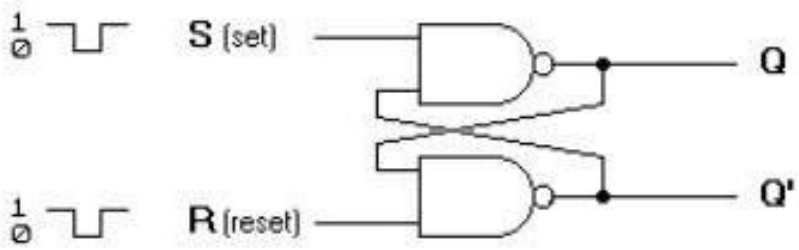
11. Thus this number N represents the time taken for integrator output to reduce from -VA to 0. Hence N represents the desired digital output code proportional to the analog input VA.

12. If VA increases, then the integrator capacitor vi11 charge to a higher negative voltage during the time interval T Therefore the time T required to reduce the integrator output to zero increases.

13. Therefore the counter output count (N) will be higher. Thus N is proportional to VA.

b) Describe working of SR latch using NAND gates with proper truth table.

Ans:- (Diagram- 2mks, working – 1 mks, truth table-1 mks)



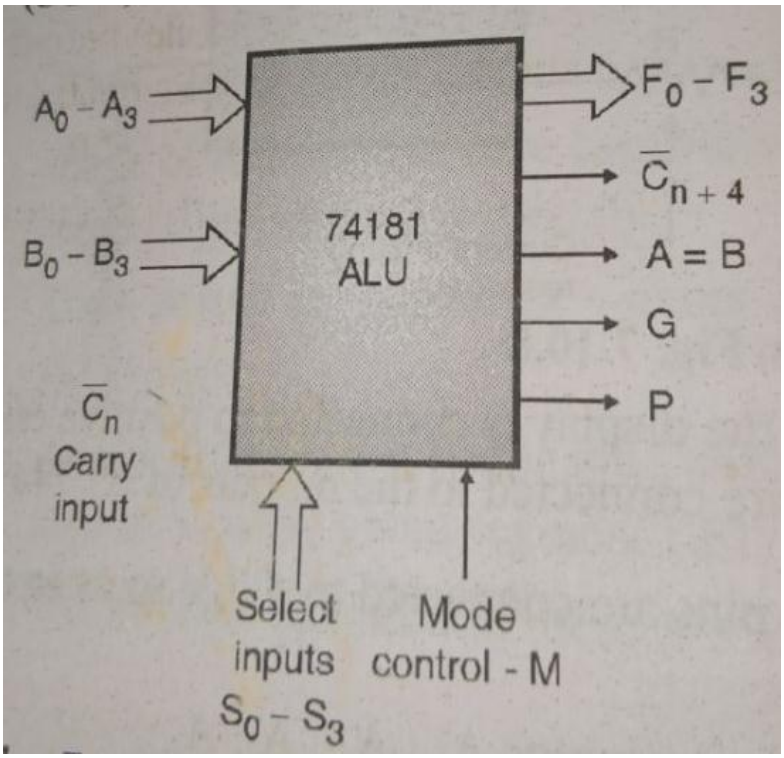
(a) Logic diagram

S R	Q Q'	
1 0	0 1	
1 1	0 1	(after S=1, R=0)
0 1	1 0	
1 1	1 0	(after S=0, R=1)
0 0	1 1	

(b) Truth table

c) Draw the block diagram of ALU IC 74181 and also write its operation.

Ans:- (Block diagram- 2 mks, operation- 2 mks)



Operation-

A 4 bit ALU does arithematic and logical operations on 4 bits inputs Aand B , Output is achieved on output F.The IC can perform 16 arithematic and 16 logical operations that depends on mode control M.

For M=0, it does logical operation

For M=1, Arithematic operation.The details of pins are as shown-

Pin Descriptions

Pin Names	Description
$\overline{A}0$–$\overline{A}3$	Operand Inputs (Active LOW)
$\overline{B}0$–$\overline{B}3$	Operand Inputs (Active LOW)
S0–S3	Function Select Inputs
M	Mode Control Input
C_n	Carry Input
$\overline{F}0$–$\overline{F}3$	Function Outputs (Active LOW)
A = B	Comparator Output
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
C_{n+4}	Carry Output

d) Mention any eight Boolen laws.

Ans:- (Eight laws- ½ mks each)

1.	Law of Identity	$\overline{A} = A$ $\overline{\overline{A}} = A$
2.	Commutative Law	$A \cdot B = B \cdot A$ $A + B = B + A$
3.	Associative Law	$A \cdot (B \cdot C) = A \cdot B \cdot C$ $A + (B + C) = A + B + C$
4.	Idempotent Law	$A \cdot A = A$ $A + A = A$
5.	Double Negative Law	$\overline{\overline{A}} = A$
6.	Complementary Law	$A \cdot \overline{A} = 0$ $A + \overline{A} = 1$
7.	Law of Intersection	$A \cdot 1 = A$ $A \cdot 0 = 0$
8.	Law of Union	$A + 1 = 1$ $A + 0 = A$
9.	DeMorgan's Theorem	$\overline{AB} = \overline{A} + \overline{B}$ $\overline{A + B} = \overline{A}\,\overline{B}$
10.	Distributive Law	$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$ $A + (BC) = (A + B) \cdot (A + C)$

e) Draw 3 bit synchronous counter with truth table and explain working.

Ans:- (Diagram- 2 mks, working – 1 mks, truth table – 1mks)

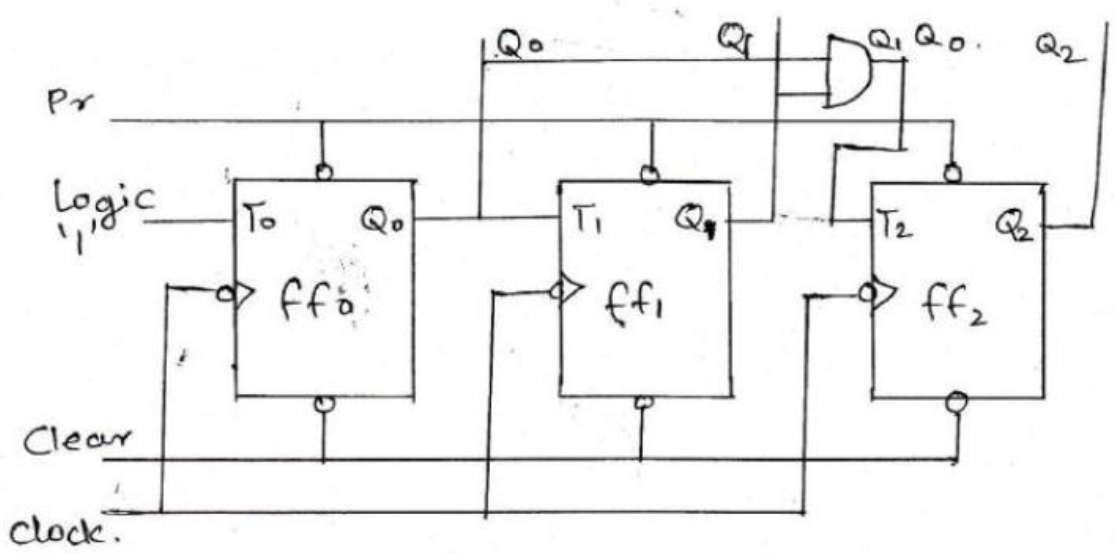
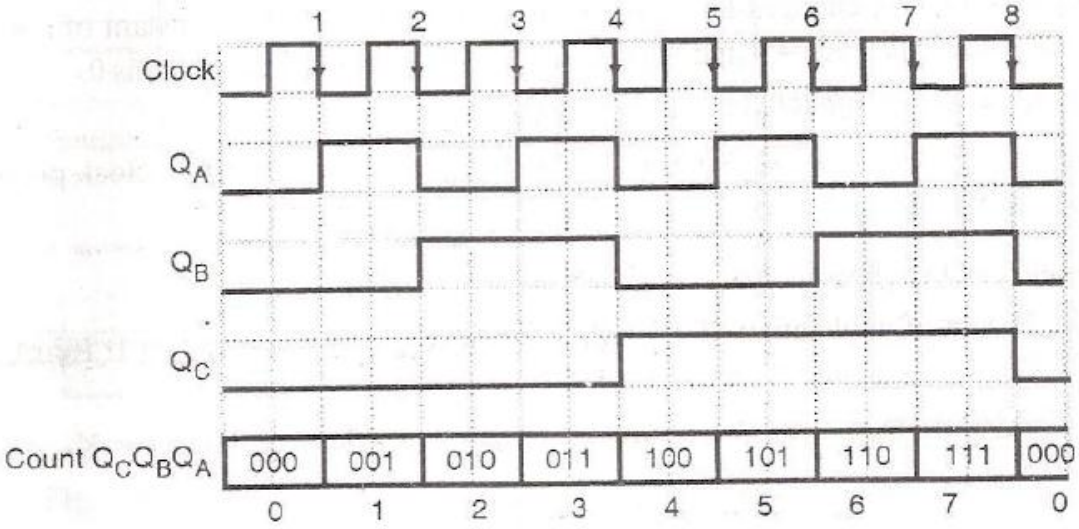


Fig: bit synchronous counter

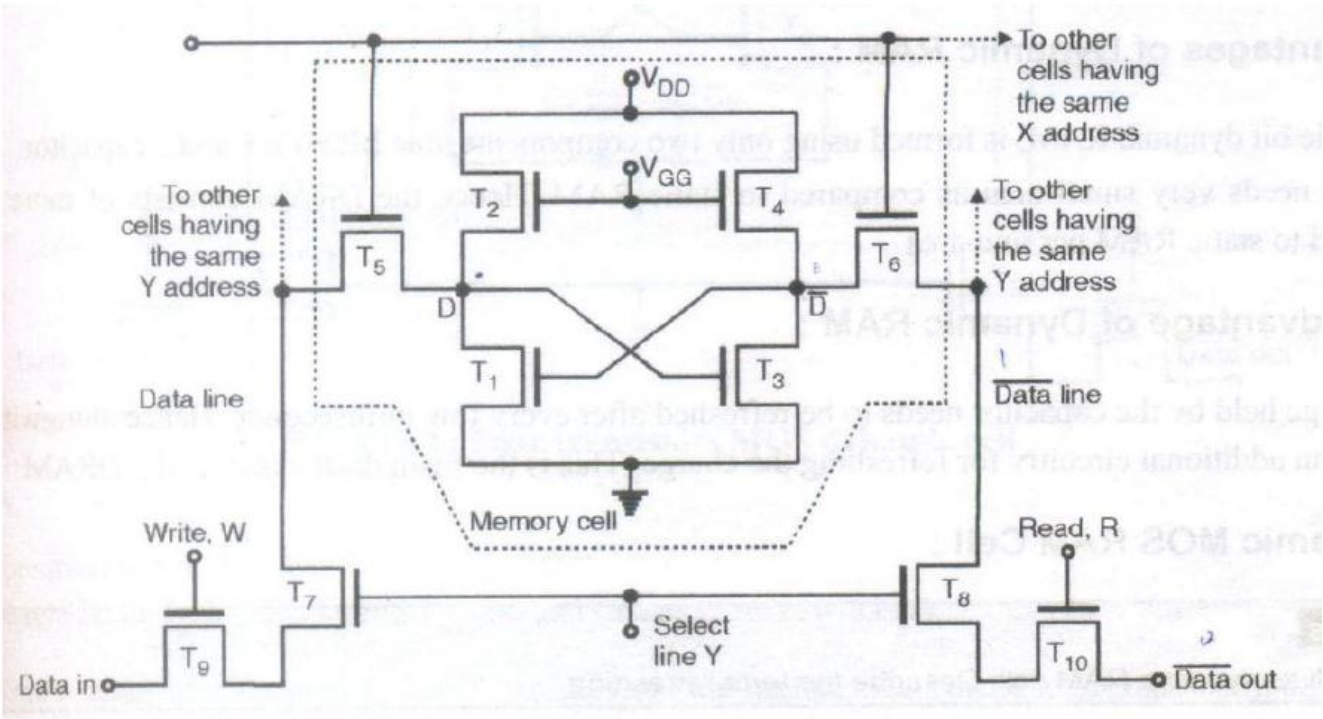
Clock	Q_C	Q_B	Q_A
0	0	0	0
1st (↓)	0	0	1
2nd (↓)	0	1	0
3rd (↓)	0	1	1
4th (↓)	1	0	0
5th (↓)	1	0	1
6th (↓)	1	1	0
7th (↓)	1	1	1



f) Draw and explain static RAM cell (TTL).

Ans:- (Diagram- 2 mks, explanation – 2 mks)

Static RAM cell with NMOS CELL



T2 & T4 are acting as resistances. X & Y lines are used for addressing cell.
When X=Y=1 (high) ,the cell is selected . When X=1, the MOSFETS T5 & T6 are turned ON .,which will connect memory cell to the data line and data bar line.
When Y=1 ,the MOSFETS T 7 & T8 are turned ON .,which will make read & write operation possible