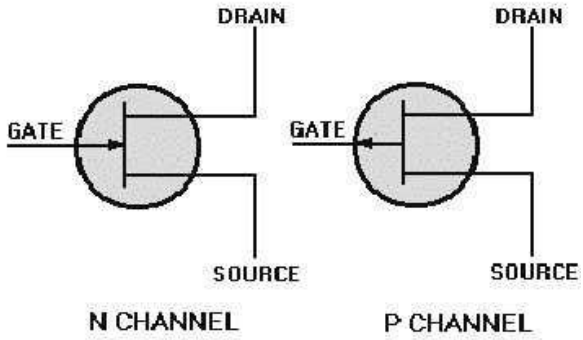
MODEL ANSWER

WINTER– 17 EXAMINATION

Subject Title: Electronic devices and circuits Subject Code: 17319

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q.N.	Answer	Marking Scheme
Q.1	(A)	**Attempt any SIX :**	12-Total Marks
	a)	**List any two applications of transistor.**	2M
	Ans:	**Applications of transistor:** 1. As a switch 2. As an amplifier 3. In Oscillators 4. In Multivibrators 5. In Time base generators	Any two 1M each
	b)	**Draw symbol of n-channel and p-channel JFET.**	2M
	Ans:	**Symbol of n-channel and p-channel JFET:** 	1M each

c) **What is coupling? List the types of amplifier coupling.** **2M**

Ans: The term Coupling occurs in multi stage amplifiers and refers to the way in which the output of one stage is connected to the input of next stage. **1M definition,**

There are mainly three types of coupling which are **1M for types**

- Transformer coupling
- RC coupling
- Direct coupling

d) **Which type of feedback is used in amplifier and in oscillator?** **2M**

Ans: In amplifier negative feedback is used and in oscillator positive feedback is used **1M each**

e) **Compare BJT & UJT (any two points).** **2M**

Ans: **1M each**

Sr. No.	BJT	UJT
1	Bipolar device	Unipolar device
2	It has three terminals: Emitter , Base , collector	It has three terminals: Emitter, Base 1, Base 2
3	It has two PN junction	It has only PN junction

f) **List the types of biasing of transistor. Which type of biasing is used mostly?** **2M**

Ans: **1M any two methods.**

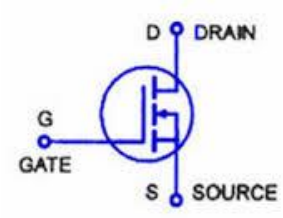
1. Fixed bias.
2. Collector-to-base bias.
3. Fixed bias with emitter resistor.
4. Voltage divider bias or potential divider.
5. Emitter bias.

The voltage divider biasing is mostly used. **1M**

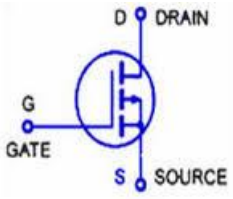
g) **Draw neat symbol of E-MOSFET & D-MOSFET.** **2M**

Ans: **½ M Each**

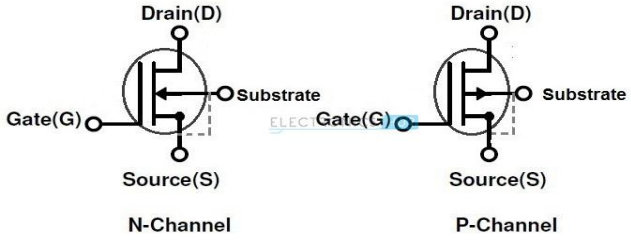
Symbol of E-MOSFET-



N-channel EMOSFET



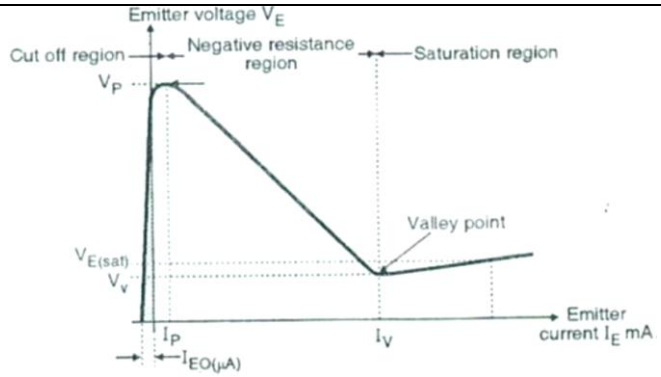
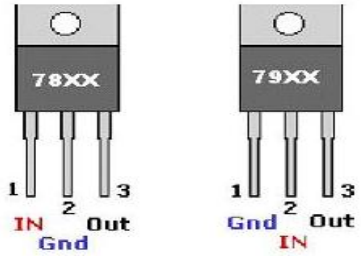
P-channel EMOSFET

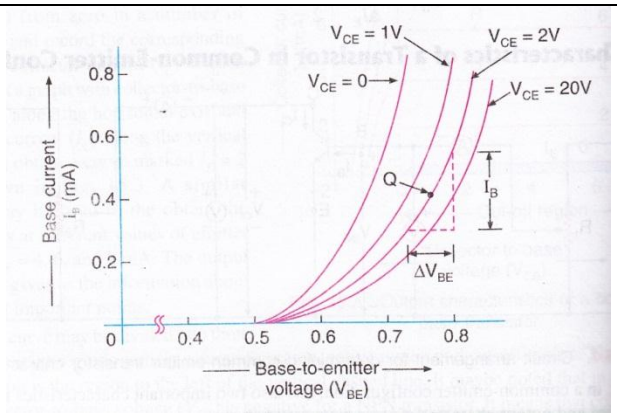
		Symbol of DMOSFET:- 	**½ M Each**
(h)	**Write any two application of tuned amplifier.**		**2M**
Ans:	**Application of Tuned amplifier:** 1. Communication transmitter and receivers 2. As an RF amplifier in TV receiver & Radio receiver		**1M Each**
(B)	**Attempt any TWO :**		**8 - Total Marks**
a)	**Compare CB, CE & CC on the basis of** **(i) Input Resistance (Ri)** **(ii) Output Resistance (Ro)** **(iii)Current Gain (Ai)** **(iv)Voltage gain (Av)**		**4M**
Ans:			**1M each**

Parameters	**CB**	**CE**	**CC**
Input Impedance	Low(100Ω)	Low(750Ω)	Very High(750KΩ)
Output Impedance	Very High(450KΩ)	High(45kΩ)	Low(50Ω)
Current Gain	Less than unity	High (100)	High(100)
Voltage Gain	High(About150)	Very high(about 500)	Less than 1

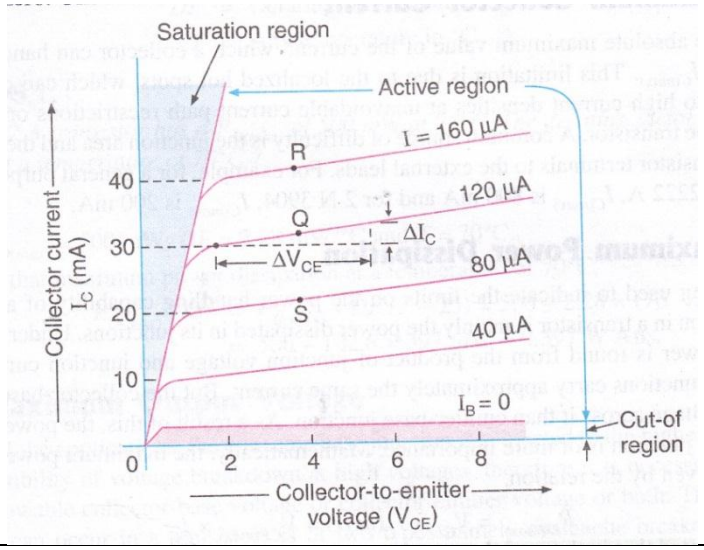
(Values may differ since different reference books provide different values)

b)	**Explain working of UJT with the help of VI characteristics.**	**4M**
Ans:	**V-I Characteristic :**	**2M**

		 **Working:** • This is graphically representation of emitter voltage versus emitter current. For the emitter potentials less than Vp the UJT is in OFF state. • As emitter potential increases and reaches $Vp = \eta V_{BB} + V_D$, the UJT starts conducting. Then with increase in emitter current I_E the emitter voltage decreases. • The reduction in voltage across UJT is due to the drop in resistance R_{B1} With increase in value of I_E. • This region is known as "Negative Resistance" region, which is stable enough to be used in various applications. • Eventually valley point will be reached and a further increase in I_E will place the device into saturation.	**2M**
	c)	**Draw labelled pin diagram of IC 78 XX and IC 79 XX. Also write the function of these IC's.**	**4M**
	Ans:	 **Function of IC 78 XX and IC 79 XX:-** The main function of these IC is to supply required regulated Positive and negative voltage to the electronic circuits.	**1M each Pin Diagram ,1M for labeling** **1M**
Q 2		**Attempt any FOUR :**	**16 – Total Marks**
	a)	**Draw labelled Input and Output character of transistor in CE configuration.**	**4M**
	Ans:	**Input Characteristic of CE configuration:**	**2M**



Output Characteristics of CE configuration:

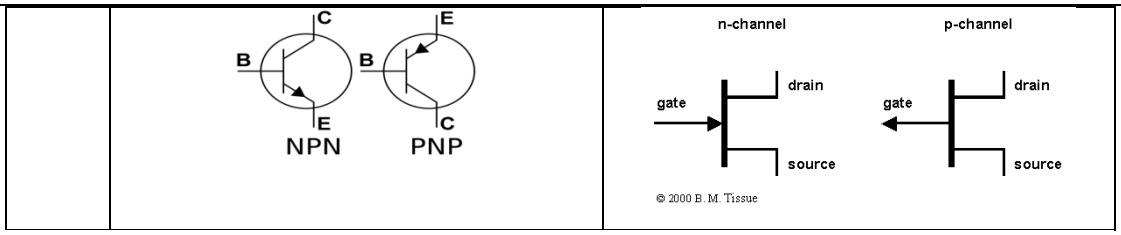


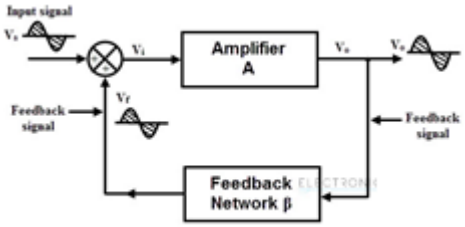
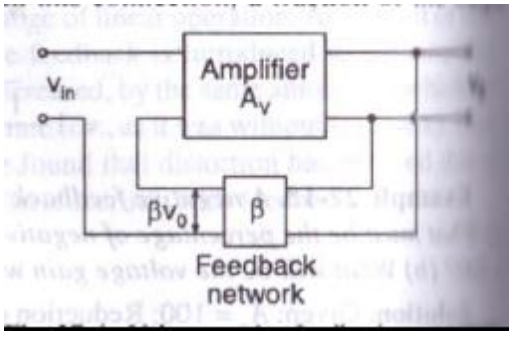
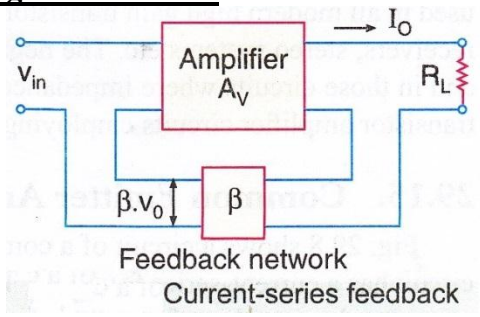
2M

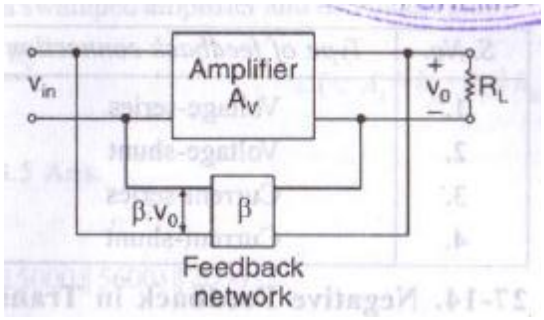
b) Compare BJT & FET (any four points). **4M**

Ans: **(Any four points 1M each)**

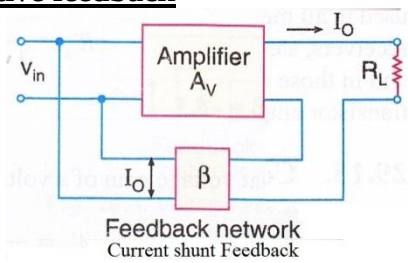
Sr. No.	BJT	FET
1	Bipolar device i.e current flows due to both electrons and holes	Unipolar device i.e current flows due to only one of majority carrier either electrons and holes
2	It has two PN junctions.	It has only one PN junction.
3	Current controlled / operated device	Voltage controlled / operated device
4	It has three terminals: Emitter, Base, Collector	It has three terminals: Source, Gate, Drain
5	**Symbols :**	**Symbols :**

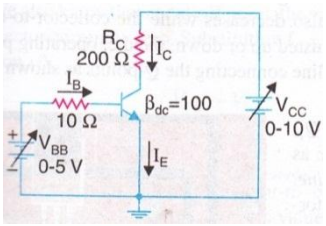


	c)	**List types of feedback connection. Draw anyone type of connection diagram.**	**4M**
	Ans:	**<u>Types of feedback connection:</u>** **A) <u>Positive feedback-</u>**  **B) <u>Negative Feedback-</u>** **i. <u>Voltage series negative feedback</u>**  **ii. <u>Current series negative feedback</u>**  **iii. <u>Voltage Shunt negative feedback</u>**	**Types 2M, any one Diagram 2M**



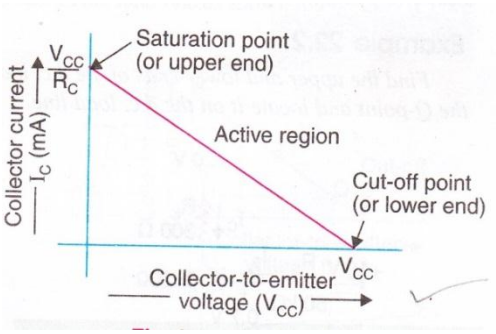
iv. Current shunt negative feedback



d)	**What is biasing? Explain the concept of DC load line.**	**4M**
Ans:	**Transistor Biasing** is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor. **Concept of DC load line:-** For proper operation of a transistor a fixed level of certain currents and voltage in a transistor are set. These values of current and voltage defines the point at which the transistor operates this point is called operating point. It is also known as quiescent point or simply Q-point. **Explanation with Diagram:-**  Consider the transistor circuit shown in the fig. for this circuit we know that the value of collector current is given by the relation. $I_C = \frac{V_{CC} - V_{CE}}{R_C}$ .....Equation (i) Where ,	**1M** **3M**

V_{CC} = value of DC supply voltage in the collector circuit.
V_{CE} = The value of collector to emitter and
R_c = value of collector resistance
The value of collector to emitter voltage (V_{CE}) at saturation point is very small as compare to V_{CC} supply. Therefore

$$I_C = \frac{V_{CC}}{R_C}$$



At cut off point the value of collector current is zero substituting $I_C = 0$ in equation (i)

$$0 = \frac{V_{CC} - V_{CE}}{R_C}$$

OR

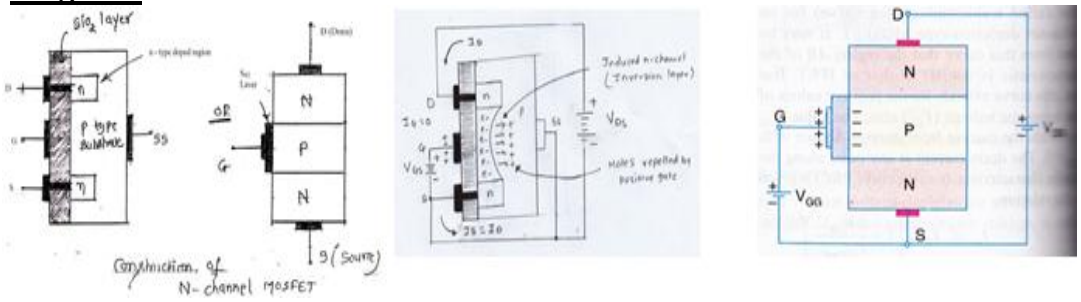
$V_{CE} = V_{CC} = V_{CE(cut\ off)}$……..Equation (ii)

Equation (i),(ii) are the Q point coordinate of DC load line.

e) **Explain working of E-MOSFET with the help of neat constructional diagram.** **4M**

Ans:

Diagram:



2M

Working principle:-

Case1:- When V_{GS}=0 volt **2M**

If V_{GS}=0 volt and a +ve voltage applied between its drain and source, then due to the absence of the n-type channel a zero drain current will result.

Case2:- When V_{GS}=positive and V_{GS}=positive

		• The +ve potential at the gate terminal will repel the holes present in the p-type substrate. • This results in creation of a depletion region sio_2 insulting layer. But the minority carriers i.e the e-s in the p-type substrate will be attracted towards the gate terminal and gather near the surface of sio_2 layer. • As we increase the positive V_{GS}, the number of electrons gathers near Sio_2 layer we increase. • The electron concentration near Sio_2 layer increase to such an extent that it creates an induced n-channel. This connects the n-type doped region. This induced n-channel is called 'inversion layer'. The drain current then start flowing through this induced channel. And the value of V_{GS} at which this conduction begins is called as 'threshold voltage' $V_{GS\ (TH)}$. **Case 3:-** Effect of increasing in V_{DS} • The $+V_{GS}$ is kept constant and the V_{GS} is increased gradually .due to this, the gate terminal becomes less and less +ve with respect to drain. So less number of electrons are attracted towards gate terminal and the induced channel becomes narrow that means, the channel width will be reduced to a point of pinch off and the saturation condition will occur, hence I_D will remains constant.	
	f)	**Describe the concept of thermal runaway. How it can be avoided?**	**4M**
	Ans:	**Concept of thermal runaway:** 1. The reverse saturation current in semiconductor devices changes with temperature. The reverse saturation current approximately doubles for every 10^0 c rise in temperature. 2. As the leakage current of transistor increases, collector current (Ic) increases 3. The increase in power dissipation at collector base junction. 4. This in turn increases the collector base junction causing the collector current to further increase. 5. This process becomes cumulative. & amp; it is possible that the ratings of the transistor are exceeded. If it happens, the device gets burnt out. This process is known as 'Thermal Runaway'. **Remedy to avoid thermal runaway:** Thermal runaway can be avoided by 1) Using stabilization circuitry 2) Heat sink	**2M** **2M**
Q. 3		**Attempt any FOUR :**	**16 – Total Marks**
	a)	**Explain working of transistor as a switch with neat circuit and waveforms.**	**4M**

Ans:

- The switch operates between two states namely saturation and cut-off state.
- The saturation state occurs when both the junctions(i.e. emitter-base junction and collector-base junction) of transistor are forward biased.
- The cut off state occurs when both the junctions of transistors are reverse biased.

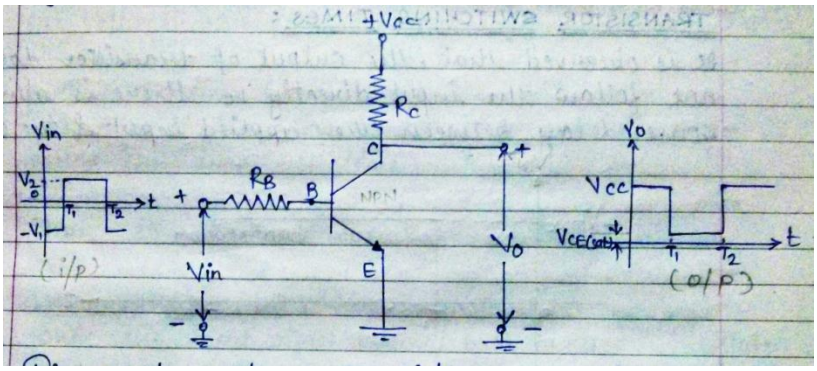


Figure above shows transistor as a switch with input and output waveforms.

- A input (V_{in}) is applied at the base of the transistor. At time T_1, the input voltage (V_{in})is equal to'-V_1' and emitter-base junction is reverse biased.∴the transistor is in cut-off and hence practically no current exists in the circuit.
- $\therefore I_B = 0, I_C = \beta . I_B = 0$
  Apply KVL to output loop

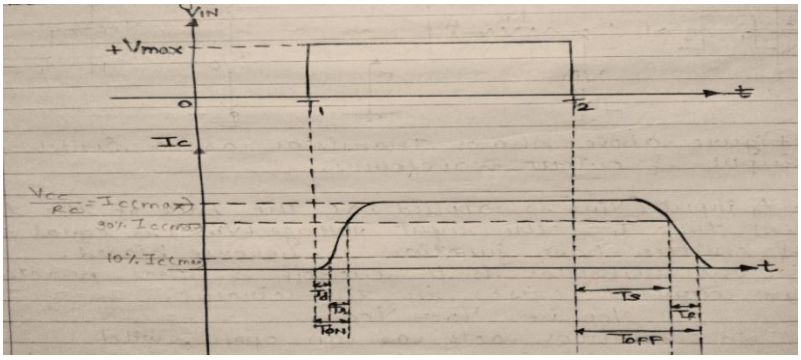
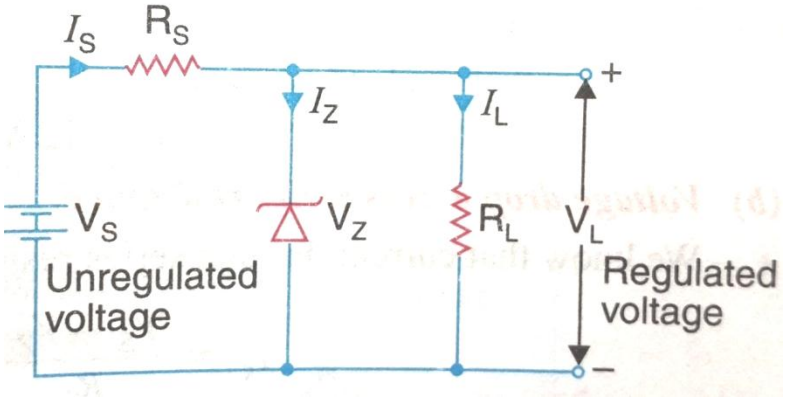
$$\therefore V_{CC} - I_C R_C - V_O = 0$$
$$\therefore V_{CC} = V_O \ldots\ldots (AS I_C R_C = 0)$$
$$\therefore V_{CC} = V_{CE} = V_O$$

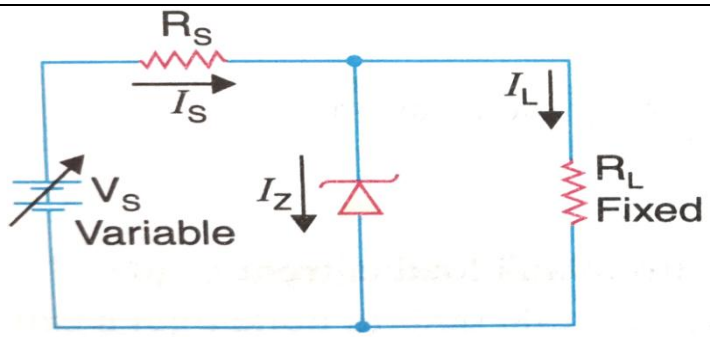
- So transistor acts as an open switch.
- For the time interval $T_1 < t < T_2$, the input voltage is equal to V_2, both the emitter base and collector base junctions are forward biased and the transistor is in saturation.
- The output voltage $V_0 = V_{CE\ (sat)} = 0.2V$ for silicon and collector current is maximum $I_C = \frac{V_{CC}}{R_{CC}}$.
- So transistor acts as a closed switch.
- By applying KVL to output loop:

$$V_{CC} - I_C R_C - V_O = 0$$
$$V_O = V_{CC} - I_C R_C$$

As I_C is maximum, $I_C R_C$ is also maximum.
∴V_O is negligible i.e.$V_{CE(sat)}$.

(Explanation- 3M)

		Waveform:-  	**1M**
	b)	**Draw circuit of Zener diode as a voltage regulator and explain it's working.**	**4M**
	Ans:	**Circuit of Zener diode as voltage regulator:**  **Working:** **Circuit Description-** As the zener diode is connected in parallel or shunt with the load hence it is also known as SHUNT REGULATOR. A resistance (Rs) is connected in series with the zener diode to limit current in the circuit. For proper operation, the input voltage (Vs) must be greater than the zener voltage (Vz). Where, Rz= zener resistance $Is=Iz + I_L$ **Working :** **A] Regulation by varying input voltage-**	**Diagram: 2M, Working:2 M**



(a) Varying input voltage.

Here the load Resistance is kept fixed and input voltage is varied within the limits

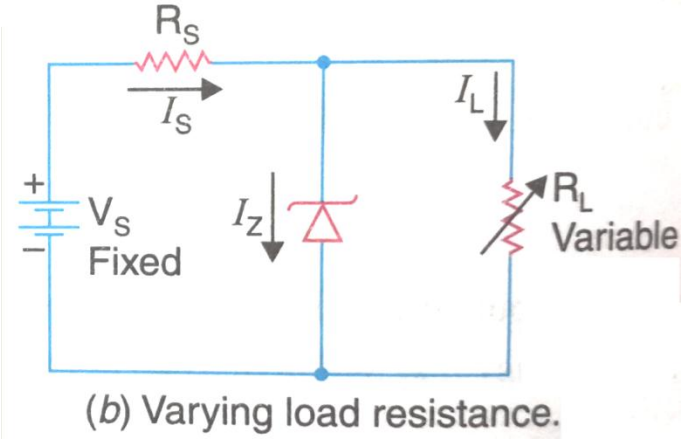
CONDITION 1. -WHEN INPUT VOLTAGE IS INCREASED

When input voltage is increased the input current (Is) also increases. Thus current through zener diode gets increased without affecting the load current(IL).The increase in input voltage also increases the voltage drop across the resistance Rs thereby keeping the VL constant.

CONDITION 2.- WHEN INPUT VOLTAGE IS DECREASED

When input voltage is decreased, the input current gets reduced, as a result of this Iz also decreases. The voltage drop across Rs will be reduced and thus the load voltage (V_L) and load current (I_L) remains constant.

B] REGULATION BY VARYING LOAD RESISTANCE

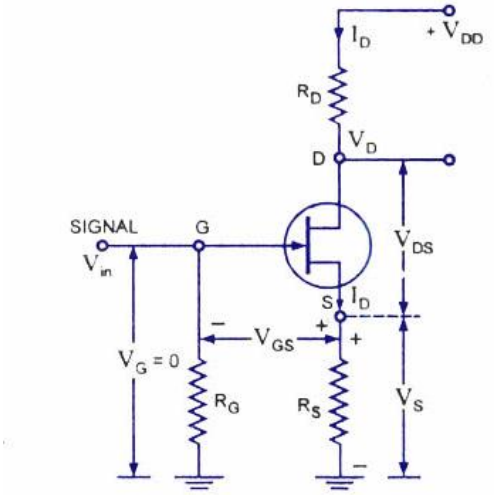


(b) Varying load resistance.

In this method the input voltage is kept constant where as load resistance RL is varied.

CONDITION 1. WHEN LOAD RESISTANCE IS INCREASED

When load resistance is increased, the load current reduces, due to which the zener current I_Z increases. Thus the value of input current and voltage drop across series resistance is kept constant. Hence the load voltage remains constant.

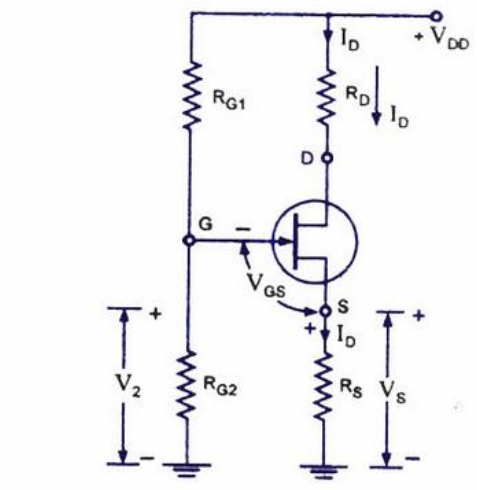
		CONDITION 2. WHEN LOAD RESISTANCE IS REDUCED When load resistance is decreased, the load current increases. This leads to decrease in I_Z. Because of this the input current and the voltage drop across series resistance remains constant. Hence the load voltage is also kept constant.	
	c)	**List types of FET biasing and explain anyone type with circuit diagram.**	**4M**
	Ans:	**Types of FET biasing-** i. Self Biasing Method ii. Voltage Divider bias iii. Source Bias **1. SELF BIASING** • In this circuit there is only one drain supply and no gate supply. • The gate terminal is connected through resistor R_G to the ground. • The source terminal is connected through resistor R_S to the ground. {NOTE: In JFET input PN junction between gate & source is always reverse bias, due to this input resistance of JFET is very high. Due to this input gate current I_G = zero. Hence if resistor R_G is connected in series with gate terminal, voltage drop across R_G is zero as $V_{RG} = I_G R_G = 0$}  • $V_G = I_G R_G = 0$ • $V_{GS} = V_G - V_S$ $= -V_S$ APPLY KVL TO INPUT LOOP $V_{GS} + I_D R_S = 0$ $\therefore V_{GS} = -I_D R_S$ • $I_D = I_{DSS}\{1-\frac{V_{GS}}{V_P}\}^2$ Shockley's equation • APPLY KVL TO OUTPUT LOOP $V_{DD} - I_D R_D - V_{DSQ} - I_D R_S = 0$ $V_{DSQ} = V_{DD} - I_D R_D - I_D R_S$	**List Types:1M, Explain with Circuit diagram 3M**

$= V_{DD} - I_D [R_D + R_S]$

OR

2. VOLTAGE DIVIDER BIAS

- The name voltage divider derived from the fact that resistor R_1 & R_2 are connected on the gate side between the V_{DD} supply and ground form a voltage divider.



$$V_G = \frac{R_2}{R_1+R_2} V_{DD}$$

- APPLY KVL TO INPUT LOOP

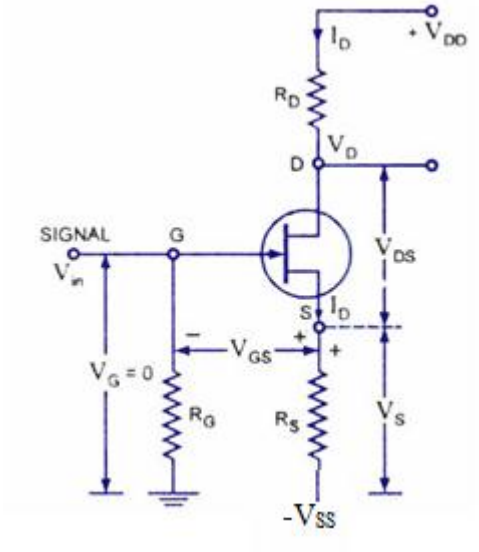
$V_G - V_{GS} - I_D R_S = 0$
$V_{GS} = V_G - I_D R_S$

- $I_D = I_{DSS} \{1-\frac{V_{GS}}{V_P}\}^2$ Shockley's equation
- APPLY KVL TO OUTPUT LOOP

$V_{DD} - I_D R_D - V_{DSQ} - I_D R_S = 0$
$V_{DSQ} = V_{DD} - I_D R_D - I_D R_S$
$= V_{DD} - I_D [R_D + R_S]$

OR

3. SOURCE BIAS

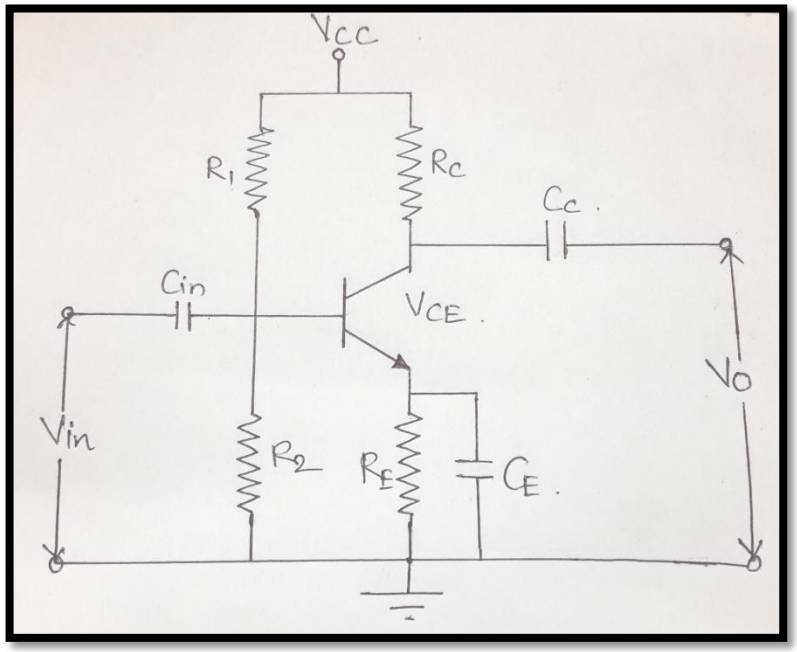


APPLY KVL TO INPUT LOOP

- $V_{GS} + I_D R_S - V_{SS} = 0$

$V_{GS} = V_{SS} - I_D R_S$

- $I_D = I_S = \frac{V_S + V_{SS}}{R_S}$
- $V_{DS} = V_D - V_S$
  $= V_{DD} - I_D R_D - V_S$
  $= V_{DD} - I_D R_D + V_{GS}$

	d)	**Describe working of single stage CE amplifier with sketch.**	**4M**
	Ans:	**Circuit Diagram:** 	**Diagram: 2M, Working:2 M**

Circuit Description:

- The input a.c. signal is applied across the base emitter terminals of the transistor& output is taken across collector emitter terminals of the transistor. V_{BB} supply forward biases the emitter base junction & V_{CC} supply reverse biases the output junction.
- The Q point is determined by the V_{CC} supply along with the resistance $R_{C.}$The resistances $R_{1,}R_{2,}$ R_E form the biasing & stabilisation circuit & thus establishes proper operating point.
- Input capacitor ($C_{in}\approx 10\mu F$) : It blocks DC voltage to the base, if it is not provided the source resistance comes across R_2,so that transistor gets unbiased. It allows a.c. to pass & isolates source resistance from R_2.
- Emitter capacitance ($C_E\approx 100\mu F$): it is used in parallel with R_E to provide a low reactance path to the amplified a.c. signal. If it is not used then amplified a.c. signal flowing through R_E will cause a voltage drop across it, thus reducing the output voltage.
- Coupling capacitor ($C_C\approx 10\mu F$): it couples one stage of amplification to the next stage. If it is not used, R_C comes across with the R_1 of next stage & biasing of 2nd stage gets disturbed. In short it isolates the d.c. of one stage from the next stage but allows the a.c. signal.

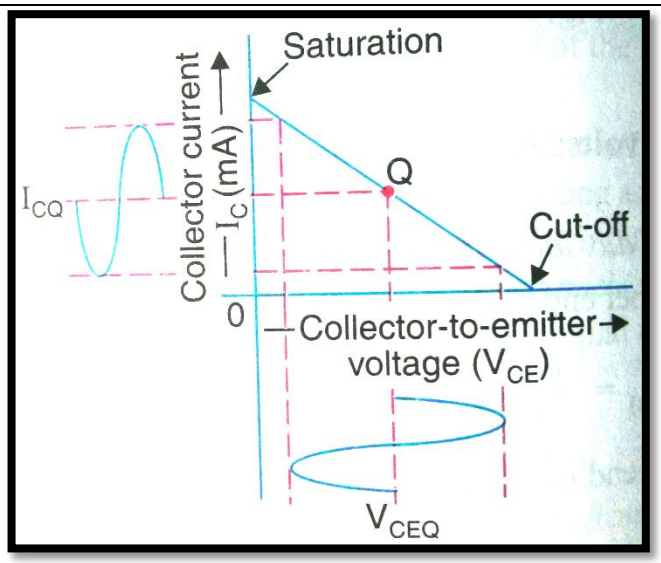
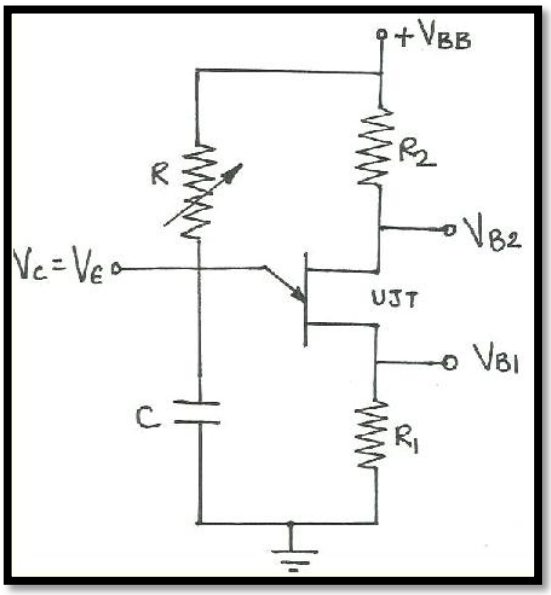
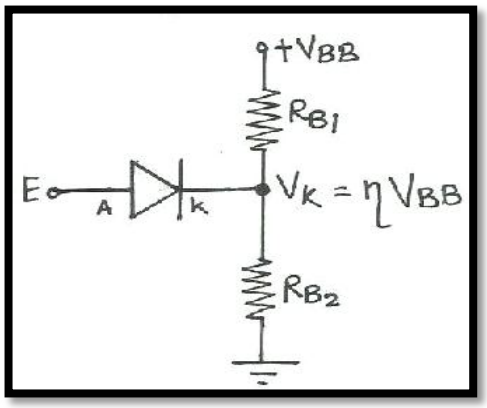
PHASE REVERSAL / WORKING:

- Consider above common emitter amplifier circuit. The input a.c. signal is applied across the base emitter terminals of the transistor & output is taken across collector emitter terminals of the transistor. VBB supply forward biases the emitter base junction & VCC supply reverse biases the output junction.
- Now apply KVL to collector to emitter loop'

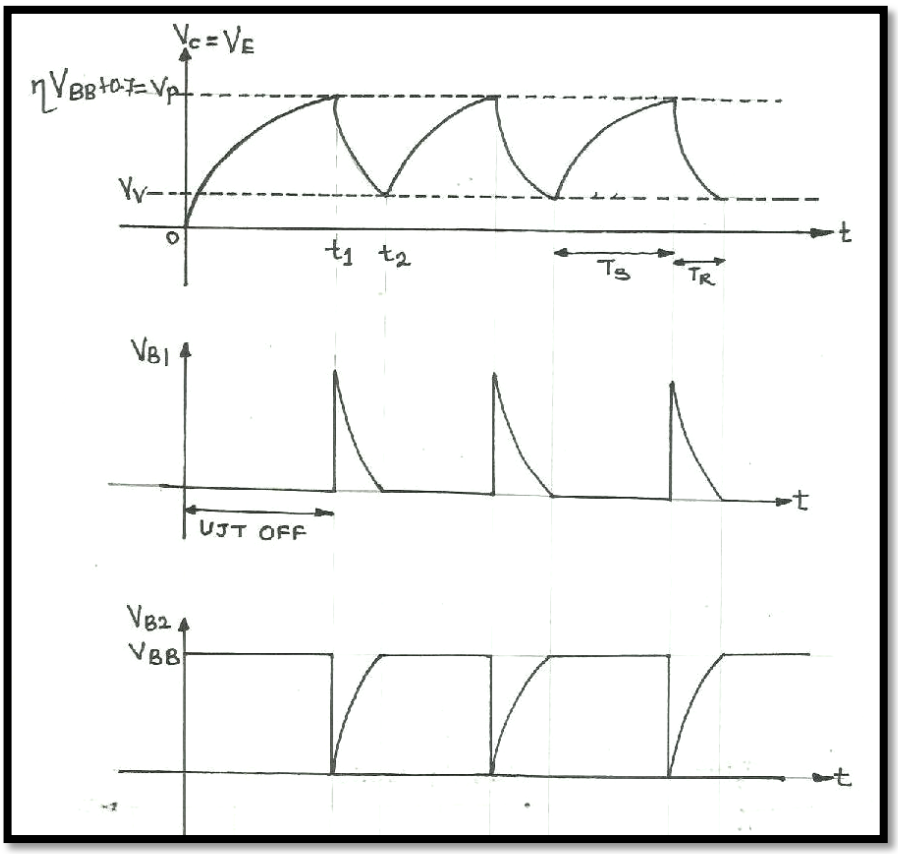
VCC – IC RC – VCE = 0.

∴ VCC – IC RC = VCE ---------- (1)

- When the input a.c. signal voltage increases, the base current increases as a result collector current increases (as IC = β I_B). Hence voltage drop IC RC increases. As VCC is constant, from equation 1 output voltage VCE decreases.
- From above in common emitter amplifier when the input increases in the positive, the output voltage decreases. i.e. output is 180° out of phase with input.
- Graphically phase reversal is shown as below.

			
	e)	**With the help of circuit diagram explain UJT relaxation oscillator with necessary waveforms.**	**4M**
	Ans:	**<u>UJT relaxation oscillator:</u>** **<u>Circuit diagram:</u>**  	**Diagram: 2M, Working:1 M, Waveforms :1M**

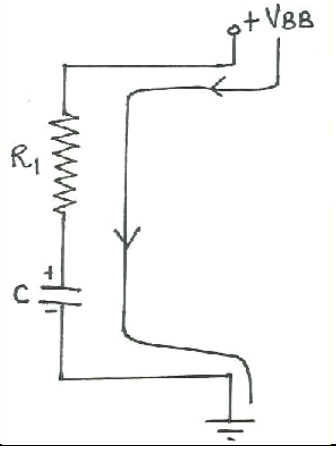
WAVEFORMS:



At t = 0:

- Supply voltage + $V_{BB}$is given the circuit then $V_C = V_E = V_A = 0$ Volts
- By internal potential divider voltage at cathode is
- $V_K = + \eta V_{BB.}$
- If V_A (V_E) < V_K, then internal PN junction (diode) is reverse biased.
- Therefore, it acts as open switch and UJT is OFF.

At, t >0 :



- Current flows from + V_{BB} to ground through resistor R1 and capacitor C. Thus capacitor starts charging exponentially as constant voltage source + V_{BB} is applied.
- Hence in waveform from t = 0, and t > 0, $V_C = V_E$increasing exponentially.
- Therefore no current flows through UJT.
- $\therefore V_{R1} = I.R1 = 0$

$\therefore V_{B1} = 0.$

At t > 0,

- $V_{B2} = V_{BB} - V_{R2}$
- $\therefore V_{B2} = V_{BB}$ ----- (Since $V_{R2} = I.R2 = 0$ as I = 0)

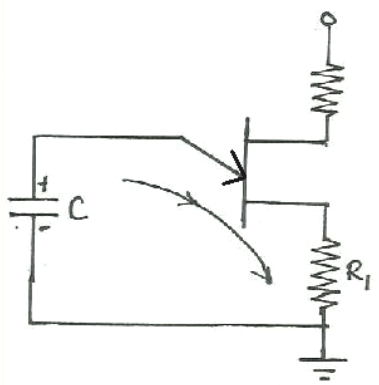
At $t = t_1$:

- Increasing voltage across capacitor is now become $V_C = (\eta V_{BB} + 0.7)$ Volts.Which is equal to anode voltage from equivalent circuit.

$\therefore V_C = V_E = V_A = (\eta V_{BB} + 0.7)$ Volts.

- As $V_A > V_K$ internal PN junction (diode) is forward biased hence it acts as a closed switch, and UJT is ON i.e. UJT starts conducting.
- $V_{B1} = V_{R1}$ = maximum and $V_{B2} = V_{BB} - V_{R2} = 0$

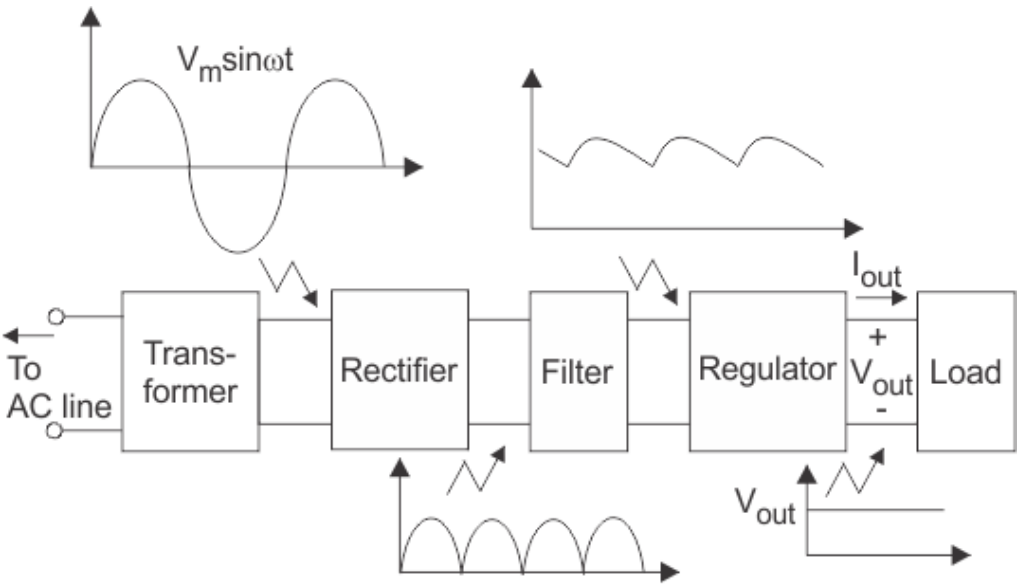
At $t > t_1$:

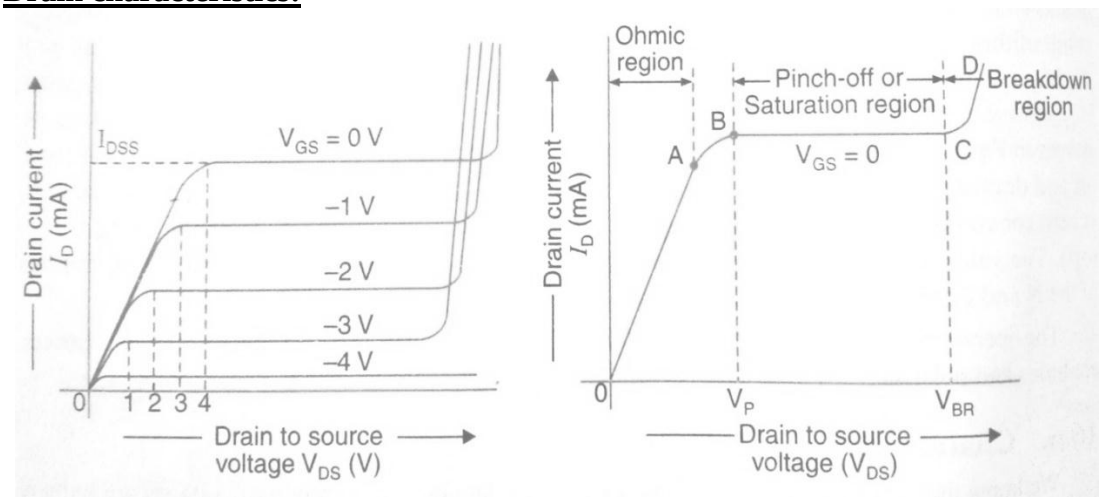
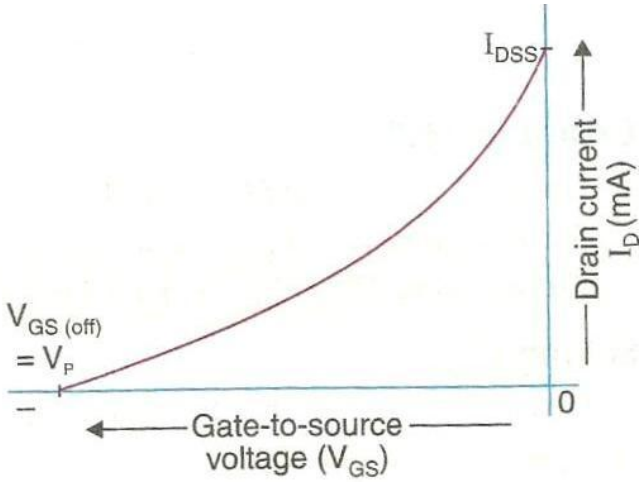


- Charged capacitor finds path for discharging. Charged capacitor discharges exponentially through ON UJT & resistor R1. i.e. V_c decreases.
- As $V_{B1} = V_c$, therefore V_{B1} also starts decreasing exponentially.

At $t = t_2$:

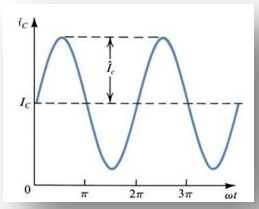
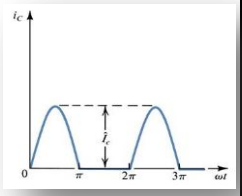
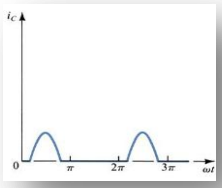
- Decreasing capacitor voltage reached to a point where VA = Vk (as VC = VE= VA)
- ∴ Again internal PN junction (diode) reverse biases.
- Therefore UJT is OFF & no current flows through it.
- Therefore all the waveforms continuously repeat themselves.

	f)	**Draw block diagram of DC regulated power supply and explain each block in detail.**	**4M**
	Ans:	**Block diagram of a regulated dc power supply-**  Components of typical linear power supply 1. A step down transformer 2. A rectifier 3. A DC filter 4. A regulator **Step Down Transformer** A step down transformer will step down the voltage from the ac mains to the required voltage level. The turn's ratio of the transformer is so adjusted such as to obtain the required voltage value. The output of the transformer is given as an input to the rectifier circuit. **Rectification** Rectifier is an electronic circuit consisting of diodes which carries out the rectification process. Rectification is the process of converting an alternating voltage or current into corresponding direct (dc) quantity. The input to a rectifier is ac whereas its output is unidirectional pulsating dc. Usually a full wave rectifier or a bridge rectifier is used to rectify both the half cycles of the ac supply (full wave rectification) **DC Filter** The rectified voltage from the rectifier is a pulsating dc voltage having very high ripple content. But this is not we want, we want a pure ripple free dc waveform. Hence a filter is used. Different types of filters are used such as capacitor filter, LC filter, Choke input filter, π type filter.	**Diagram: 2M, Explain:2M**

		Regulator This is the last block in a regulated DC power supply. The output voltage or current will change or fluctuate when there is change in the input from ac mains or due to change in load current at the output of the regulated power supply or due to other factors like temperature changes. This problem can be eliminated by using a regulator. A regulator will maintain the output constant even when changes at the input or any other changes occur. Transistor series regulator, Fixed and variable IC regulators or a zener diode operated in the zener region can be used depending on their applications. IC's like 78XX and 79XX are used to obtained fixed values of voltages at the output. With IC's like LM 317 and 723 etc we can adjust the output voltage to a required constant value.	
Q. 4	**A)**	**Attempt any FOUR :**	**16 – Total Marks**
	a)	**Draw labelled drain and transfer characteristics of JFET.**	**4M**
	Ans:	**Drain characteristics:**  	**2M**
		Transfer characteristics:  	**2M**
	b)	**Compare class A, class B, class C power amplifier on the basis of**	**4M**

(i) Operating pt. (ii) Efficiency (iii) Conduction angle (iv) nature of OIP waveforms.

Ans:

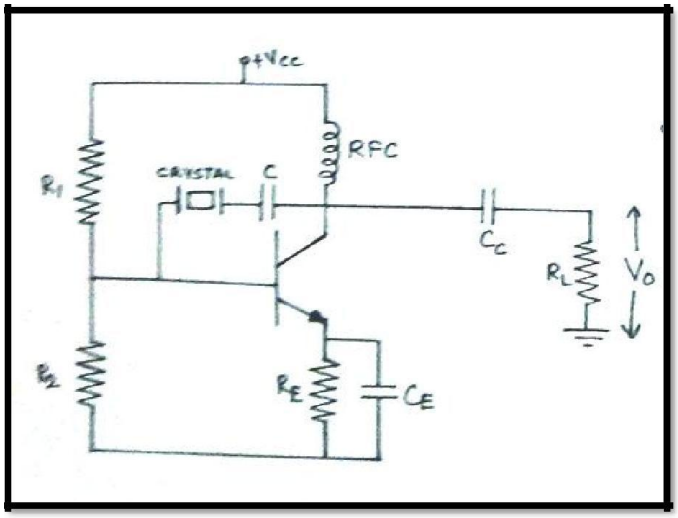
Sr. No.	Parameter	Class A	Class B	Class C
1	Operating pt.	Centre of DC load line	On the X-axis(in cut –off region)	Below X-axis(below
2	Efficiency	Lowest 25% to 50%	Higher (78.5%)	Very high 95%
3	Conduction angle	360^0 or full cycle	180^0 or half cycle	Less than 180^0
4	Nature of OIP			

Each point : 1M

c) Draw neat circuit of crystal oscillator and give significance of piezoelectric effect. **4M**

Ans:

Circuit Diagram of Crystal Oscillator:

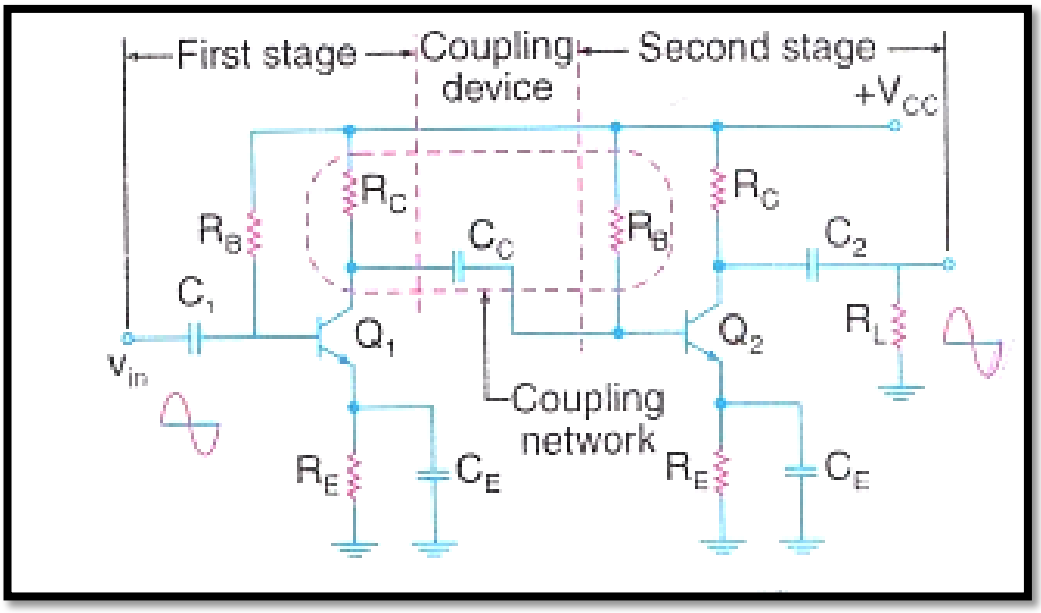
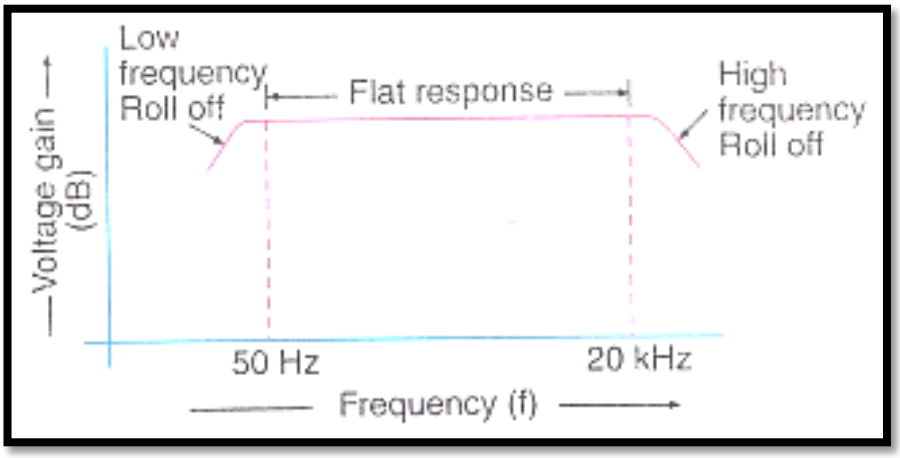


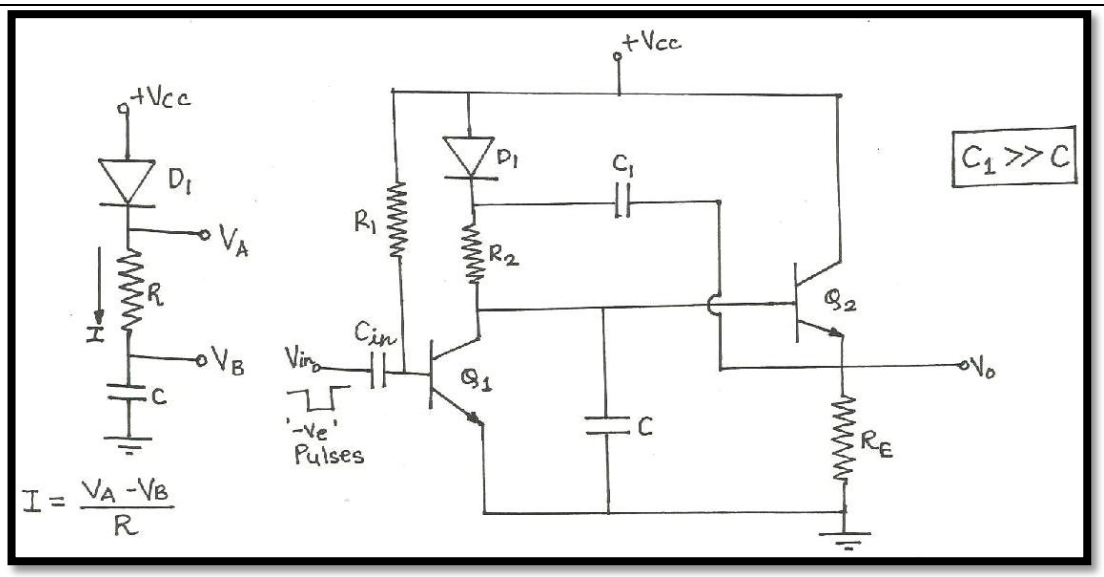
Circuit diagram:2 M, Piezoelectric effect : 2M

Piezoelectric effect :

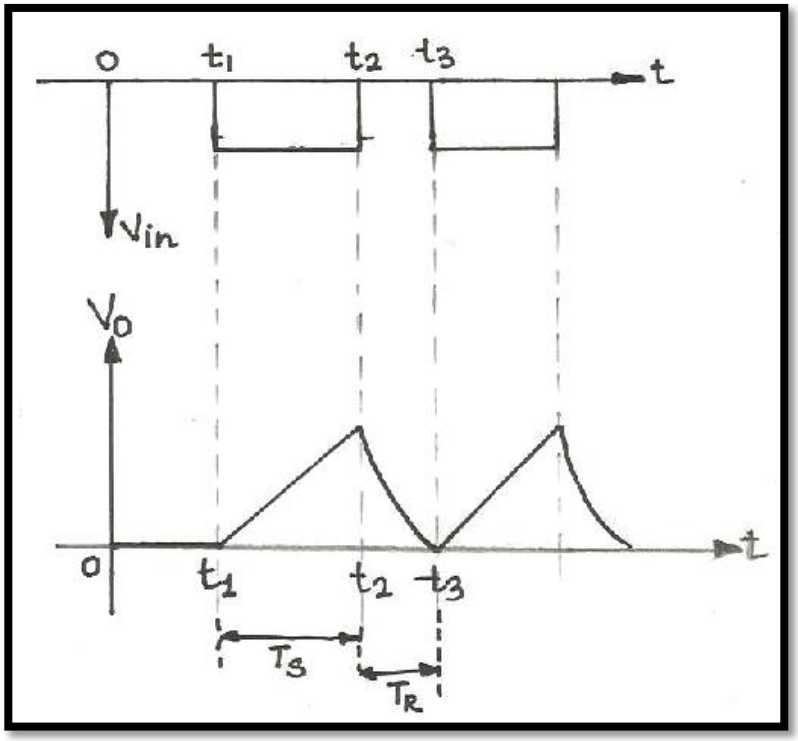
Crystal exhibits a property called as piezo-electric property, which states that:
When the crystal is placed across an ac source, it starts vibrating. The amount of vibration depends upon the frequency of the applied voltage (By changing the frequency , we can find a frequency at which the crystal vibrations reach its maximum value & this frequency called as resonant frequency =

$$\frac{1}{2\pi\sqrt{LC}}$$

	d)	**Draw neat circuit of two stage RC coupled amplifier and also draw it's frequency response.**	**4M**
	Ans:	**Circuit Diagram:**  **Frequency Response:**  	**Circuit diagram:2 M, Frequency Response: 2M**
	e)	**Describe working of Bootstrap time base generator with neat diagram and waveforms.**	**4M**
	Ans:	**Circuit diagram:**	**Diagram :2M, Waveform: 1M, Working : 1M**



Waveforms:

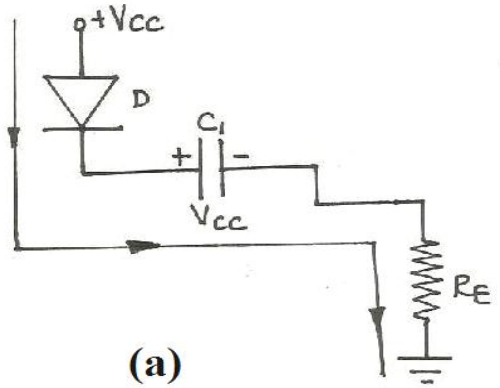


Working:

At t = 0 :

- Input is not given to the base of transistor Q_1. Only V_{CC} applied.
- Resistor values R_1& R_2 are so selected that Q_1 goes into saturation & acts as a close switch.

- Due to this capacitor C is prevented from charging (current flows through Q_1 & goes to ground).
- $\therefore V_{C1} = V_{B2} = 0.2\ V = V_{CE\ (sat).}$
- Therefore transistor Q_2 goes into cut off.
- In the above circuit Q_2 is working as emitter follower & hence output voltage V_O is taken across resistor R_E.
- Since Q_2 is off, therefore its emitter current is zero.
- Hence voltage drop across R_E = output voltage = $I_E * R_E = 0$ volts.
  So from t=0 to $t<t_1$,
  Q_1 = ON; $V_{C1} = 0.2\ V = V_{CE\ (sat)}$
  Q_2 = OFF; $V_O = V_{RE} = 0$ volts
  & current direction in circuit is shown below:

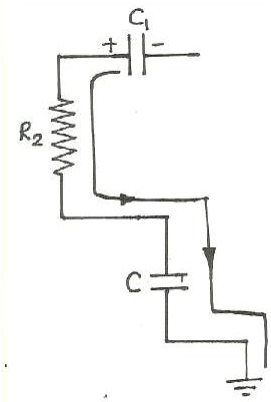


(a)

- Now, as shown in above figure (a), C1 charging through resistor (RF + RE) where RF is forward resistance of diode.
- Since both these resistors are small value, charging current is high. ∴C1 charges quickly to +VCCvolts.
- For diode now, VA = VK = +VCC
- Due to this diode is reverse biased & acts as open switch. Hence the above current stops flowing immediately.

At $t = t_1$

- Negative input pulse '-Vin' of sufficient magnitude is given to the base of Q1.Therefore transistor Q1 goes into cutoff & acts as open switch. ∴Capacitor C is now allow to charge through resistor R2. But in this case DC supply voltage used is the charged C1. Which is also equal to +VCC.



NOTE: Diode D is reverse biased &∴ acts as open switch. When C starts charging but $C_1 >> C$

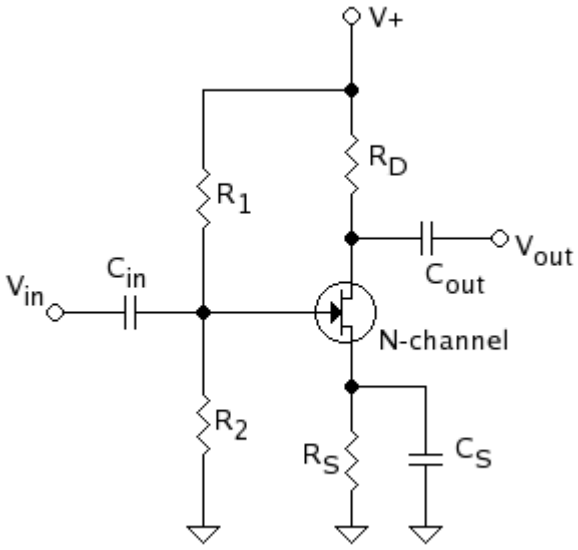
∴ C_1 does not discharge appreciable]

- The voltage across capacitor C now starts increasing, which is also a base voltage of Q_2.
- Since Q_2 is working as emitter follower, its emitter voltage $V_{E2} = V_O$ follows base voltage = V_C
- Hence emitter voltage also starts increasing as capacitor C starts charging.
- This V_O is fed back by capacitor C_1 to top point of R_2 (point A) & due to this voltage at point A as well as voltage at point B increases by same amount.
- Now, voltage drop across $R_2 = V_A - V_B$ remains constant. Due to this charging current through R_2 remains constant.
- Hence capacitor C charges linearly due to constant current source.
- Therefore as shown in waveform from $t = t_1$ to $t < t_2$ output voltage increases linearly with time.

At $t = t_2$ to $t = t_3$

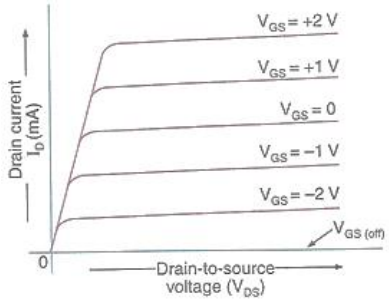
- At t = t2 '-Vin' is removed &∴ Q1 now once again goes into saturation & acts as close switch. The charged capacitor C now quickly discharges through saturation resistor (RSat) of transistor Q1 which is small.
- Hence VO reduces to zero in TR time which is very small. As R2>RSatTs> TR.

	f)	**Draw and explain common source FET amplifier.**	**4M**
	Ans:	**Circuit Diagram:**	**Diagram : 2M** **Explanation : 2M**



- Above circuit shows CS N-channel FET amplifier.
- Voltage divider biasing circuit is used.
- C_1 & C_2 are coupling capacitors used to couple input AC signal & output respectively.
- C_S is a bypass capacitor which keeps the source of FET effectively.

Operation:

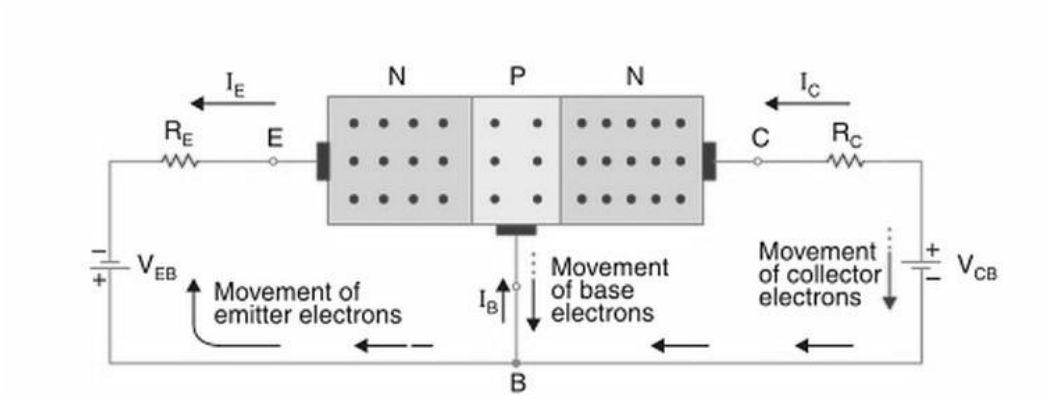


DURING POSITIVE HALF CYCLE:

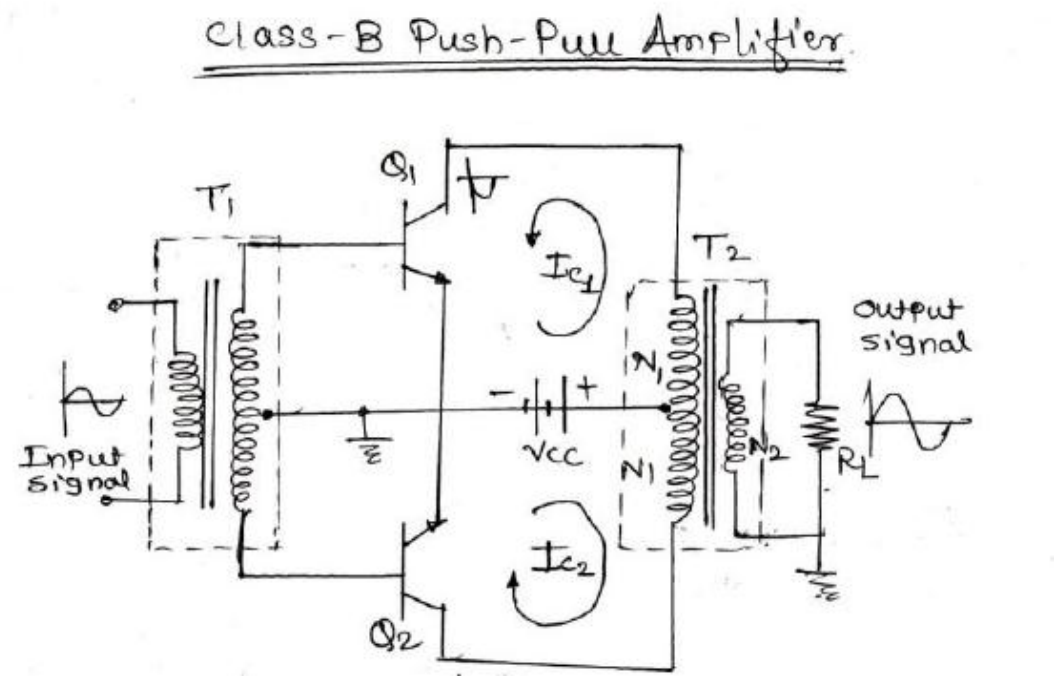
- As the gate to source voltage increases, the drain current also increases.
- As a result of this, the voltage drop across resistor R_D also increases.
- This causes the drain voltage to decrease. As $V_{DS} = V_{DD} – I_D R_D$.
- It means that the positive half cycle of the input produces negative half cycle of the output voltage.
- In other words output voltage is 180° out of phase with the input voltage.

DURING NEGATIVE HALF CYCLE:

- As the gate to source voltage decreases, the drain current also decreases.
- As a result of this, the voltage drop across resistor R_D also decreases.
- This causes the drain voltage to increase. As $V_{DS} = V_{DD} – I_D R_D$.
- It means that the negative half cycle of the input produces positive half cycle of the output voltage.

		• In other words output voltage is 180° out of phase with the input voltage.	
Q.5		**Attempt any FOUR :**	**16 – Total Marks**
	a)	**Explain operation of NPN transistor with neat constructional diagram.**	**4M**
	Ans:	**Diagram :**  **Explanation:** • The construction for a bipolar NPN transistor is shown above. The voltage between the Base and Emitter (V_{BE}), is positive at the Base and negative at the Emitter because for an NPN transistor, the Base terminal is always positive with respect to the Emitter ie. the emitter base junction is forward biased. Also the Collector supply voltage is negative with respect to the Base (V_{CB}) ie. collector-base junction is reverse biased. • The forward bias on the emitter base junction causes the electrons in the emitter region to flow towards base region. This constitutes I_E. • The electrons after reaching in the base region tend to combine with the holes and they constitute I_B. • However most of the electrons do not combine with the holes in the base region. It is due to the fact that base width is made extremely small and lightly doped and hence electrons do not get sufficient holes for recombination. Thus most of the electrons diffuse to the collector regions and constitute I_C. • The relation between I_E, I_B and I_C is, $I_E = I_B + I_C$	**Diagram : 2M** **Explanation : 2M**
	b)	**Define parameters of JFET** **(i) rd** **(ii) gm** **(iii) μ and** **Derive relation between them.**	**4M**
	Ans:	**Definitions** : i) Drain resistance (rd) : It is defined as ratio of drain to source voltage to drain	**Definitions : 3M**

		current for constant gate to source voltage. rd = $\Delta V_{DS}/\Delta I_D$ keeping constant V_{GS} ii) Transconductance (gm) : It is defined as ratio of change in drain current (ΔI_D) to the corresponding change in gate to source voltage (V_{GS}) at a constant value of drain to source voltage (V_{DS}) gm = $\Delta I_D/\Delta V_{GS}$ keeping Constant V_{DS} iii) Amplification factor (μ) It is defined as the ratio of change in drain to source voltage (V_{DS}) to change in the gate to source voltage (V_{GS}) at a constant value of I_D. μ = $\Delta V_{DS} / \Delta V_{GS}$ keeping I_D constant. **Relation between μ, gm and rd:** From definitions, μ = $\Delta V_{DS} / \Delta V_{GS}$ ..... i) gm = $\Delta I_D / \Delta V_{GS}$..... ii) rd = $\Delta V_{DS} / \Delta I_D$ .... iii) Multiply and Divide eq i) by ΔI_D μ = ($\Delta I_D / \Delta V_{GS}$) * ($\Delta V_{DS} / \Delta I_D$) i.e μ =gm * rd (from ii & iii)	**Relation : 1M**
	c)	**Explain working of class B push pull amplifier with i/p and output waveforms.**	**4M**
	Ans:	• In class B amplifier transistor conducts only for half cycle of input signal. This type of output signal gives large distortion. In order to avoid this we use two transistors connected in push-pull arrangement. One conducts in positive half cycle and other conducts in negative half cycle. • Transistor T1 is called as input transformer and is called phase splitter and produces two signals which are 180º out of phase with each other. Transistor T2 is called output transformer and is required to couple the a.c. output signal from the collector to the load.	**Diagram : 1M** **Explanation : 2M** **Waveforms :1M**



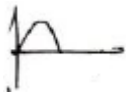
Working:

- When there is no input signal both the transistor Q1 and Q2 are cut-off. Hence no current is drawn from VCC supply. Thus there is no power wasted in standby the power dissipation in both transistor is practically zero.
- During positive half cycle the base of Q1 is positive and Q2 is negative. As a result of this Q1 conduct, while the transistor Q2 is OFF. And at the output half cycle is obtained.
- During negative half cycle, Q1 turns OFF and Q2 conducts, and another half cycle is obtained at the output. At any instant only one transistor in the circuit is conducting. Each transistor handles one half of the input signal.
- Then output transformer joins these two halves and produces a full-sine wave in the load resistor.

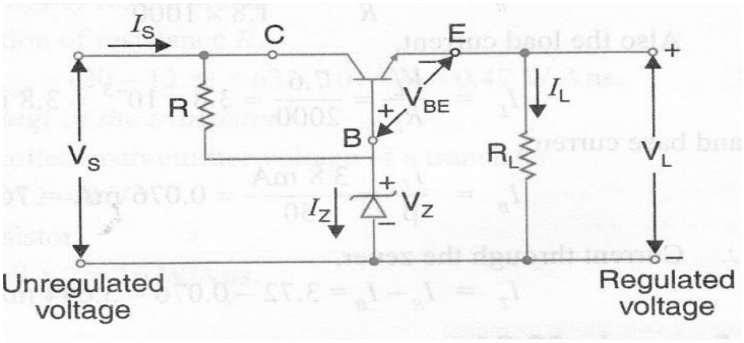
Input and output waveforms-

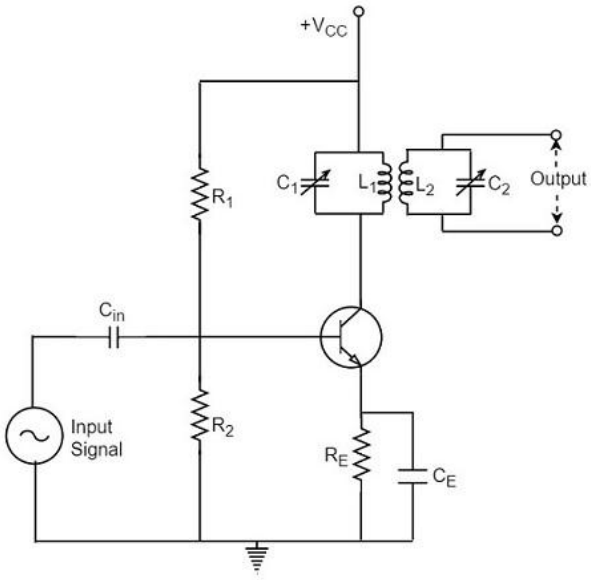
Input signal

When Q1 conducts

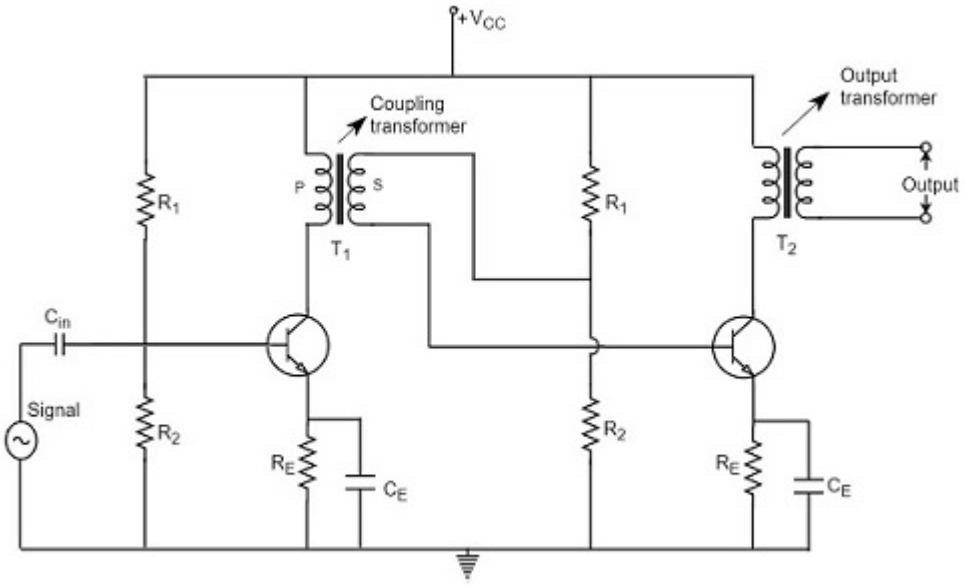


When Q2 conducts

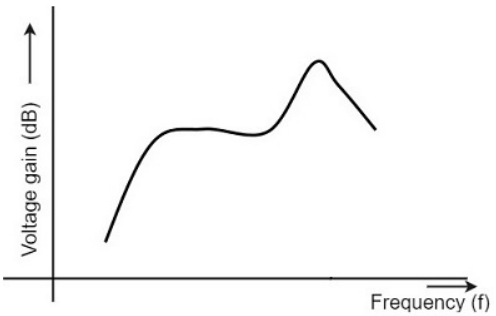
		Ouput signal 	
	d)	**Enlist different types of time base generator. Write any four applications of it.**	**4M**
	Ans:	**<u>Different types of time base generator: (Any two)</u>** **1)** Voltage time base generator. **2)** Current time base generator. **3)** Millers Sweep Generator. **4)** Saw Tooth Generator. **5)** Bootstrap Time base generator. **<u>Applications of time base generator:</u>** **1)** TV receivers. **2)** Frequency synthesizer. **3)** In the electron beam deflection system in cathode ray tube. **4)** In screen deflection system of a radar.	**Types : 2M** **Applications : 2M (1/2 m each for any four)**
	e)	**Draw and explain transistorized series voltage regulator.**	**4M**
	Ans:	**<u>Diagram :</u>**  **<u>Explanation :</u>** • In this circuit transistor acts as a control element. This transistor is connected in series with the load hence the circuit is called as Series Voltage Regulator. Other components in the circuit are Zener diode (V_Z), and resistor R. • Zener diode V_Z is operated in breakdown region and provides constant voltage V_Z. • As V_Z & V_{BE} of the transistor are constant, output voltage across R_L will also be constant. To find output voltage V_O, Applying KVL to o/p loop of the circuit $V_{BE} + I_L R_L - V_Z = 0$ Therefore, $V_O = I_L R_L = V_Z - V_{BE}$ $V_O = V_Z - V_{BE}$	**2M** **2M**

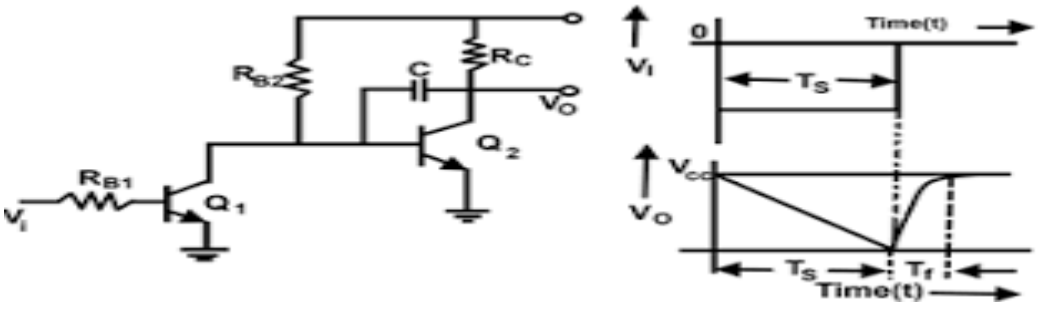
		If output voltage increases then V_{BE} decreases. Due to reduction in V_{BE}, I_B decreases and I_C decreases. This will increase the collector to emitter voltage across the transistor and V_O will be regulated this is because $V_O = Vin - V_{CE}$ If the output voltage decreases, then exactly opposite action will take place and the output voltage is regulated.	
	f)	**Draw neat circuit diagram of double tuned amplifier. Write any two advantages and two applications of it.**	**4M**
	Ans:	**Circuit diagram:**  **Advantages of double tuned amplifier:** **1)** Better frequency response. **2)** Bandwidth is increased. **3)** Sensitivity is increased. **4)** Better Selectivity. **Applications of double tuned amplifier:** **1)** Used for coupling the various circuits of radio and television receivers. **2)** Intermediate frequency (IF) amplifiers in radio receivers.	**2M** **Advantages : 1M (any two 1/2 m each)** **Applications : 1M (any two 1/2 m each)**
Q.6		**Attempt any FOUR :**	**16 – Total Marks**
	a)	**List any four advantages of negative feedback.**	**4M**
	Ans:	**Advantages of negative feedback** 1) Less amplitude distortion 2) High stabilized gain 3) Higher fidelity 4) Less phase distortion 5) Noise reduces	**Advantages (any 4) : 4M**

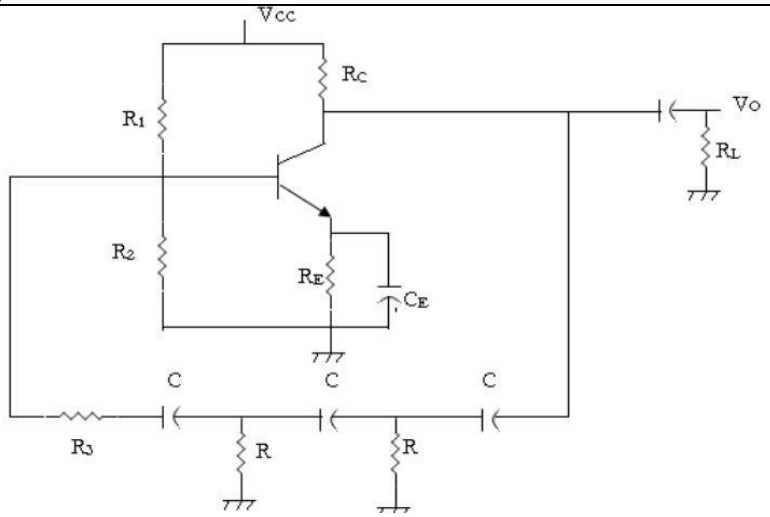
		6) Increased bandwidth 7) Less frequency distortion	
	b)	**Define:** **(i) Load Regulation** **(ii) Line Regulation**	**4M**
	Ans:	**(i) <u>Load Regulation</u>** The load regulation indicates the change in output voltage that will occur per unit change in load current. Mathematically, $\% L.R = \frac{V_{NL}-V_{FL}}{V_{FL}} * 100$ where, V_{NL} = Load voltage with no load current V_{FL} = Load voltage with full load current **(ii) <u>Line Regulation</u>** The line regulation or source regulation rating of a voltage regulator indicates the change in output voltage that will occur per unit change in the input voltage. Mathematically, $\% S.R = \frac{V_{HL}-V_{LL}}{V_N} * 100$ where, V_{HL} = Load voltage with high line voltage V_{LL} = Load voltage with low load current V_N = output voltage under normal operating conditions	**Definition : 2M each**
	c)	**Draw neat circuit of two stage transformer coupled amplifier and draw it's frequency response.**	**4M**
	Ans:	**<u>Circuit Diagram :</u>**	**Circuit Diagram : 2M** **Response : 2M**

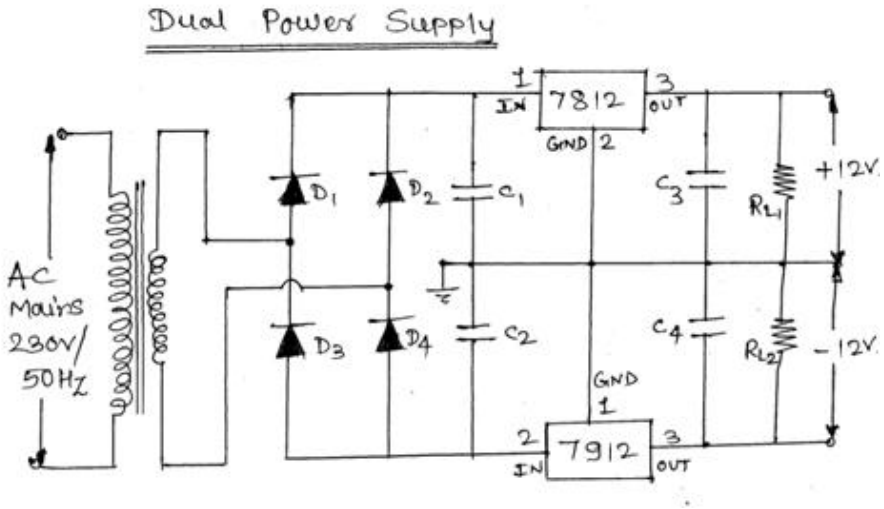


Response :



	d)	**Draw neat circuit of Miller sweep generator and explain it with waveforms.**	**4M**
	Ans:	 **Working:** Figure shows the circuit of a Miller integrator or a sweep circuit. Transistor Q1 acts as a switch and transistor Q2 is a common - emitter amplifier. i.e. a high gain amplifier. Consider the case when Q1 is ON and Q2 is OFF. At this condition, the voltage across the capacitor C and the output voltage Vo is equal to Vcc. When a negative pulse is applied to the base of Q1, the emitter - base junction of Q1 is reverse biased and hence Q1 is turned OFF. Thus, the collector voltage (Vc1) of Q1 increases which increases the bias to Q2 and as a result Q2 is turned ON. Since	**Circuit Diagram : 1M** **Working 2M** **Waveform :1M**

		Q2 conducts, Vo begins to decrease. Because the capacitor is coupled to the base of transistor Q2, the rate of decrease of output voltage is controlled by rate of discharge of capacitor. The time constant of the discharge is given by td = $R_{B2*}C$. As the value of time constant is very large, the discharge current practically remains constant. Hence, the run down of the collector voltage is linear. When the input pulse is removed, Q1 turns ON and Q2 turns OFF. The capacitor charges quickly to +Vcc through Rc with the time constant t =R_C*C.	
	e)	**Describe working of RC phase shift oscillator with neat sketch. Write formula for frequency of oscillation.**	**4M**
	Ans:	 **Working-** • The circuit consist of a single stage amplifier in C.E configuration and the RC phase shifting network consisting of three identical RC sections. • The resistors R_1, R_2 and R_E are connected for transistor biasing. C.E is the emitter bypass capacitor. • As shown in diagram the output V_O of single stage C.E amplifier has been connected as an input to the RC phase shifting network. • The output of the phase shifting network is connected at the input of the amplifier. • As amplifier is C.E type, it introduces a phase shift of 180º between its input and output. The additional 180º phase shift is introduced by the RC phase shift network . • The phase shift around the loop will be precisely equal to 360º . The gain of the amplifier and feedback factor β are adjusted properly to have a loop gain Aβ ≥ 1 , then sustained sinusoidal oscillations will be obtained at the oscillator output. Frequency of oscillation is given by, $$f = \frac{1}{2\pi(\sqrt{6})CR}$$	**Circuit Diagram : 1M** **Working 2M** **Formula :1M**
	f)	**Draw neat circuit of DC regulated dual power supply for ± 12 V using IC 78 XX**	**4M**

		&IC 79 XX.	
	Ans:	**Diagram :** 	**Diagram : 4M**