Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q.1.

a) Attempt any Three of the following: 12

i. Describe the functions of the following pins of 80386.

1. $\overline{BE_3} - \overline{BE_0}$
2. $M/\overline{IO}$
3. $\overline{ADS}$
4. $\overline{BS16}$

Ans: (One mark per function of pin)

1. $\overline{BE_3} - \overline{BE_0}$ **(Bus/byte enable signal)**
The 32-bit Data bus supported by 80386 and the memory system of 80386 can be viewed as a 4-byte wide memory access mechanism. The four byte enable lines, $\overline{BE_3} - \overline{BE_0}$, may be used for enabling these four banks. Using these four enable signal lines, the CPU may transfer 1 byte/2bytes/3bytes or 4bytes of data simultaneously.

2. $M/\overline{IO}$ **(Memory / input output (#)) :Output signal**
This output pin differentiates between the memory and I/O cycles. If it is low, microprocessor is performing IO function and if high it is performing memory function.

3. $\overline{ADS}$ **(address strobe signal :active low : output signal)**
The address status output pin indicates that the address bus and bus cycle definition (w/R#, D/C#, M/IO#, BE_0#-BE_3) are carrying the respective valid signals. The 80386 does not have any ALE signal and so this signal may be used for latching the address to external latches.

4. $\overline{BS16}$ **(bus size 16: active low :input signal)**
The bus size-16 input pin allows the interfacing of 16-bit devices with the 32-bit wide 80386 data bus. Successive 16-bit bus cycles may be executed to read a 32-bit data from a peripheral.

ii. What is multimedia extension?

Ans: (Explanation 4M)

1. Intel introduced the MMX(multimedia extension) technology at a atime when there was a tremendous need to improve the 2-D and 3-D imaging for multimedia applications.
2. Most of the algorithms in multimedia applications involve operations on several pixels (picture call) simultaneously.
3. A pixel of an image may be represented by a 24-bit quantity. Similarly, in case of a black and white image, a pixel may be represented by an 8-bit number.
4. Most of the image processing algorithms and images compression techniques required for involves operations on multiple numbers of pixels simultaneously.
5. Thus most of the multimedia applications require SIMD (single Instruction stream Multiple Data Stream) kind of architecture. This is precisely what Intel provides through a set of the 57 MMX instructions.
6. These instructions help the programmer to write efficient programs for image filtering, image enhancement, coding and other algorithms.
7. Using conventional CPUs, we can operate on two pixels at the most, concurrently. Using MMX instruction set, on the other hand, we can load eight pixels simultaneously and perform concurrent operations on them.

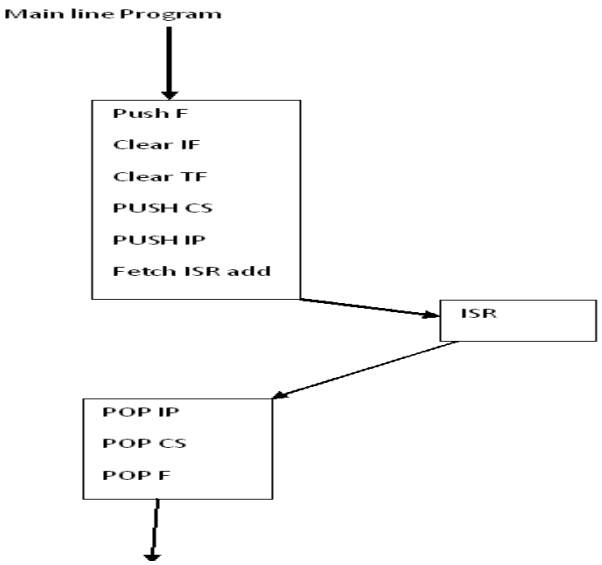
iii. How the interrupt is processed in X86 processor?

Ans: (Explanation 4 Marks for the steps , Diagram optional : if drawn 1 mark can be given to the diagram)

Interrupt processing sequence of 8086

1) It decrements stack pointer by 2 & push flag register on stack.
2) It clears the interrupt request by clearing interrupt flag.
3) It also reset trap flag in flag register.
4) Decrement stack pointer by 2 & store code segment in it.
5) Decrement stack pointer by 2 & pushes IP in it.
6) If fetches the ISR & jumps on it.

After the completion of ISR, it decodes the instruction IRET & retrieves the main program address & status of flag register.



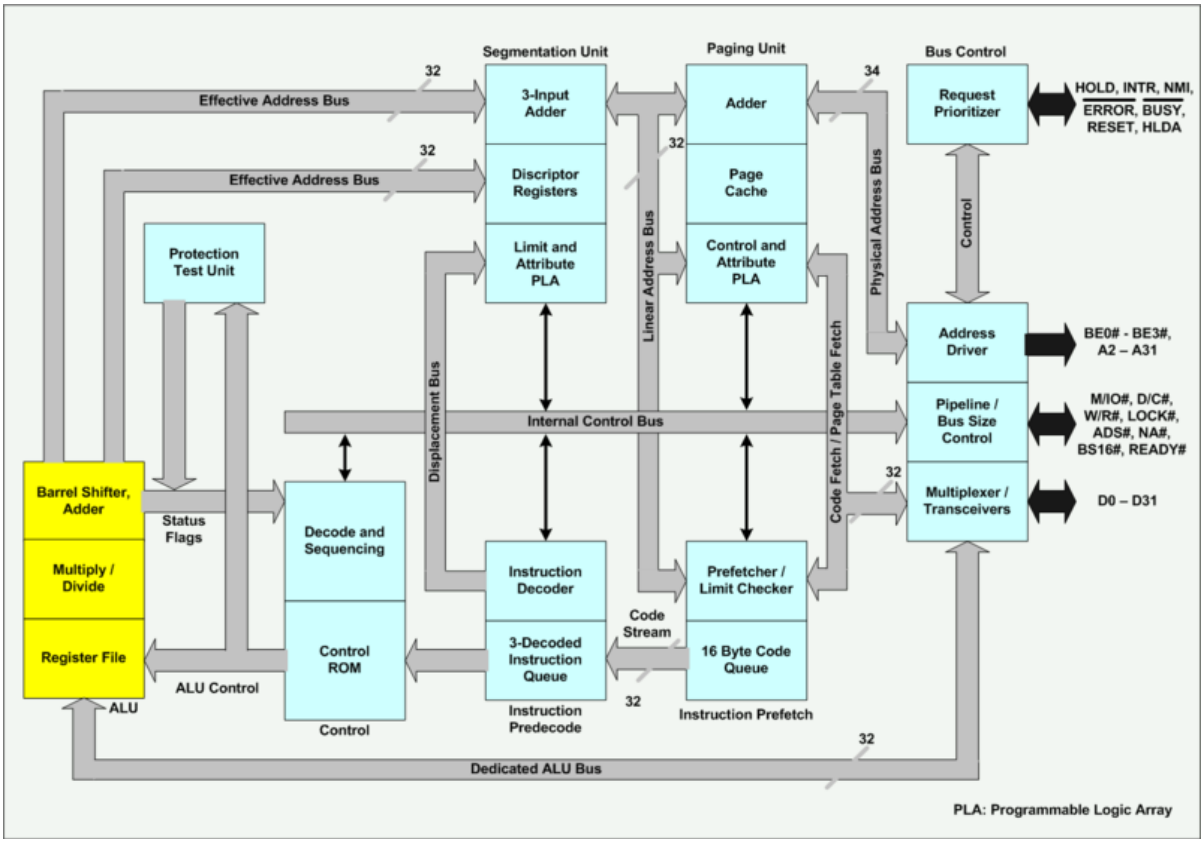
iv. Write any four advantages of RISC processor.

Ans: (Any four Points 4 Marks, any relevant advantages can be given marks)

1. RISC instructions, being simple, can be hard wired.
2. A set of simple instructions results in reduced complexity of the control unit and the data path; as a consequence, the processor can work at a high clock frequency and thus yield higher speed.
3. As a result several extra functionalities, such as memory management units or floating point arithmetic units, can also be placed on the same chip.
4. Smaller chips allow a semiconductor manufacturer to place more parts on a single silicon wafer, which can lower the per-chip cost dramatically.
5. High level language compilers produce more efficient code in RISC processor than its counterpart CISC processor, because they tend use the smaller set of instructions in a RISC computer.
6. Shorter design cycle- a new RISC processor can be designed, developed as tested more quickly since RISC processors are simpler than corresponding CISC processors.
7. The application programmers who use the microprocessor's instructions will find it easier to develop code with smaller and optimized instructions set.
8. Another advantage is that the loading and decoding of instructions in a RISC processor is simple and fast, as it is not needed to wait until the length of an instruction is known in order to start decoding the following one. Decoding is simplified as opcode and address fields are located in the same position foe all instructions.

b) Attempt any ONE of the following: 6

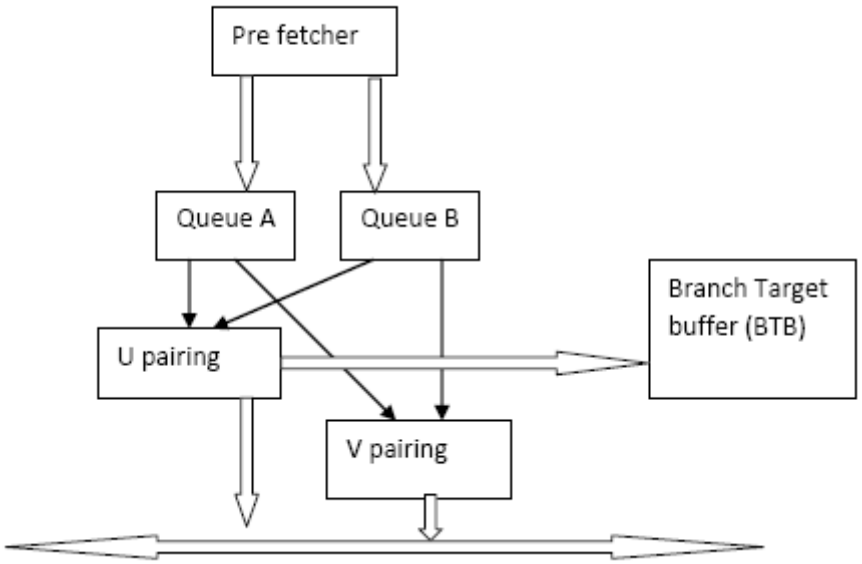
i. Draw the neat labeled architecture of 80386.
Ans : (Neat Labeled diagram 6 M)



ii. With neat sketch describe the branch prediction logic in Pentium processor.
Ans: (Diagram: 2 Marks, Explanation 4 Marks)

Branch Prediction Logic:-

The Pentium processor includes branch prediction logic to avoid pipeline stalls, if correctly, predict whether or not branch will be taken when branch instruction is executed if branch prediction is not correct recycle penalty is applicable to u pipeline & 4 cycle penalty if branch is related to v pipeline.
The prediction mechanism is implemented using 4 way set associative cache with 256 entries referred as branch target buffer. Whenever branch is taken CPU enters the branch instruction address & the destination address in BTB. When an instruction is decoded CPU searches the BTB to determine presence of entry. If its present CPU uses precious history to decide to take the branch.



Q.2. Attempt any Four of the following: 16

a) State the functions of Test and debug register of 80386 with the neat diagram.

Ans: (Debug Registers: 1 Mark for diagram, 1Mark for description]

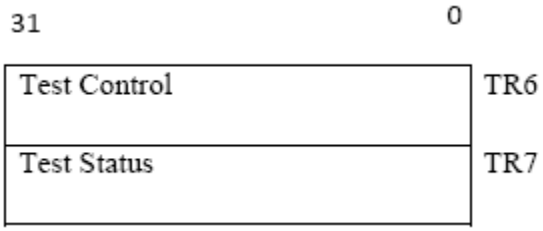
31 0	
Linear Breakpoint Address 0	DR0
Linear Breakpoint Address 1	DR1
Linear Breakpoint Address 2	DR2
Linear Breakpoint Address 3	DR3
Intel Reserved	DR4
Intel Reserved	DR5
Breakpoint Status	DR6
Breakpoint Control	DR7

There are eight debug registers DR0 to DR7 for hardware debugging. The DR0 to DR3 are used to store program controllable breakpoint addresses. The DR4 and DR5 are not used and are reserved by Intel. The DR6 and DR7 are used to hold the breakpoint status and breakpoint control information respectively.

Test registers of 80386: [1 mark for diagram, 1 mark for description]

The 80386 has two test registers for page caching. The registers are TR6 – Test Control and TR7 – Test Status. TR6 & TR7 are used for translation look aside buffer (TLB). TLB holds page table address translation to reduce the no. of memory required for page table translation.

The test registers are used to perform the confidence checking on the paging. TR6 is the TLB testing command register. By writing into this register, you can either initiate a write directly into the TLB or perform a mock TLB lookup. TR7 is the TLB testing data register. When a program is performing writes, the entry to be stored is contained in this register, along with cache set information.



b) List the floating point exception in Pentium.
Ans: (Listing of 6 interrupts : 4 marks)
The Pentium provides six floating point exceptions

1. Invalid operation (#I)
   Stack overflow or underflow (#IS).
   Invalid arithmetic operation (#IA).
2. Divide-by-zero (#Z).
3. Demoralized operand (#D)
4. Numeric overflow (#O)
5. Numeric underflow (#U)
6. Inexact result (precision)(#P).

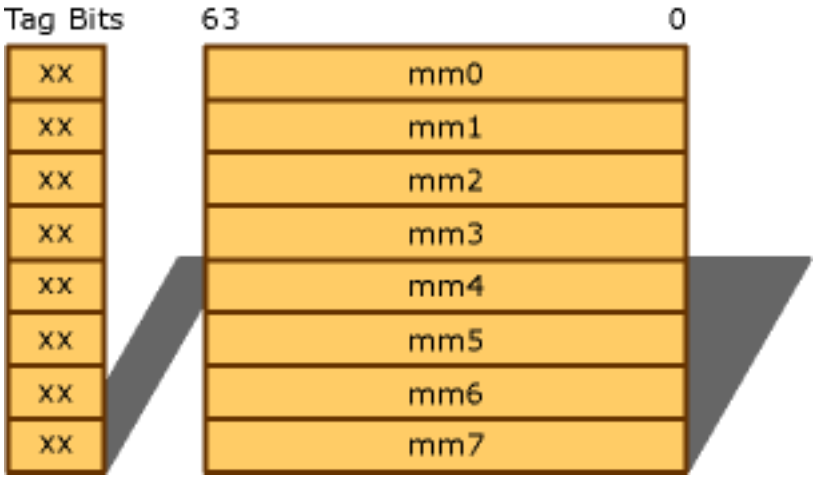
- Each of the six exception classes have a corresponding flag bit in the FPU status word and a mask bit in the FPU control word.

c) What do you mean by hybrid architecture?
Ans: (Explanation of hybrid architecture: 4Marks, any relevant points other than this can be given marks)

1. Till mid 1990's processor design was split into two opposing camps. Some used CISC designs due to its low burden on compiler developers and wide availability of existing software.
2. Others use RISC designs because of its simplicity and efficiency.
3. Today most CISC processors are based on hybrid ISC-RISC architecture. Such hybrid architecture uses a decoder to convert CISC instructions into RISC instructions before execution.
4. These are then processes by a RISC core which performs a few basic instructions very quickly. Also RISC core allows performance enhancing features such as branch prediction and pipelining.
5. These have only been possible in RISC designs, since fixed length instructions are required for such features to work. Example Pentium and Athlon family of processor.
6. These processors are compatible with software developed for their CISC predecessors, yet they perform competitively against processors based on RISC design.
7. A CISC-RISC hybrid continues to consume a lot of power and is not best candidates for mobile and embedded applications.
8. Apart from having RISC core the number of general purpose registers in CISC processor has also grown and allow more instructions to be processes simultaneously.

9. Intel Pentium III with SSE technology has an additional set of eight 128 bit vector registers for running SIMD (single instruction multiple data) instructions.
10. The future successor to Pentium series Intel itanium IA-64 will even raise the bar further by implementing 128 general purpose registers.
11. Many modern RISC processor support more instructions than old CISC designs. Example Motorola G4 processor used in power Macs and eMacs

d) How the intel MMX architecture handles floating points register?
Ans: (MMX registers diagram : 2 marks , explanation : 2 marks)



1. In Pentium there are eight general purpose floating point registers in a floating point unit.
2. Each of these eight registers are 80-bit wide for floating point operations, 64 bits are used for mantissa and rest of 16 bit for exponent.
3. Intel MMX instructions use these floating point registers as MMX registers and used only 64 bit mantissa portion of these registers to store MMX operands.
4. Thus MMX programmers virtually get new MMX registers each of 64bits.
5. It is possible to use same set of registers as floating point registers and MMX register in the same program; it is preferable not to use them concurrently.
6. After a sequence of MMX instruction is executed, these registers should be cleared by an instruction 'EMMS' which implies empty MMX stack.
7. The floating point users should use same instruction after executing floating point instructions.
8. Although content switching between multimedia program execution and floating point execution is permissible. It is not recommended.
9. It is advisable that multimedia program developers should partition MMX instruction into separate library routine.

e) List the hardware and software interrupts.
Ans: (types of hardware interrupts : 2marks, types of software interrupts : 2marks)
(i) Hardware Interrupts (External Interrupts). The Intel microprocessors **support hardware interrupts** through:

Two pins that allow interrupt requests, INTR and NMI

One pin that acknowledges, INTA, the interrupt requested on INTR.

INTR and NMI

INTR is a maskable hardware interrupt. The interrupt can be enabled/disabled using STI/CLI instructions or using more complicated method of updating the FLAGS register with the help of the POPF instruction.

NMI is a non-maskable interrupt. Interrupt is processed in the same way as the INTR interrupt. Interrupt type of the NMI is 2, i.e. the address of the NMI processing routine is stored in location 0008h. This interrupt has higher priority than the maskable interrupt.

– **Ex: NMI, INTR.**

(ii) Software Interrupts (Internal Interrupts and Instructions) .S**oftware interr**upts can be caused by:

INT instruction - breakpoint interrupt. This is a type 3 interrupt.

INT <interrupt number> instruction - any one interrupt from available 256 interrupts.

Single-step interrupt - generated if the TF flag is set. This is a type 1 interrupt. When the CPU processes this interrupt it clears TF flag before calling the interrupt processing routine.

f) Describe any two dedicated interrupts.
(Any Two 4M)

- **INT 0(Divide by zero error)**
  The interrupt with type number 0 is dedicated to the divide by zero error. This interrupt is an 'error generated' interrupt (also called an 'exception'). On division, if the quotient registers is not large enough to contain the quotient. This interrupt is generated automatically. Dedicating type 0 for this case means that the corresponding interrupt vector in the interrupt vector table is available at 0000:0000

- **INT 1 (single stepping)**
  This type number is dedicated for single stepping or trace. Single stepping is an important idea in debugging during logical debugging of our programs. We would like to stop after the execution of each instruction and check the contents of register, memory and so on. We usually perform the action of trace this way. Intel has provided the Trap flag for this, and this flag has to be let this happen. The ISR for viewing the register and memory content will be pointed by the vector of interrupt type 1. However, an important issue in this is how to set the trap flag. No such instruction has been encountered so far. Recollect the flag register configuration.

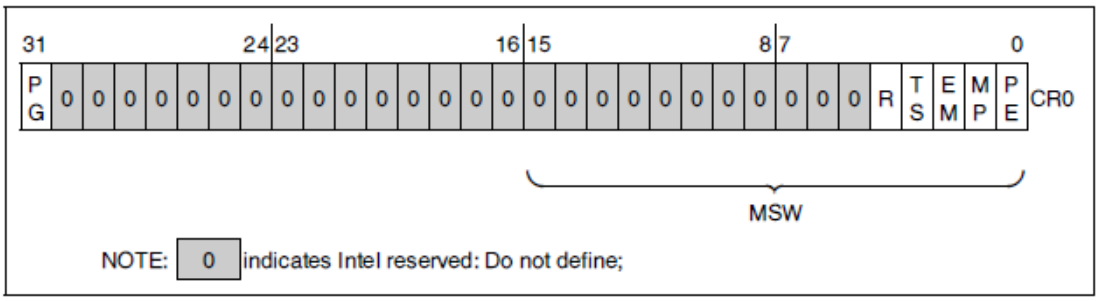
- **INT 2 (Non Maskable Interrupt)**
  This interrupt corresponds to the vector (pointer) of the hardware interrupt NMI. When an interrupt is received on the pin NMI (Non Maskable Interrupt) of the processor, a type 2 interrupt occur- this means that the ISR for NMI must be written in the address pointed by the corresponding IVT content.

- **INT 3 (Breakpoint Interrupt)**
  This is the breakpoint interrupt, which is useful for de-bugging. We will need to set breakpoints (stop after executing a group of instruction) and check the content of registers and memory after executing instructions up to the breakpoint.

- **INT 4 (Overflow Interrupt)**
  This interrupts corresponding to the overflow flag. If the overflow flag is set, this interrupt occurs but not automatically. An instruction INTO (interrupt on overflow) must be written after the program segment which is likely to cause the overflow flag (OF) to be set.

Q.3. Attempt any Four of the following: 16

a) Draw the MSW of 80386 and describe the function of each bit.
Ans: (Diagram of MSW : 2 MARKS , explanation :2 Marks)



Control Register 0

Register CR0 contains a number of special control bits that are defined as follows in the 80386:

PG Selects page table translation of linear addresses into physical addresses when PG = 1. Page table translation allows any linear address to be assigned any physical memory location.

ET Selects the 80287 coprocessor when ET = 0 or the 80387 coprocessor when ET = 1. This bit was installed because there was no 80387 available when the 80386 first appeared. In most systems, ET is set to indicate that an 80387 is present in the system.

TS Indicates that the 80386 has switched tasks (in protected mode, changing the contents of TR places a 1 into TS). If TS = 1, a numeric coprocessor instruction causes a type 7 (coprocessor not available) interrupt.

EM Is set to cause a type 7 interrupt for each ESC instruction. (ESCape instructions are used to encode instructions for the 80387 coprocessor.) We often use this interrupt to emulate, with software, the function of the coprocessor. Emulation reduces the system cost, but it often takes at least 100 times longer to execute the emulated coprocessor instructions.

MP Is set to indicate that the arithmetic coprocessor is present in the system.

PE Is set to select the protected mode of operation for the 80386. It may also be cleared to reenter the real mode. This bit can only be set in the 80286. The 80286 could not return to real mode without a hardware reset, which precludes its use in most systems that use protected mode.

b) What are the advancement available in Pentium pro inline with the Pentium architecture.
(Ans: any 4 advantages of Pentium pro. Any other advantages can be given marks)

- Pentium pro is advanced from Pentium:
- Pentium pro having 12 stages of pipelining.(explain in detail)

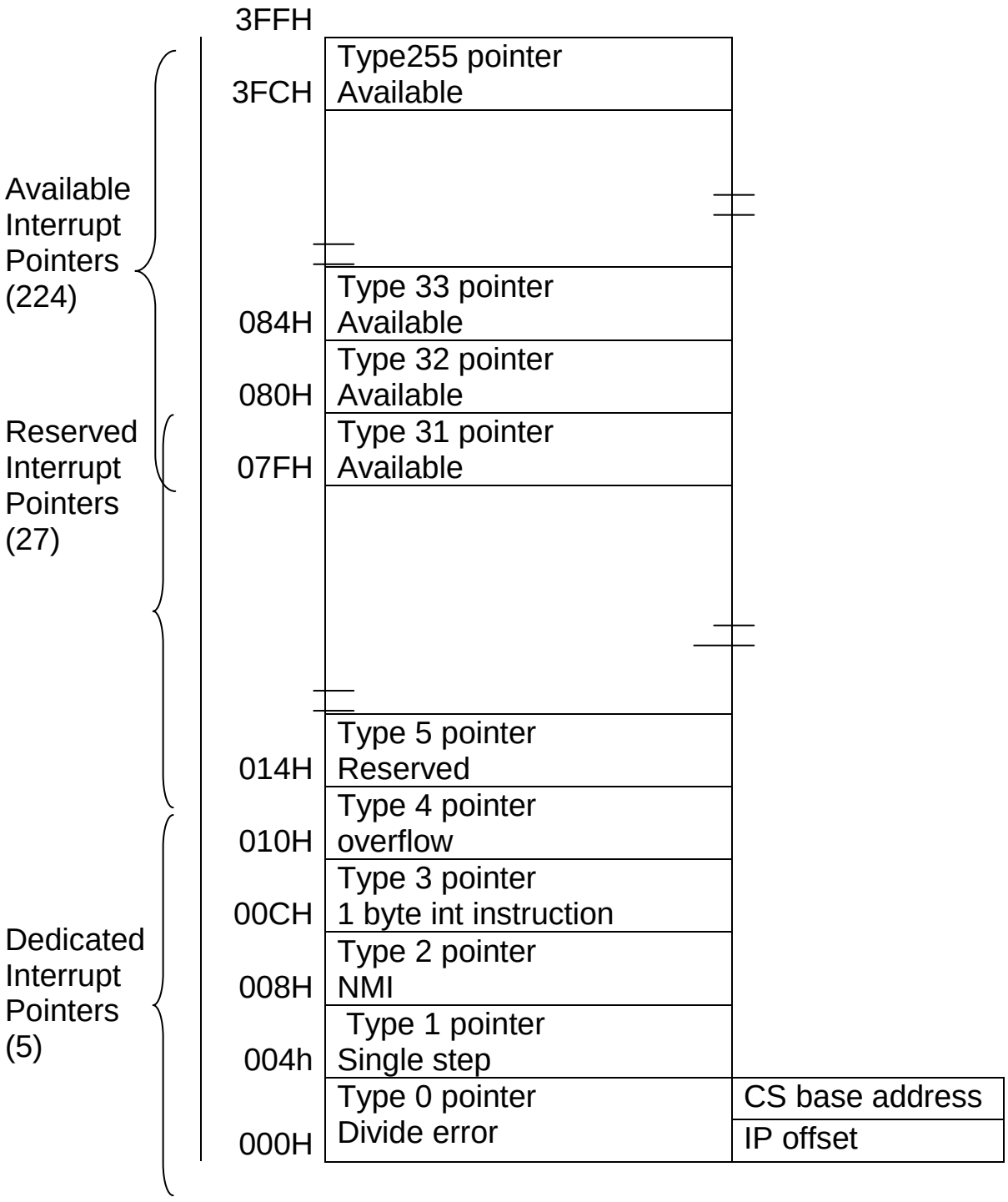
- Dynamic execution of instruction (in detail)
- multiple branch instruction(in detail)
- Dual independent bus.
- Out of turn execution

c) State the instruction latency in RISC processor designing.
Ans: (instruction latency: 4 marks for explanation)

A poorly designed instruction set can cause a pipelined processor to stall frequently

1) Highly encoded instructions, such as those used in CISC machine need complex decoders, they should be avoided.
2) Variable length instructions require multiple references to memory to fetch the entire instruction should not be considered for inclusion.
3) Instruction which access main memory, instead of register are slow in execution since main memory is comparatively slow.
4) Complex instruction which require multiple clock for their execution.

d) Draw the interrupt vector table of X86 and labeled each field in it.
Ans : (diagram with neat labels : 4 marks)

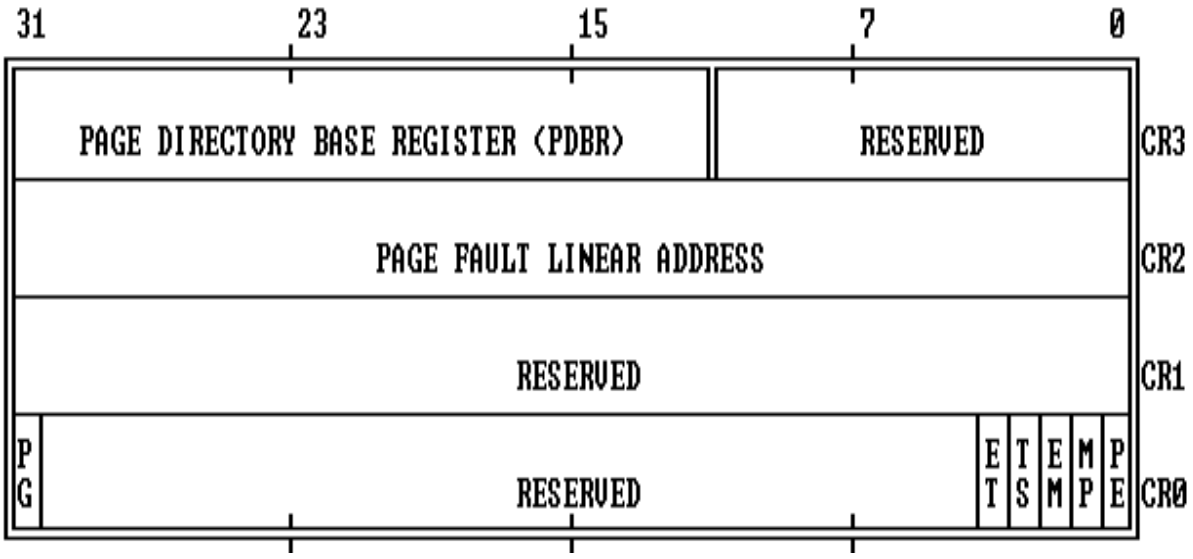


Interrupt Vector Table

e) How many control registers are present in 80386. State the function of each.
Ans:= (list of 4 control registers : 1 mark: function of CRO, CR2 and CR3 : 1 mark each=3 marks, diagram optional)

Control Registers: shows the format of the 80386 control registers CR0, CR2, and CR3. These registers are accessible to systems programmers only via variants of
CR0 contains system control flags, which control or indicate conditions that apply to the system as a whole, not to an individual task.

EM (Emulation, bit 2)
EM indicates whether coprocessor functions are to be emulated.
ET (Extension Type, bit 4)
ET indicates the type of coprocessor present in the system.
MP (Math Present, bit 1)
MP controls the function of the WAIT instruction, which is used to coordinate a coprocessor.
PE (Protection Enable, bit 0)
Setting PE causes the processor to begin executing in protected mode. Resetting PE returns to real-address mode.
PG (Paging, bit 31)
PG indicates whether the processor uses page tables to translate linear addresses into physical addresses.
TS (Task Switched, bit 3)
The processor sets TS with every task switch and tests TS when interpreting coprocessor instructions.
CR2 is used for handling page faults when PG is set. The processor stores in CR2 the linear address that triggers the fault.
CR3 is used when PG is set. CR3 enables the processor to locate the page table directory for the current task.



Q.4.

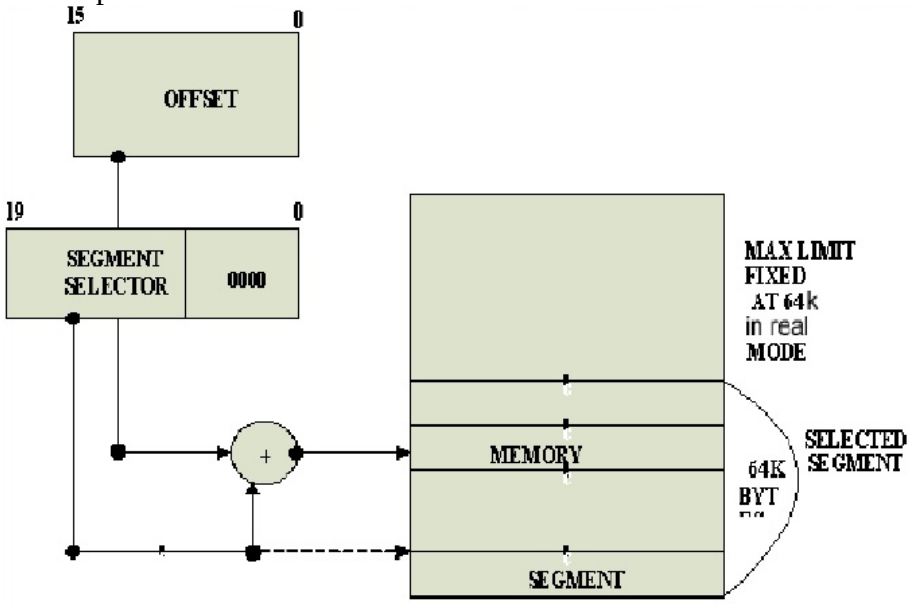
a) Attempt any Three of the following: **12**

i. Describe the real addressing mode of 80386 with neat diagram.
Ans: (diagram 2 marks , description 2 marks)

Real Address Mode of 80386

- After reset, the 80386 starts from memory location FFFFFFF0H under the real address mode. In the real mode, 80386 works as a fast 8086 with 32-bit registers and data types.
- In real mode, the default operand size is 16 bit but 32- bit operands and addressing modes may be used with the help of override prefixes.

- The segment size in real mode is 64k, hence the 32-bit effective addressing must be less has 0000FFFFFH. The real mode initializes the 80386 and prepares it for protected mode.



Physical Address Formation In Real Mode Of 80386

Memory Addressing in Real Mode: In the real mode, the 80386 can address at the most 1Mbytes of physical memory using address lines A0-A19.

- Paging unit is disabled in real addressing mode, and hence the real addresses are the same as the physical addresses.
- To form a physical memory address, appropriate segment registers contents (16-bits) are shifted left by four positions and then added to the 16-bit offset address formed using one of the addressing modes, in the same way as in the 80386 real address mode.
- The segment in 80386 real mode can be read, write or executed, i.e. no protection is available.
- Any fetch or access past the end of the segment limit generates exception 13 in real address mode. •The segments in 80386 real modes may be overlapped or non-overlapped.
- The interrupt vector table of 80386 has been allocated 1Kbyte space starting from 00000H to 003FFH

ii. Write any four features of Pentium.
Ans : (Any 4 features : 4 marks, 1 mark each)

Following are the features of Pentium:

1) It is based on net burst micro architecture.
2) Superscalar architecture
3) Dynamic branch prediction
4) Pipelined Floating-Point Unit
5) Separate code and data caches
6) 64-bit data bus
7) Address parity
8) Support for Intel MMX technology

9) Dual power supplies—separate VCC2 (core) and VCC3 (I/O) voltage inputs • Separate 16-Kbyte, 4-way set-associative code and data caches, each with improved fully associative TLBs
10) Pool of four write buffers used by both execution pipelines
11) Enhanced branch prediction algorithm
12) New Fetch pipeline stage between Prefetch and Instruction Decode

iii. Write any four features of RISC processor.

Ans: (Any 4 features : 4 marks, 1 mark each)

Features of RISC

- Simple instruction set :in a RISC machine the instruction set is simple.
- Same length Instruction: each instruction is same length so that it may be fetched in single operation.
- Single machine cycle instructions: most instruction complete in one machine cycle so processor handle several instruction at same time.
- Pipelining: massive pipeline is embedded in risc processor. pipelining is key to speed up RISC machine.
- Very few addressing modes and formats: addressing modes are less and having few formats.
- Large no of registers: large number of register to prevent large amount of interaction with memory.
- Micro coding not required.
- Load and store architecture.

iv. State the functions of following interrupts.

Ans: (1 mark for one function of interrupt service)

1) INT25H
2) INT10H
3) INT16H
4) INT21H

Ans: (1 mark for one function of interrupt service)

1) **INT 25H : Absolute Disk Read:** Reads from one or more logical sectors on the specified drive and copies the data to the specified buffer.

   Eg. Function 3Fh- Read from a File or Device.

2) **INT** 10H:**Video Reference:** To use one of these functions, first place the function number in AH, then set the other input registers, then call the function with INT 10h. Registers not used by the function as inputs or outputs are not affected.
   Eg. Function 06H : Scroll up the screen.

3) **INT 16H: Keyboard Services:** This is the application-level interface to the keyboard. Keystrokes are processed asynchronously (in the background).
   Function 02h : read the keyboard flag

4) **INT 21H:** DOS provides INT 21h, is called the DOS function dispatcher and supports functions such as: read from the keyboard, write to the screen, write to the printer, read and write to disk files, etc. INT 21h must be told which function is being requested.
Eg. Function 01h – used to read the character from standard input device.

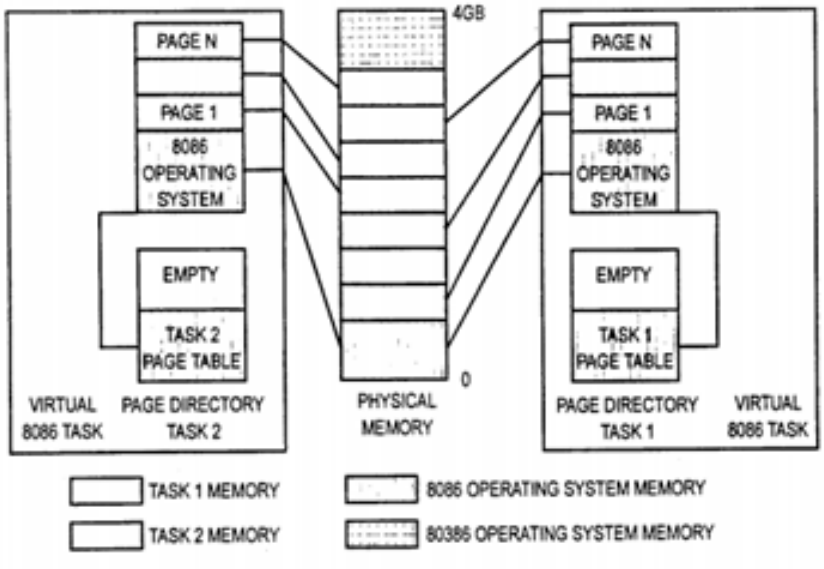
b) Attempt any One of the following: 6

i. Describe the virtual 8086 mode in 386 with sketch of memory mapping.
Ans: (diagram :3 marks, explanation : 3 marks)

Virtual 8086 Mode

- In its protected mode of operation, 80386DX provides a virtual 8086 operating environment to execute the 8086 programs.
- The real mode can also used to execute the 8086 programs along with the capabilities of 80386, like protection and a few additional instructions.
- Once the 80386 enters the protected mode from the real mode, it cannot return back to the real mode without a reset operation.
- Thus, the virtual 8086 mode of operation of 80386, offers an advantage of executing 8086 programs while in protected mode. The address forming mechanism in virtual 8086 mode is exactly identical with that of 8086 real mode.
- In virtual mode, 8086 can address 1Mbytes of physical memory that may be anywhere in the 4Gbytes address space of the protected mode of 80386. Like 80386 real mode, the addresses in virtual 8086 mode lie within 1Mbytes of memory. In virtual mode, the paging mechanism and protection capabilities are available at the service of the programmers.
- The 80386 supports multiprogramming, hence more than one programmer may be use the CPU at a time.
- Paging unit may not be necessarily enable in virtual mode, but may be needed to run the 8086 programs which require more than 1Mbyts of memory for memory management function.
- In virtual mode, the paging unit allows only 256 pages, each of 4Kbytes size. • Each of the pages may be located anywhere in the maximum 4Gbytes physical memory. The virtual mode allows the multiprogramming of 8086 applications. • The virtual 8086 mode executes all the programs at privilege level 3.Any of the other programmers may deny access to the virtual mode programs or data.
- However, the real mode programs are executed at the highest privilege level, i.e. level 0. • The virtual mode may be entered using an IRET instruction at CPL=0 or a task switch at any CPL, executing any task whose TSS is having a flag image with VM flag set to 1. • The IRET instruction may be used to set the VM flag and consequently enter the virtual mode.
- The PUSHF and POPF instructions are unable to read or set the VM bit, as they do not access it.
- Even in the virtual mode, all the interrupts and exceptions are handled by the protected mode interrupt handler.
- To return to the protected mode from the virtual mode, any interrupt or execution may be used.

- As a part of interrupt service routine, the VM bit may be reset to zero to pull back the 80386 into protected mode.

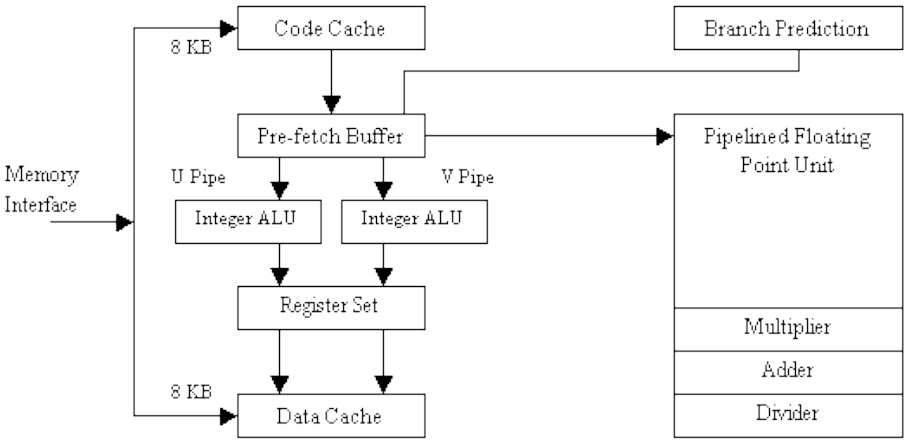


ii. Describe the Pentium CPU architecture with neat sketch.
Ans: (diagram: 3 marks, explanation: 3 marks)

Pentium Architecture

The Pentium family of processors originated from the 80486 microprocessor. The term "Pentium processor" refers to a family of microprocessors that share a common architecture and instruction set. The first Pentium processors were introduced in 1993. It runs at a clock frequency of either 60 or 66 MHz and has 3.1 million transistors. Some of the features of Pentium architecture are

- Complex Instruction Set Computer (CISC) architecture with Reduced Instruction Set Computer (RISC) performance.
- 64-Bit Bus
- Upward code compatibility.
- Pentium processor uses Superscalar architecture and hence can issue multiple instructions per cycle.
- Multiple Instruction Issue (MII) capability.
- Pentium processor executes instructions in five stages. This staging, or pipelining, allows the processor to overlap multiple instructions so that it takes less time to execute two instructions in a row.
- The Pentium processor fetches the branch target instruction before it executes the branch instruction.
- The Pentium processor has two separate 8-kilobyte (KB) caches on chip, one for instructions and one for data. It allows the Pentium processor to fetch data and instructions from the cache simultaneously.
- When data is modified, only the data in the cache is changed. Memory data is changed only when the Pentium processor replaces the modified data in the cache with a different set of data.
- The Pentium processor has been optimized to run critical instructions in fewer clock cycles than the 80486 processor.



OR

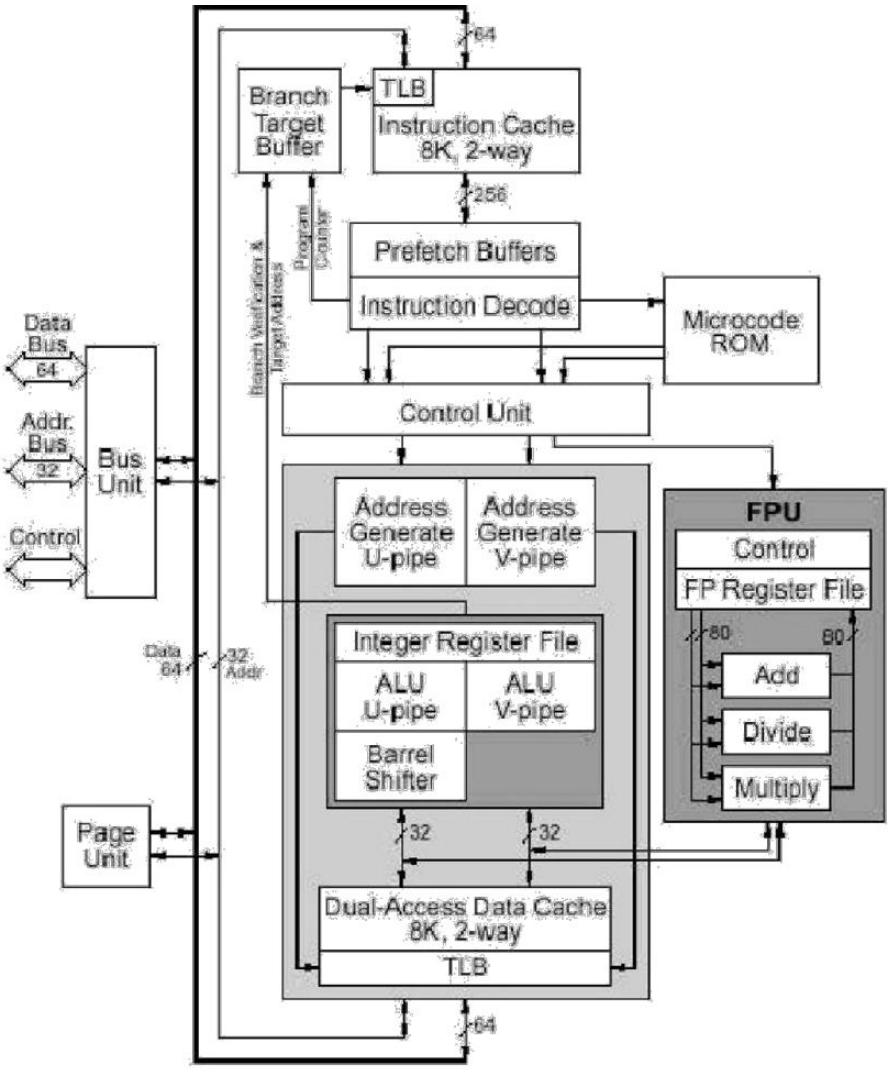


Figure 1. Pentium block diagram.

The Pentium processor has two primary operating modes

1. **Protected Mode** - In this mode all instructions and architectural features are available, providing the highest performance and capability. This is the recommended mode that all new applications and operating systems should target.
2. **Real-Address Mode** - This mode provides the programming environment of the Intel 8086 processor, with a few extensions. Reset initialization places the processor in real mode where, with a single instruction, it can switch to protected mode

The Pentium's basic integer pipeline is five stages long, with the stages broken down as follows:

1. **Pre-fetch/Fetch:** Instructions are fetched from the instruction cache and aligned in pre-fetch buffers for decoding.
2. **Decode1:** Instructions are decoded into the Pentium's internal instruction format. Branch prediction also takes place at this stage.
3. **Decode2:** Same as above, and microcode ROM kicks in here, if necessary. Also, address computations take place at this stage.
4. **Execute:** The integer hardware executes the instruction.
5. **Write-back:** The results of the computation are written back to the register file.

Floating Point Unit

There are 8 general-purpose 80-bit Floating point registers. Floating point unit has 8 stages of pipelining. First five are similar to integer unit. Since the possibility of error is more in Floating Point unit (FPU) than in integer unit, additional error checking stage is there in FPU.

Q.5. Attempt any four of the following: 16

a) List the system address register 80386 and state their one function each.

ANS: (Listing and description of all system address registers =4 marks)
Systems Address Registers:

There are total 4 system address registers:

Four registers of the 80386 locate the data structures that control segmented memory management which are:

1. GDTR (Global Descriptor Table Register) : The Global Descriptor Table Register (GDTR) is a dedicated 48-bit (6 byte) register used to record the base and size of a system's global descriptor table (GDT).
2. LDTR (Local Descriptor Table Register):
   These registers point to the segment descriptor tables GDT and LDT.
3. IDTR (Interrupt Descriptor Table Register):
   This register points to a table of entry points for interrupt handlers (the IDT).
4. TR (Task Register):
   This register points to the information needed by the processor to define the current task.

b) State the functions of INT 17H. Give any two examples.

ANS: (2 functions of INT 17H =4marks, 2 marks each function)

INT 17H is used for printer services.

1. **AH=02: Return Printer Status**
   This function call checks the printer status and returns it in the `ah` register. The values returned are:
   AH: Bit Meaning
   7 1=Printer busy, 0=printer not busy

6 1=Acknowledge from printer
5 1=Out of paper signal
4 1=Printer selected
3 1=I/O error
2 Not used
1 Not used
0 Time out error

Acknowledge from printer is, essentially, a redundant signal (since printer busy/not busy gives you the same information). As long as the printer is busy, it will not accept additional data. Therefore, calling the print character function (ah=0) will result in a delay.

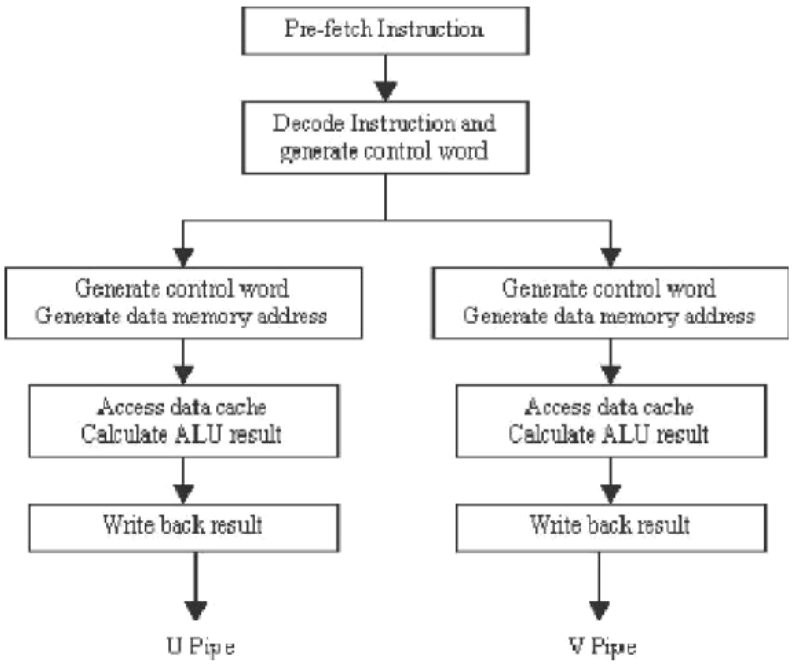
2. AH=0: Print a Character

If `ah` is zero when you call `int 17h`, then the BIOS will print the character in the `al` register. Exactly how the character code in the `al` register is treated is entirely up to the printer device you're using. Most printers, however, respect the printable ASCII character set and a few control characters as well. Many printers will also print all the symbols in the IBM/ASCII character set (including European, line drawing, and other special symbols). Most printers treat control characters (especially ESC sequences) in completely different manners. Therefore, if you intend to print something other than standard ASCII characters, be forewarned that your software may not work on printers other than the brand you're developing your software on.

c) Draw the superscalar organization of Pentium processor and state the function of each stage.

ANS: (diagram = 2 marks, functions of stages =2 marks)

Superscalar Architecture:



First stage of the pipe-line is Prefetch (PF) stage in which instructions are prefetched from the on chip instruction cache or memory. Because the Pentium processor has separate caches for instructions and data, prefetches no longer conflict with data references for access to the cache. If the requested line is not in the code cache, a memory reference is made. In the PF stage, two independent pairs of line-size (32-byte) prefetch

buffers operate in conjunction with the branch target buffer. This allows one prefetch buffer to prefetch instructions sequentially, while the other prefetches according to the branch target buffer predictions. The prefetch buffers alternate their prefetch paths.

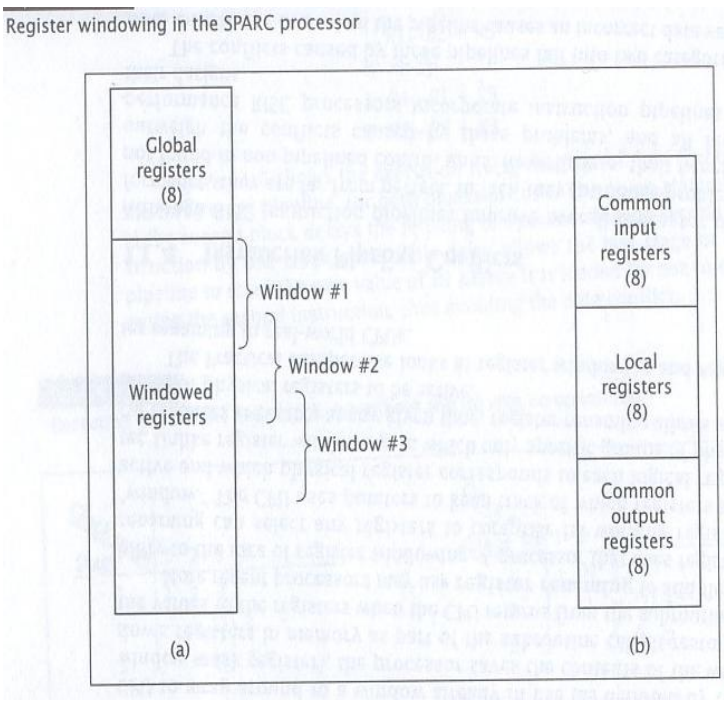
The second pipe-line stage is Decode1 (D1) in which two parallel decoders attempt to decode and issue the next two sequential instructions. The decoders determine whether on e or two instructions can be issued contingent upon the instruction pairing rules described in the section titled "Instruction Pairing Rules." The Pentium processor will decode near conditional jumps (long displacement) in the second opcode map (0Fh prefix) in a single clock in either pipe-line.

The D1 stage is followed by third stage i.e. Decode 2 (D2) in which the address of memory resident operands are calculated.

The fourth stage **Execute (EX) stage** of the pipe line for both ALU operations and for data cache access; therefore those instructions specifying both an ALU operation and a data cache access will require more than one clock in this stage. In EX all u-pipe instructions and all v-pipe instructions except conditional branches are verified for correct branch prediction. Microcode is designed to utilize both pipe-lines and thus those instructions requiring microcode execute.

The final and fifth stage is **Writeback (WB)** where instructions are enabled to modify processor state and complete execution. In this stage v-pipe conditional branches are verified for correct branch prediction. All the registers and memory locations are updated in this stage.

d) What do you meant by register windowing in RISC processor?
ANS: (Diagram of register windowing =1 mark, Description =2marks)



1. The reduced hardware requirements of RISC processors leave additional space available on the chip for the system designer. RISC CPUs generally use this space to include a large number of registers (> 100 occasionally).
2. The CPU can access data in registers more quickly than data in memory so having more registers makes more data available faster. Having more registers also helps reduce the number of memory references especially when calling and returning from subroutines.

3. The RISC processor may not be able to access all the registers it has at any given time provided that it has many of it.
4. Most RISC CPUs have some global registers which are always accessible. The remaining registers are windowed so that only subsets of the registers are accessible at any specific time.
5. To understand how register windows work, we consider the windowing scheme used by the Sun SPARC processor.
6. The processor can access any of the 32 different registers at a given time. (The instruction formats for SPARC always use 5 bits to select a source/destination register which can take any 32 different values.
7. Of these 32 registers, 8 are global registers that are always accessible. The remaining 24 registers are contained in the register window.
8. The register window overlaps. The overlap consists of 8 registers in SPARC CPU. Notice that the organizations of the windows are supposed to be circular and not linear; meaning that the last window overlaps with the first window.
9. Example: the last 8 registers of window 1 are *also* the first 8 registers of window 2. Similarly, the last 8 registers of window 2 are also the first 8 registers of window 3. The middle 8 registers of window 2 are local; they are not shared with any other window.
10. The RISC CPU must keep track of which window is active and which windows contain valid data. A window pointer register contains the value of the window that is currently active. A window mask register contains 1 bit per window and denotes which windows contains valid data.
11. Register windows provide their greatest benefit when the CPU calls a subroutine. During the calling process, the register window is moved down 1 window position. In the SPARC CPU, if window 1 is active and the CPU calls a subroutine, the processor activates window 2 by updating the window pointer and window mask registers. The CPU can pass parameters to the subroutine via the registers that overlap both windows instead of memory. This saves a lot of time when accessing data. The CPU can use the same registers to return results to the calling routine.

e) State the features of Pentium III processor.

ANS: (Any eight features of Pentium III processor . Half mark each. 0.5*8=4 marks)
The features of Pentium III processor are :

1. Pentium III processor has 512KB full speed on chip L2 Cache with ECC(ERROR CORRECTING CODE) for high performance workstations/servers. Can work on WINDOWS 98, WINDOWS NT, 2000,LINUX OS.
2. PIII is incorporated with MMX technology.
3. Dynamic execution, micro-architecture incorporates unique combination of multiple branch prediction, data flow analysis and speculative execution.
4. It Supports power management capabilities like System management mode and
5. The Pentium III processor has Multiple low power states.
6. Pentium III is optimized for 32 bits applications running on advanced 32 bits OS.
7. It has 32KB L1 cache divided as 16KB instruction cache and 16KB data cache.
8. It has Quad quad word wide ie. 256 bits cache data bus , ways set associative cache
9. It provides improved cache hit rate.
10. It supports Multiprocessor system.
11. It Works on 1.0 GHz, 850, 800, 750, 700, 650 MHZ.

(Note: any other significant features to be given marks)

f) What do you meant by Dynamic execution of instruction in Pentium processor?
ANS: (Dynamic execution of instruction description =4 marks)
Dynamic Execution Technology: ⇒ Dynamic execution incorporates the concepts of out-of-order and speculative execution.
The Pentium processor's implementation of these concepts removes the constraint of linear instruction sequencing between the traditional fetch and execute phases of instruction execution.
Up to 3 instructions can be decoded per clock cycle.
These decoded instructions are put into a buffer, which can hold up to 40 instructions.
Instructions are executed from this buffer when their operands are available (versus instruction order).
Up to 4 instructions can be executed per clock cycle.

Q.6. Attempt any four of the following: 16

a) What do you meant by paging? State the two advantages of paging.
ANS: (Paging =2 marks, advantages=2 marks =>1 mark per advantage)

Paging is one of the memory management techniques used for virtual memory multitasking operating system. The segmentation scheme may divide the physical memory into a variable size segments but the paging divides the memory into a fixed size pages. The segments are supposed to be the logical segments of the program, but the pages do not have any logical relation with the program. The pages are just fixed size portions of the program module or data.
The advantages of paging scheme are as given below:

1. The complete segment of a task need not be in the physical memory at any time. Only a few pages of the segments, which are required currently for the execution need to be available in the physical memory. Thus the memory requirement of the task is substantially reduced, relinquishing the available memory for other tasks. Whenever the other pages of task are required for execution, they may be fetched from the secondary storage.
2. There is no need to keep the pages in the memory which have been executed, and hence the space occupied by them may be relinquished for other tasks. Thus paging mechanism provides an effective technique to manage the physical memory for multitasking systems.

b) Draw and describe the segment descriptor cache register of 80386.
ANS: (Diagram of segment descriptor cache register of 80386=2 marks and description =2 marks)

Segment descriptor cache registers:

- These registers are not available for the users.
- These registers are associated with the segments and the segment registers in 80386 i.e. CS,DS,ES,SS,FS,GS
- Every segment descriptor cache register is 72 bits long.
- Every segment descriptor cache register holds
  a. 32 bits segment base address
  b. 32 bits segment limit
  c. Other required segment attributes.

Segment registers ←16 BITS→		Descriptors registers (loaded automatically)		
		Physical base address and segment limit (64 bits)		Segment attributes (9 bits)
Selector	CS			
Selector	SS			
Selector	DS			
Selector	ES			
Selector	FS			
Selector	GS			
Visible to users		←32 bits base address→	←-----32 bits limit addr.→	Invisible to users

- When a selector is loaded, its associated segment descriptor cache register is automatically get loaded with the values from descriptor table. Either from LDT or GDT.
- In the real mode, only the base address is updated directly by shifting the selector values 4 bits to the left.
- In the protected mode, the base address, limit and all attributes are loaded.

c) Write the advantages of separate code and data cache available in Pentium.
ANS: (4 advantages of separate code and data cache=4 marks, 1 mark each)

Advantages of separate instruction and data caches :

1. Separate code and data cache memories effectively and efficiently execute the branch prediction.
2. Simultaneous cache look up is achieved by Pentium processor due to the separate data and code cache.
3. The separate cache memories raise the system performance i.e. an internal read request is performed more quickly than a bus cycle to memory.
4. They reduce the use of processor's external bus when the same locations are accessed multiple times.

d) State any four features of SUN ultra SPARC.
ANS: (Any 4 features of SUN ultra SPARC, 4 points*1 mark each = 4 marks)
Features of SUN ULTRA SPARC (Scalable Processor Architecture) are:
The 64 bits Ultra SPARC architecture has following features:

1. It has 14 stages non-stalling pipeline.
2. It has 6 execution units including two for integer, two for floating point, one for load/store and one for address generation units.
3. It has a large number of buffers but only one load/store unit, it dispatches them one instruction at a time from the instruction stream.
4. It contains 32KB L1 instruction cache, 64KB L1 data cache, 2KB prefetch cache and 2 KB write cache. It also has 1MB on chip L2 cache.
5. Like Pentium MMX it also contains the instructions to support multimedia. These instructions are helpful for the implementation of image processing codes.
6. One of the major limitations of SPARC system is its low speed compared to most of the modern processors.

e) State any four differences between .com and exe program.

ANS: (Any 4 differences between .com and .exe programs. 4 points*1 marks each = 4 marks)

Sr.No	.COM programs	.EXE Programs
1.	.COM file does not contain any header	.EXE file contains header
2.	.COM file cannot contain relocation items.	.EXE file may contain relocation items.
3.	Maximum size is 64k minus 256 bytes. For PSP and 2 bytes for stack.	No limit on size; Can be of any size
4.	Entry point is PSP:0100	Entry point is defined by END directive.
5.	Stack size is 64K minus 256 bytes for PSP and size of executable data and code.	Stack size is defined in a program with STACK directive.
6.	Size of file is exact size of program.	Size of file is size of program plus header (Multiple of 256 bytes)