SUMMER – 15 EXAMINATIONS

Model Answer

Subject Code: **17320** Page No: 1/

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.

2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.

3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).

4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.

5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.

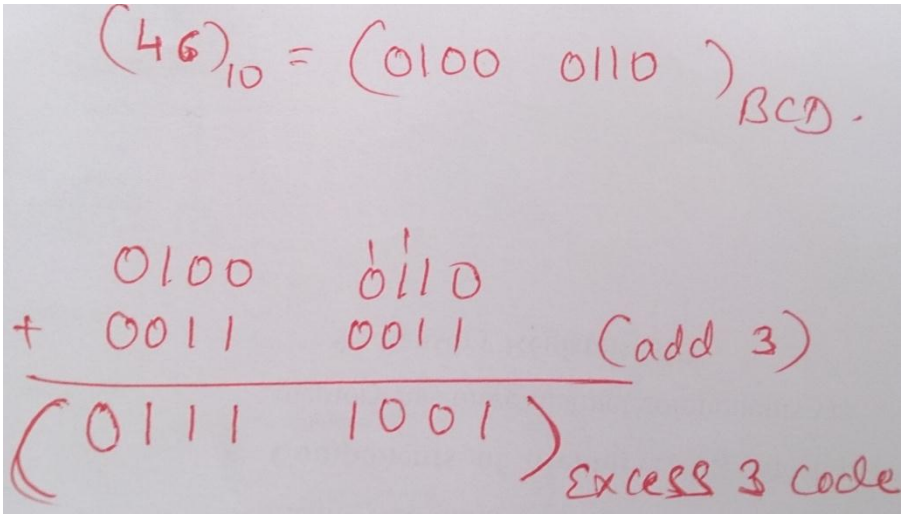
6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.

7) For programming language papers, credit may be given to any other program based on Equivalent concept.

1. **A) Attempt any six** 12

a) Convert the decimal no.46 into BCD code and in excess 3 code.

Ans:-(Conversion 2 mks each)



b) Give the two advantages of multiplexer.

Ans:-(Two advantages – 2 mks)

1. 1. It reduces the number of wires.
2. So it reduces the circuit complexity and cost.
3. We can implement many combinational circuits using MUX.
4. It simplifies the logic design.
5. It does not need the k maps and simplification.

c) State the different triggering methods in digital circuit.

Ans:-(2 methods-2 mks)

Triggering is classified into two types:

1. Level Triggered-Positive level triggering
   -Negative level triggering
2. Edge Triggered Positive Edge triggering
   -Negative Edge triggering

d) State the various types of shift registers.

Ans:-(4 types – 2mks)

1) Serial in serial out (SISO)
2) Serial in parallel out (SIPO)
3) Parallel in serial out (PIPO)
4) Parallel in parallel out (PIPO)
5) Shift right/shift left register
6) Bidirectional shift register

e) Identify the IC 0800 and IC 0809.

Ans:-(proper identification of ICs – 2 mks)

IC 0800 – 8 bit ADC IC
IC 0809- 8 bit DAC IC

f) Compare EPROM and EEPROM (any two pts)
Ans:-(2 relevant points- 2 mks)

Parameters	**EPROM**	**EEPROM**
1)Technique used for erasing	Exposure to ultraviolet light	A voltage of 20 to 25 V is applied
2)Selective erasing	Not possible. All the locations get erased.	Possible. A particular location only can be erased.

g) Write associate and commutative Boolean laws.
Ans:-(Proper laws- 2 mks)

Associative Law	Commutative Law
(A.B)C=A.(B.C)	A.B=B.A
(A+B)+C=B+(A+	A+B=B+A

h) Draw the logic symbol and truth table for two input NAND gate.
Ans:-(Symbol- 1mks, truth table-1 mks)

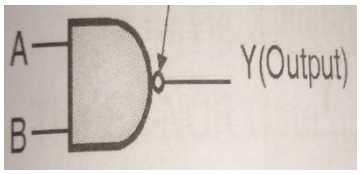


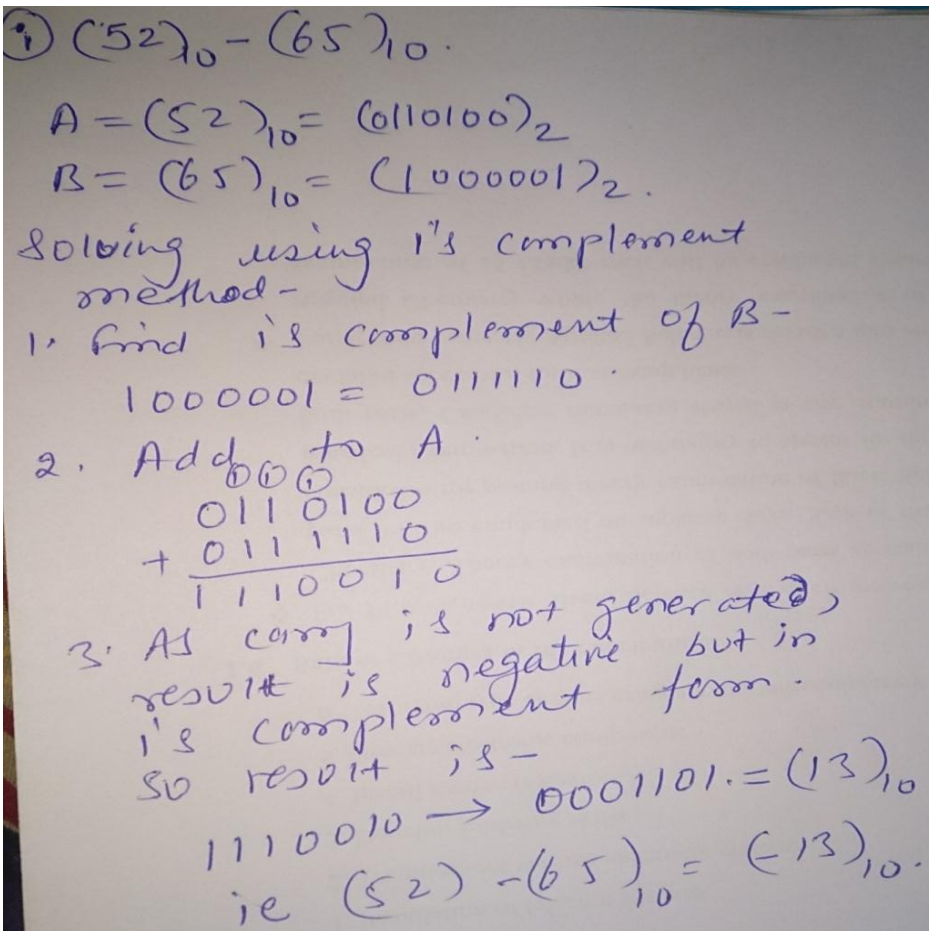
Fig: Logic Symbol

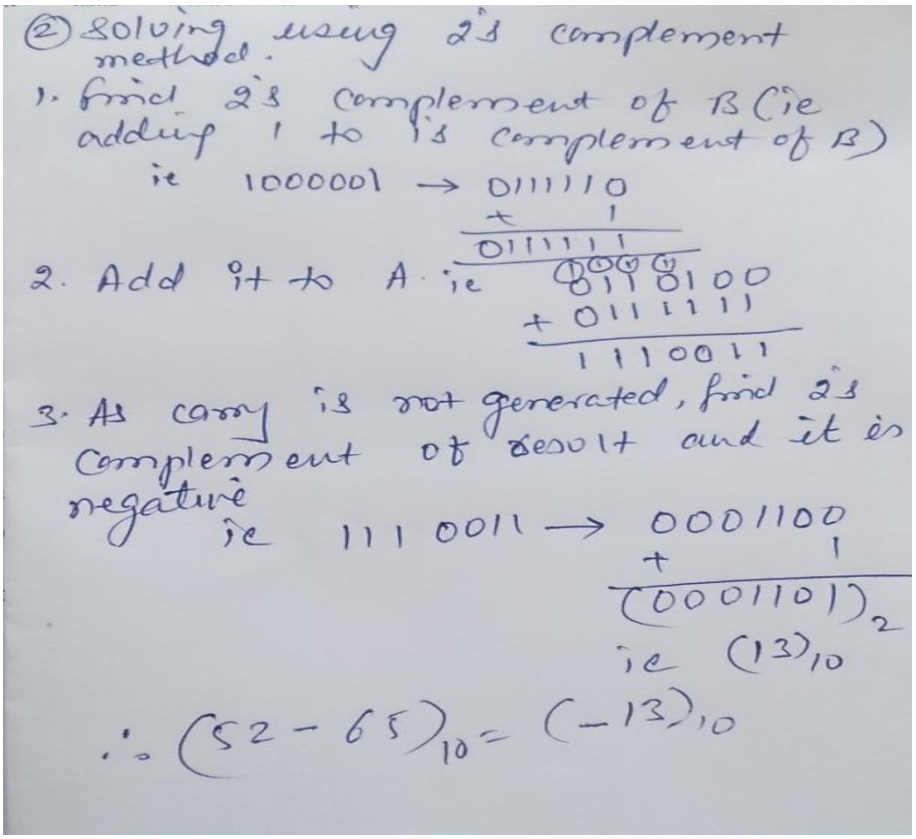
Inputs		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

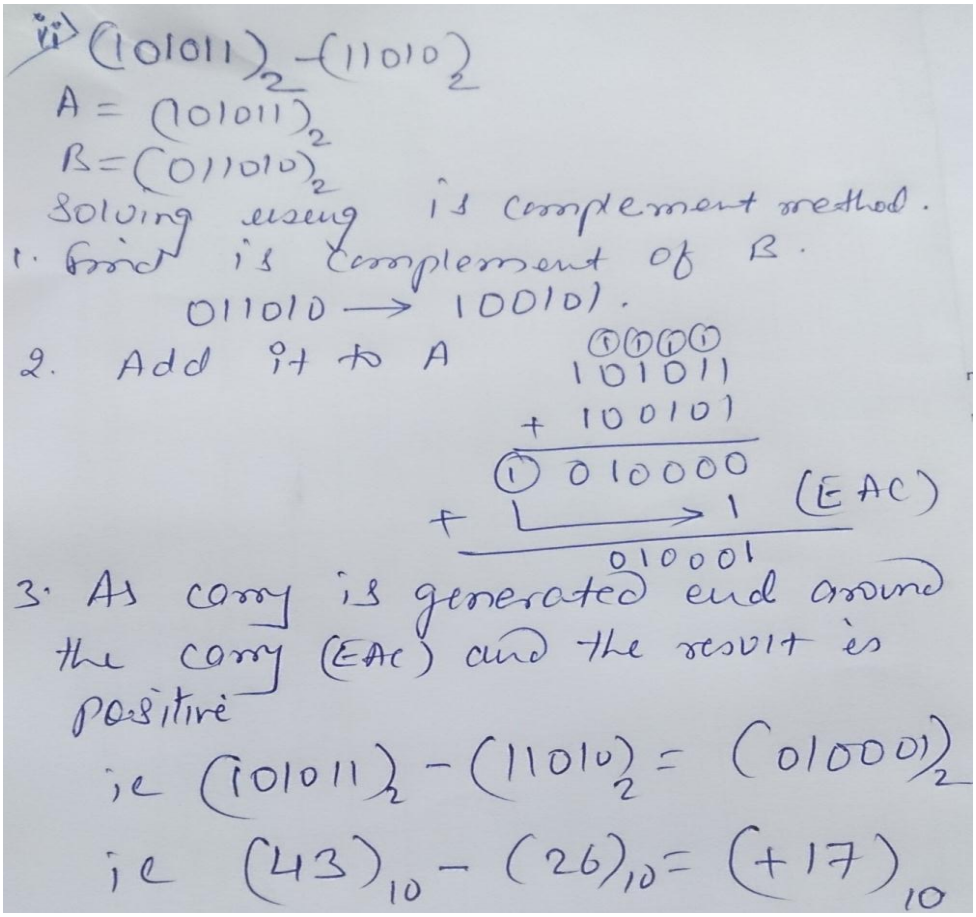
fig: Truth table

B) Attempt any two. 8

B) Solve the following subtraction using 1's and 2's complement method.
i) $(52)_{10}$- $(65)_{10}$
ii) $(101011\text{-}11010)_2$
Ans:-(Solving the two by both methods- 1 mks each)


(i) $(52)_{10} - (65)_{10}$.
$A = (52)_{10} = (0110100)_2$
$B = (65)_{10} = (1000001)_2$.
Solving using 1's complement method -
1. find 1's complement of B -
1000001 = 0111110.
2. Add to A.
0110100
+ 0111110
1110010
3. As carry is not generated, result is negative but in 1's complement form.
So result is -
1110010 → 0001101. = $(13)_{10}$
ie $(52) - (65)_{10} = (-13)_{10}$.


(ii) Solving using 2's complement method.
1. find 2's complement of B (ie adding 1 to 1's complement of B)
ie 1000001 → 0111110
+ 1
0111111
2. Add it to A. ie 0110100
+ 0111111
1110011
3. As carry is not generated, find 2's complement of result and it is negative
ie 1110011 → 0001100
+ 1
$(0001101)_2$
ie $(13)_{10}$
$\therefore (52 - 65)_{10} = (-13)_{10}$



ii) $(101011)_2 - (11010)_2$

$A = (101011)_2$

$B = (011010)_2$

Solving using 1's complement method.

1. Find 1's complement of B.

$011010 \longrightarrow 100101$.

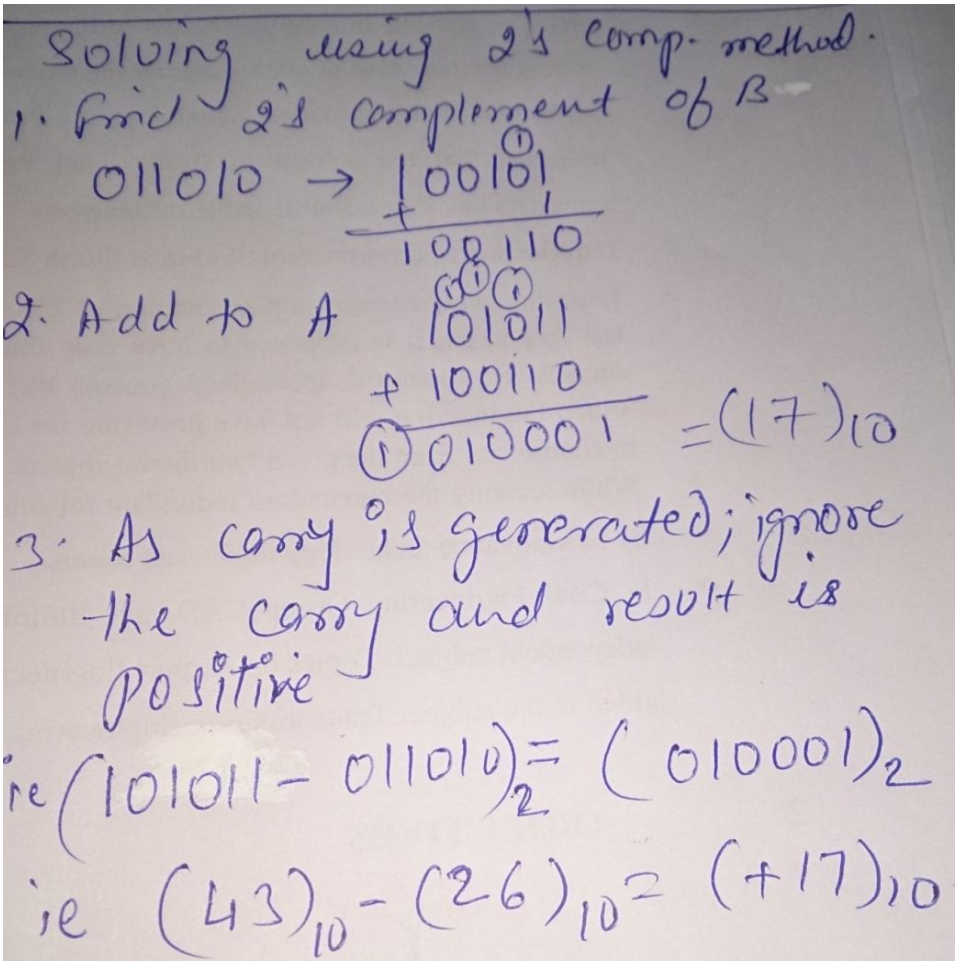
2. Add it to A

$$\begin{array}{r} \overset{1}{1}\overset{1}{0}\overset{1}{1}\overset{1}{0}\overset{1}{1} \\ 101011 \\ +\ 100101 \\ \hline (1)\ 010000 \\ +\ \longrightarrow\ 1 \quad \text{(EAC)} \\ \hline 010001 \end{array}$$

3. As carry is generated end around the carry (EAC) and the result is positive

ie $(101011)_2 - (11010)_2 = (010001)_2$

ie $(43)_{10} - (26)_{10} = (+17)_{10}$

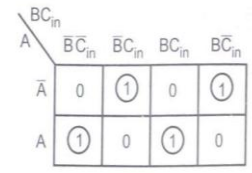


b) Explain full adder with its truth table , K map simplification and logic diagram.
Ans:-(1 mks each for truth table, kmap , 2 mks for logic diagram using gates)

Truth Table:

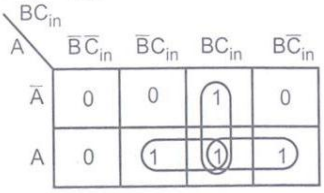
Inputs			Outputs	
A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

K-map for sum:



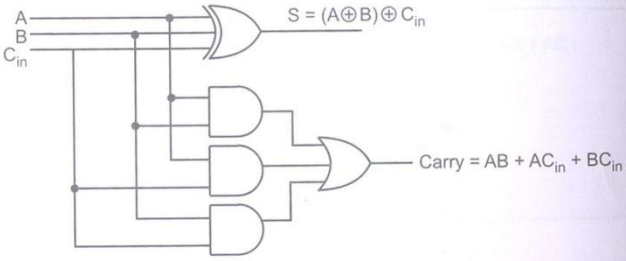
$$Sum = \bar{A}\bar{B}\,C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$

K-map for carry C_{out}



$$C_{out} = AB + AC_{in} + BC_{in}$$

Logic implementation of full adder:



c) Design a 4:1 MUX using 2:1 MUX and write truth table.
Ans:-(Proper diagram- 2 mks, truth table-2 mks)
(NOTE: Any other relevant logic diagram and truth table should be given marks)

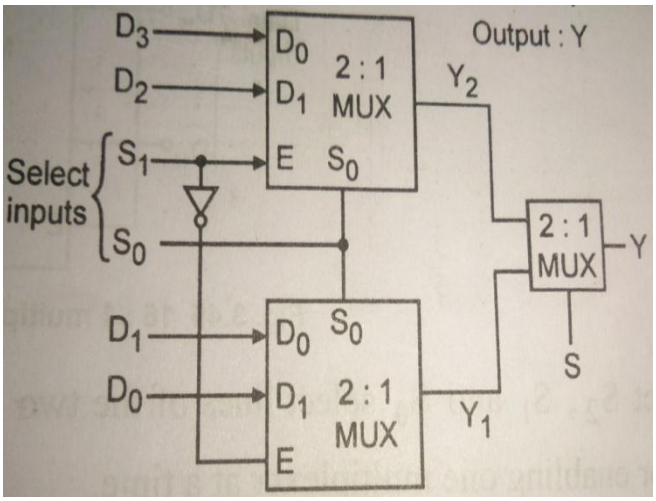
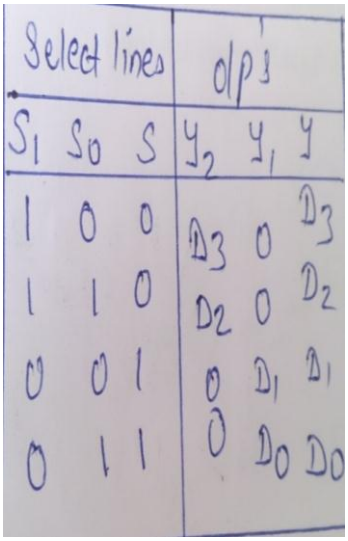


Fig: Design of 4:1 MUX using 2:1 MUX



Or

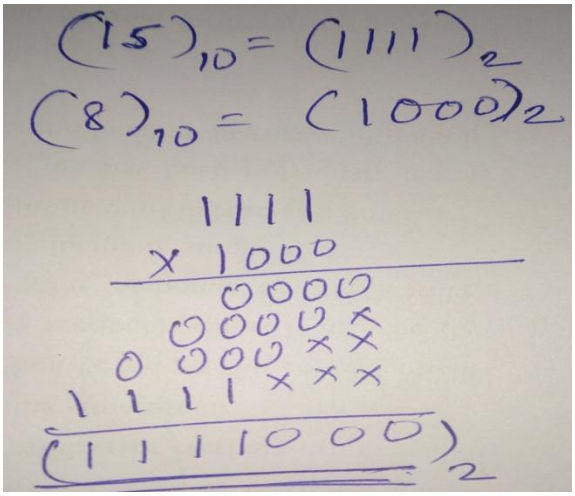
Input			Output
E (S1)	S0	S	Y
1	0	0	D3
1	1	0	D2
0	0	1	D1
0	1	1	D0

Fig: Truth table

2. Attempt any four **16**

a) Perform the following multiplication in binary number system $(15)_{10} * (8)_{10}$

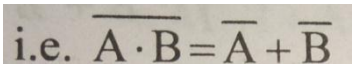
Ans:- (Equivalent binary number -1 mks each, correct answer-2 mks)



b) State and prove the both De-Morgans Theorem with logic diagram.

Ans:-(2 statements- 2mks, proof 1 mks each)

1st Theorem-It states that complement of product is equal to sum of their individual complements.



Proof :

A	B	$\overline{A}$	$\overline{B}$	$A \cdot B$	$\overline{A \cdot B}$	$\overline{A}+\overline{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

2nd Theorem-It states that complement of sum is equal to product their individual complements.

$$\text{i.e. } \overline{A+B}=\overline{A}\cdot\overline{B}$$

Proof :

A	B	A + B	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A}\cdot\overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

c) Explain the concept of minterm and maxterm with example.
Ans:-(Definition and example for both- 1mks each)
Min term- A standard SOP form is the one that includes a number of product terms. Each individual product term containing all the variables of function,is called as the minterm, denoted by m.

Example: $Y = \underbrace{\overline{A}BC}_{\text{Minterm}} + ABC + A\overline{B}\overline{C} + \overline{A}BC$

As shown , Y has four minterms and each minterm has all the three variables present.

Maxterm-A standard POS form is the one that includes a number of sum terms. Each sum terms containing all the variables in the standard POS equation is called as maxterm and denoted by M.

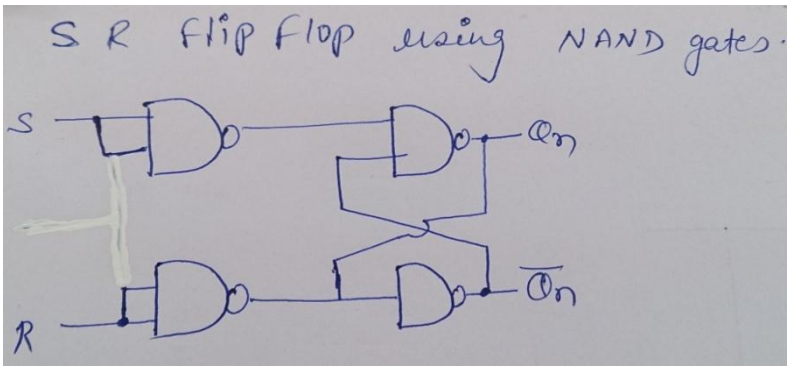
Example :

$$Y = \underbrace{(A+B+C)}_{\text{Maxterm}}\ (\overline{A}+B+C)\ (A+\overline{B}+C)$$

As shown above equation Y contains three maxterms and each term has all the three variables present.

d) Draw and explain OR flipflop using NAND gate with its truth table.
Ans:- (NOTE:-Question is printed wrongly. It should be SR flipflop. Ans is as given below)

(Diagram- 2mks, truth table-1 mks,explanation-1 mks)



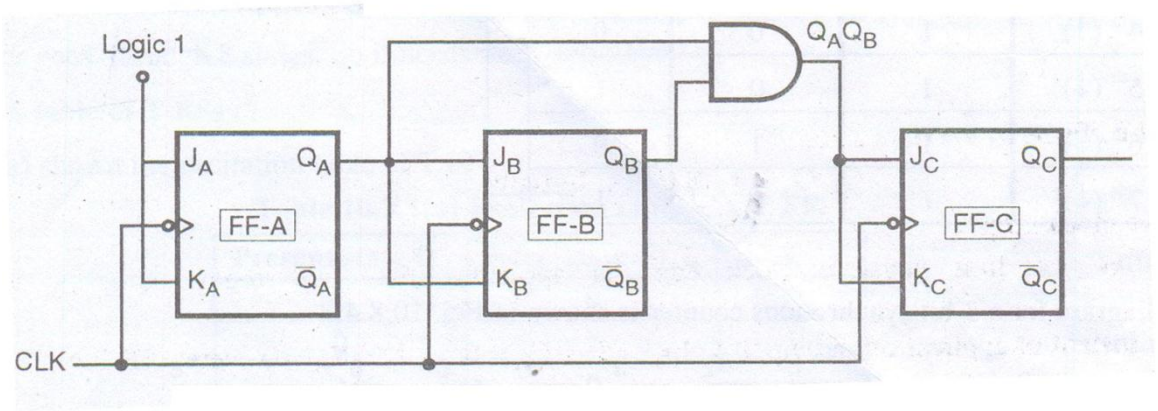
Truth table

S	R	Q_{n+1} (o/p)
0	0	Q_n (No change)
0	1	0
1	0	1
1	1	Not allowed

Explanation-

For SR flipflop for S=R=0, present o/p remains same as previous o/p ie Qn.
For s=0, R=1, o/p resets ie 0
For S=1, R=0, o/p sets ie 1
For S=R=1. o/p is not allowed or forbidden.

e) Draw the circuit diagram of 3 bit synchronous up counter with its truth table and explain its working.
Ans:-(Diagram- 2 mks, truth table-1 mks, explanation-1 mks)
Diagram-



Truth Table-

Clock	Q_C	Q_B	Q_A
0	0	0	0
1st (↓)	0	0	1
2nd (↓)	0	1	0
3rd (↓)	0	1	1
4th (↓)	1	0	0
5th (↓)	1	0	1
6th (↓)	1	1	0
7th (↓)	1	1	1

Operation: Initially all the flip flops are in reset state. i.e. QA QB QC=000

1st Clock pulse: FF-A toggles and Q_A becomes 0.But since Q_A =0 at the instant of application of 1st falling clock edge, J_B=K_B=0 and Q_B does not change state ,QA=0. Similarly Q_C also does not change state QC=0.So QC QB QA=001, after 1st clock pulse.

2nd Clock pulse:- FF-A toggles and Q_A becomes 0.But at the instant of application of 2nd falling clock edge Q_A was equal to 1.Hence, J_B=K_B=1. Hence FF-B will toggle and Q_B becomes 1. Output of AND gate is 0 at the instant of negative clock edge. So J_C= K_C =0. Hence Q_C remains 0.
So o/p QC QB QA=010 , after 2nd clock pulse

3rd clock pulse: After the 3rd clock pulse, the output are $Q_CQ_BQ_A$=011

f) Define the following specifications of DAC i) Resolution ii) Linearity iii) Accuracy iv) Setting time.
Ans:-(Each proper definition- 1 mks each)

i). Resolution-This is the smallest possible change in output voltage as a fraction or percentage of then full scale output voltage range e.g. For an 8 bit converter, there are 2^8 or 256 possible values of analog output voltage; hence then smallest change in output voltage is $1/255^{th}$ of then full scale output range. Thus, its resolution is described as one part in 255 or 0.4%.

ii). **Linearity**-Equal increment in the digital input should result in equal increments in analog output voltage.

iii) **Accuracy**- The accuracy of DAC is a measure of the differences between the actual output and the expected output voltage and specified in a percentage of full scale output voltage.

iv) **Settling time**- Time required for the analog output to settle within ±1/2 LSB of the final value after a change in the digital input referred to as settling time.

3. Attempt any four **16**

a) State the rules for BCD addition.
Ans:-(Proper rules- 4 mks)

1. Add the two BCD numbers.
2. If the sum is less or equal to 9, it is valid BCD result.
3. If the result is more than 9 or a carry is generated then add 6 (i.e. binary 0110) to the sum to make it a valid BCD result.

b) Compare CMOS and TTL logic family on following points:Propagation delay,fan out, powerdissipation , noise immunity.

Ans:-(Relevant answers- 1 mks each)

Parameters	CMOS	TTL
Propagation delay	105 nsec	10 nsec
Fan out	50	10
Power dissipation	0.1 mW	10 mW
Noise immunity	Better than TTL	Less than CMOS

c) Design 1:16 demultiplexer using 1:4 demultiplexer.
Ans:-(Proper relevant diagram with proper naming- 4 mks)

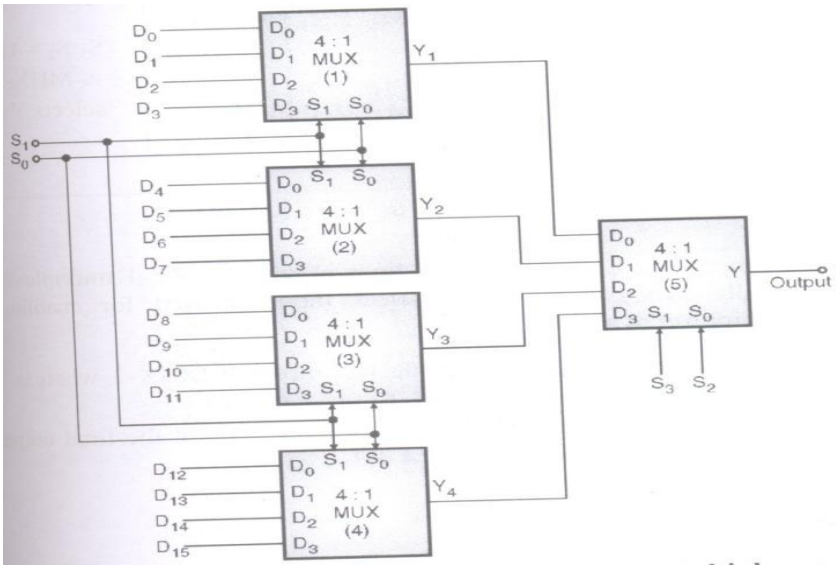


Fig: Design of 1:16 demultiplexer using 1:4 demultiplexer.

d) Compare combinational circuit with sequential circuit (any four).
Ans:-(4 relevant points- 4 mks)

Parameters	**Combinational circuit**	**Sequential circuit**
Definition	The output at any instant of time depends upon the input present at that instant of time.	The output at any instance of time depends upon the present input as well as past input and output.
Need of Memory	No memory element required in the ckt	Memory element required to stored bit
Need of clock	Clock input not necessary	Clock input necessary
Examples	E.g. Adders, Subtractors ,Code converters, comparators etc.	E.g. Flip flop, Shift registers, counters etc,
Applications	Used to simplify Boolean expressions, k-map , Truth table	Used in counters & registers

e) Draw the block diagram of dual slope ADC and explain its working with waveforms.
Ans:-(Diagram- 2 mks, explanation -1 mks, waveforms- 1mks)

The dual slope ADC consists of OPAMP,,s being used as integrator and comparator. The control logic accepts the SOC signal and generates EOC signal when the conversion is over. It also controls the two switches S1 and S2 out of which S1 is a single pole three way switch whose one terminal is connected to analog voltage VA, second one is connected to ground and the third one is connected to a negative reference voltage VREF

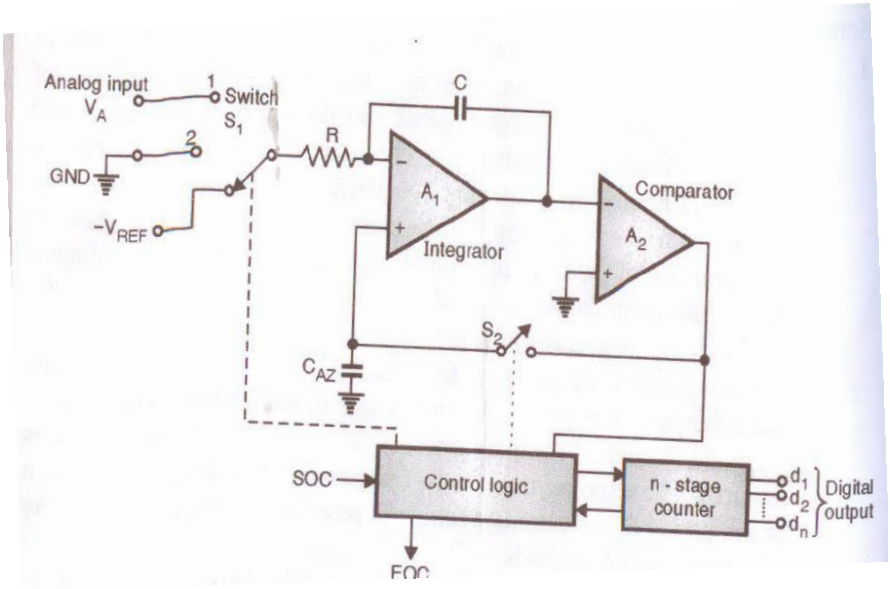
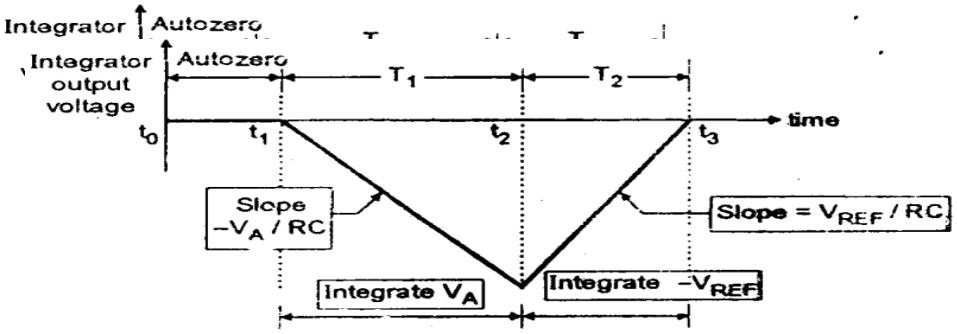


Fig: Dual Slope ADC

Operation:-

At the out Initially assume that the integrator output voltage V0= 0 and the counter is in RESET condition i.e. counter output is 00.

1. At t = t0 switch S1 is connected to ground and switch S2 is closed. The capacitor CAZ gets connected across the comparator output.
2. Any offset voltage present in the OP-AMPs will appear across the capacitor C. This will provide an automatic compensation for the input offset voltage of all the amplifiers. Therefore integrator output voltage is zero for the interval t0 to t1.
3. At instant t1 the SOC command is given to the control logic. Switch S1 is connected to VA and Switch S2 is open circuited. CAZ acts as a memory to hold the voltage required to keep the offset zero. Hence CAZ is known as the auto zero capacitor.
4. From t1 to t2, this ADC will integrate the analog input VA, for a fixed duration of clock cycles. This time interval is requited for the counter to advance through all its possible output states, because for an n-bit counter there will be 2n possible output states.
5. The counter output then reduces to zero. The time duration t1 to t2 t is represented by T1.The integrator output during this period is given by,



$$V_o = -\frac{1}{RC}\int_{t_1}^{t_2} V_A\,dt = \frac{-V_A T_1}{RC}$$

This expression represents a straight line with a slope of - VA / RC. Thus we get a decreasing ramp.

The time period T is thus represented by 2n clock cycles.

$\therefore\ T_1 = 2^n \times T$ …..Where T = one clock cycle period

6. At the end of interval T1 the integrator input is connected to a fixed negative reference voltage (-V REF) via switch S1.
7. The integrator output now starts increasing towards zero with positive slope. The slope of the line is VREF / RC for the duration t2 to t3.
8. The counter starts counting from 0. The integration will continue till the integrator output is non-zero. At instant t3 the integrator output reduces to zero then the comparator output goes from HIGH to LOW and the clock pulses given to the counter are stopped.
9. At t3. the counter output shows a number corresponding to N clock cycles it has counted during period t2 to t3.
10. Thus this number N represents the time taken for integrator output to reduce from - VA to 0. Hence N represents the desired digital output code proportional to the analog input VA.

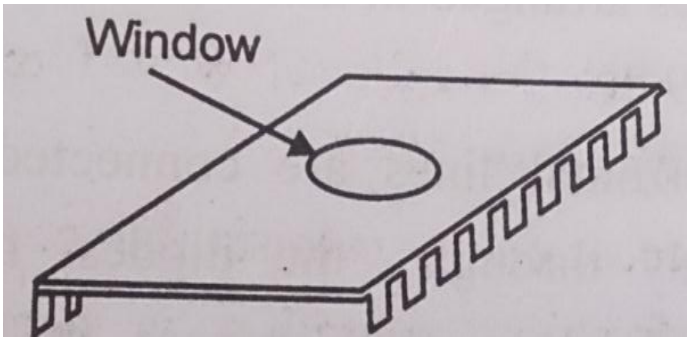
12. If VA increases, then the integrator capacitor vi1l charge to a higher negative voltage during the time interval T Therefore the time T required to reduce the integrator output to zero increases.

13. Therefore the counter output count (N) will be higher. Thus N is proportional to VA.

f) State the different types of ROMs and explain any one type of ROM.
Ans:-(2 types- 2mks, explain any 1 – 2 mks)

Types of ROMs:-
1) PROM (Programmable read only memory)
2) EPROM (Erasable Programmable read only memory)
   i) EEPROM (Electrically erasable Programmable read only memory)
   ii) UVPROM-(Ultra violet Programmable read only memory)
3) Mask programmable ROM

UV PROM- Ultra violet PROM-It can be erased by exposing the EPROM chip to ultraviolet sun rays. This EPROM has a quartz lid or window on the package as shown. we can erase the contents by exposing it to the ultraviolet rays for about 10-15 minutes, by which all the cells will be erased and all the locations will have the store as 1.



4. Attempt any four **16**

a) Design a 3:8 line decoder with truth table and logic diagram and give IC no for the same.

Ans:-(Diagram- 1 mks, truth table – 1mks, Logical diagram-1 mks, IC no-1 mks)

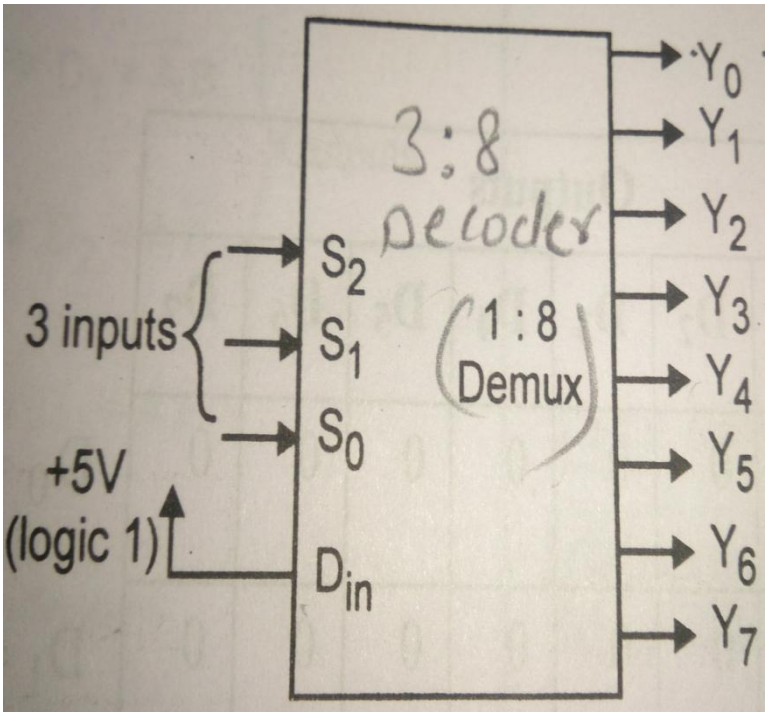


Fig: 3:8 line decoder

D_{in}	S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1

Fig: Truth Table of 3:8 line decoder

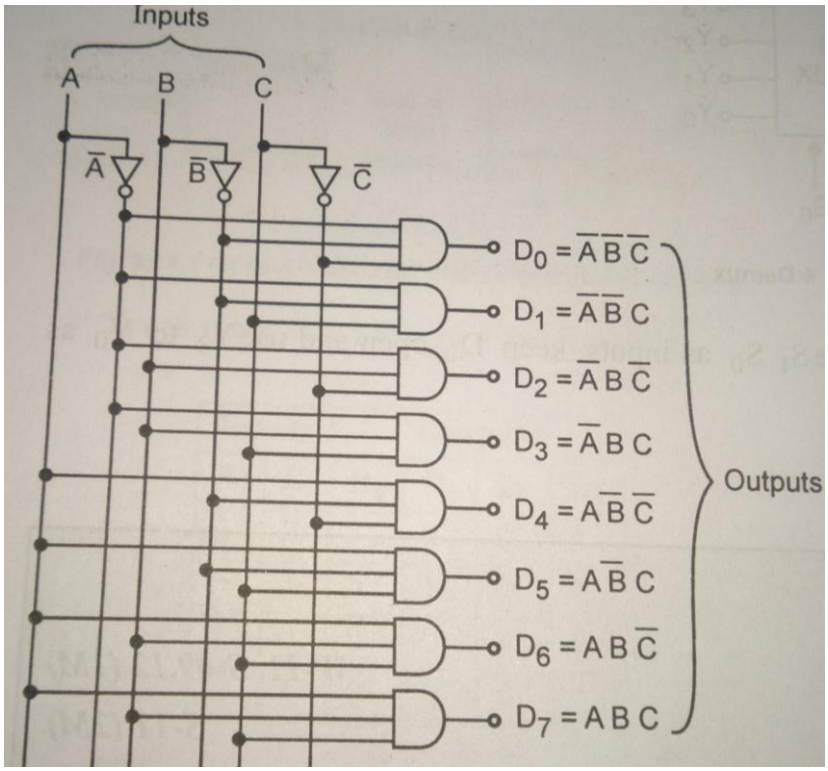


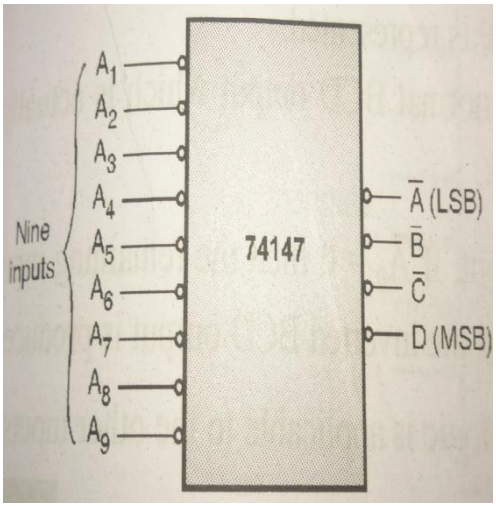
Fig: Logic Diagram of 3:8 line decoder

IC No. for 3:8 line decoder- IC 74138

b) Draw and explain decimal to BCD priority encoder using IC 74147.
Ans:-(Diagram -1 mks, truth table -2 mks, explanation – 1 mks)

Explanation-IC 74147 is basically a 10:4 encoder or decimal to BCD encoder.A1 to A9 inputs are the active low inputs and A,B, C and D are the active low outputs.A1 has the lowest priority and A9

has the highest priority. In response to the inputs, chip produces inverted BCD code corresponding to the highest numbered Active input. as shown in the truth table.



Truth Table:

Inputs									Outputs (Inverted BCD)				Normal BCD			
$\bar{A}_1$	$\bar{A}_2$	$\bar{A}_3$	$\bar{A}_4$	$\bar{A}_5$	$\bar{A}_6$	$\bar{A}_7$	$\bar{A}_8$	$\bar{A}_9$	D	C	B	A	D	C	B	A
1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
X	X	X	X	X	X	X	X	0	0	1	1	0	1	0	0	1
X	X	X	X	X	X	X	0	1	0	1	1	1	1	0	0	0
X	X	X	X	X	X	0	1	1	1	0	0	0	0	1	1	1
X	X	X	X	X	0	1	1	1	1	0	0	1	0	1	1	0
X	X	X	X	0	1	1	1	1	1	0	1	0	0	1	0	1
X	X	X	0	1	1	1	1	1	1	0	1	1	0	1	0	0
X	X	0	1	1	1	1	1	1	1	1	0	0	0	0	1	1
X	0	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0
0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1

c) What is Race around condition in JKFF? How it can be avoided?
Ans:-
(Race around condition explanation-2 mks, how to avoid it- 2methods-2mks)

Race Around Condition:-

In JK Flip-flop when J=K=1 and when clock goes high, output should toggle (change to opposite state) ,but due to multiple feedback output changes/toggles many times till the clock/enable is high. Thus toggling takes place more than once, called as race around condition.

To avoid RAC following methods can be used-
1. Design the clock with time less than toggling time (this method is not economical)
2. Use edge triggering.
3. Use Master Slave J K Flip-flop.

d) Explain the working of 4 bit ring counter with a neat diagram.

Ans:-(Diagram-2 mks, working with waveforms-1 mks, truth table- 1mks)
(Either use SR or JK flip flop or D flipflop)

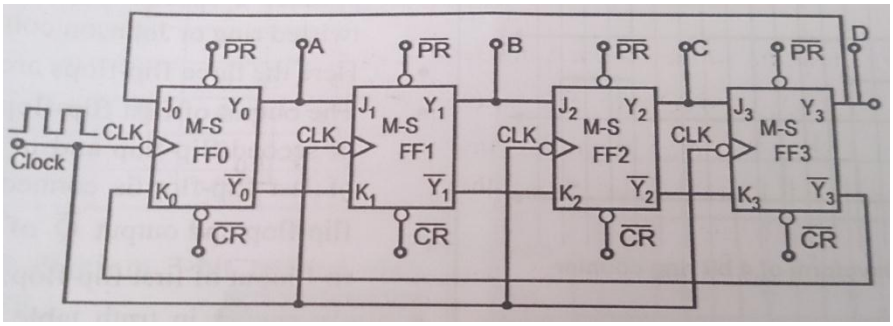


Fig: 4 bit ring counter using JK flip flop

Or

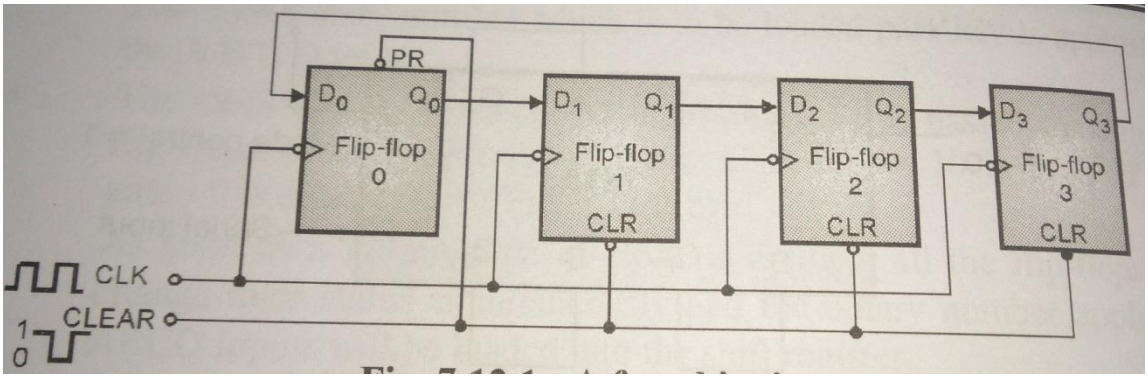


Fig: 4 bit ring counter using D flip flop

CLR	CLK	Q_0	Q_1	Q_2	Q_3
⊓	×	1	0	0	0
1	↓	0	1	0	0
1	↓	0	0	1	0
1	↓	0	0	0	1
1	↓	1	0	0	0

4 bit ring counter:-As shown the 4 bit ring counter consists of 4 D flip flops (or SR or JK) wherein the o/p of last flip flop is connected back to input of 1st flip flop. Clocks are applied simultaneously in serial output shift register manner. The working is as shown in truth table where 1 allowed to enter in 1st flip flop by activating preset terminal.
Therefore $Q_0Q_1Q_2Q_3$ =1000. Upon application of clock the data shifts from one flip flop to next in a circulating manner.
Therefore upon application of 1st Clk pulse status of $Q_0Q_1Q_2Q_3$ =0100.
2nd clk pulse status of $Q_0Q_1Q_2Q_3$ =0010;
3rd clk pulse status of $Q_0Q_1Q_2Q_3$ =0001.
And status of $Q_0Q_1Q_2Q_3$ will repeat after 4th clk pulse as shown in truth table.

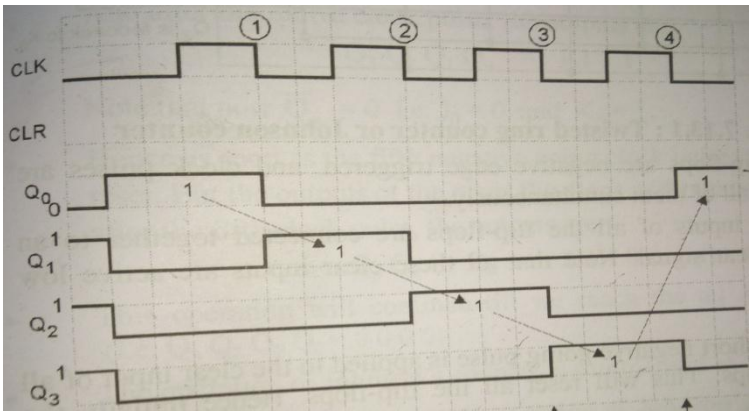


Fig: Waveform of 4 bit Ring counter

e) Describe successive approximation ADC with neat circuit diagram.
Ans:-(Diagram – 2 mks, explanation-2 mks)

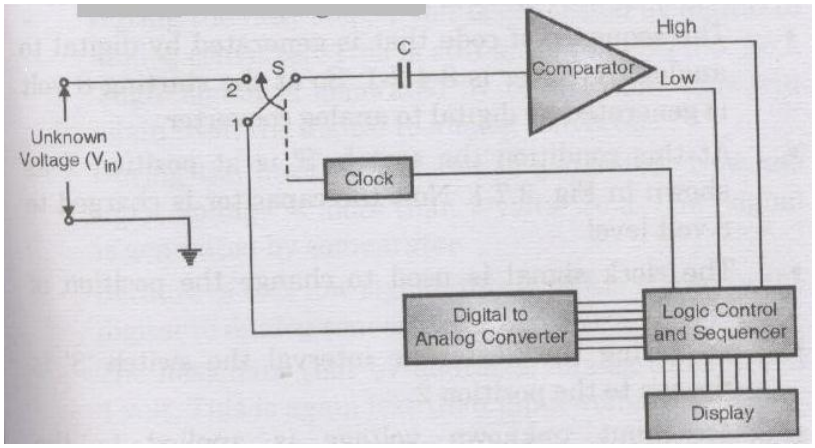


Fig: successive approximation ADC

Working:-

1. Consider that unknown voltage to be measured is 3.2135 volts. Also consider that digital to analog converter generates the codes 8- 4- 2- 1.
2. Initially the digital to analog converter is reset. The sequence of code that is generated by digital to analog converter is 8-4-2-1. So at the starting 8 volt is generated by digital to analog converter.
3. At this condition the switch, So is at position 1. Now the capacitor is charged to 8 volt level. The clock signal is used to change the position of switch.

4. So during the next time interval the switch, So is thrown to the position 2. An input Unknown voltage is applied to the capacitor. The capacitor was charged to 8 volt.
5. If input voltage is more than the voltage stored across the capacitor then the current flows into the comparator.
6. However if this input voltage is less than the capacitor voltage then the current flows in opposite direction. Now when the current flows into the comparator then high signal is generated. And when the current flows in opposite direction then low signal is generated by the comparator.
7. The generation of high signal causes the resetting of digital to analog converter. While during the generation of low signal; the data generated by digital to analog converter is retained. Here an input voltage to be measured is 3.2135.
8. Initially the digital to analog converter generates 8 volts. The comparator compares thes two voltages. Now a high signal is generated. This will reset the digital to analog converter.
9. During the next step, 4 volts is generated by digital to analog converter. This is still more than 3.2135. So a high signal is generated by comparator. This will again reset the digital to analog converter. Because of this low signal; this 2 volt is stored in the digital to analog converter.
10. The next data sent by digital to analog converter is 1 volt. This is again less than input voltage. So a low signal is generated by the comparator. Now this 1 volt is retained in digital to analog converted, so the voltage level I it becomes 2 + 1 = 3 volts.
11. This process takes place continuously until the signal in digital to analog converter

becomes equal to unknown input voltage.

f) Compare static and dynamic RAM (any 4 points).
Ans:-(Relevant 4 points- 4 mks)

Parameter	**Static RAM**	**Dynamic RAM**
1) Circuit configuration	Each SRAM cell is a flip flop	Each cell is one MOSFET & a capacitor
2) Bits stored	In the form of voltage	In the form of charges
3) No. of components per cell	More	Less
4) Storage capacity	Less than DRAM	More than SRAM

5. Attempt any four 16

a) Draw the circuit of TTL totem pole input NAND gate and explain its working.

Ans:-(Diagram- 2 mks, truth table with explanation-2 mks)

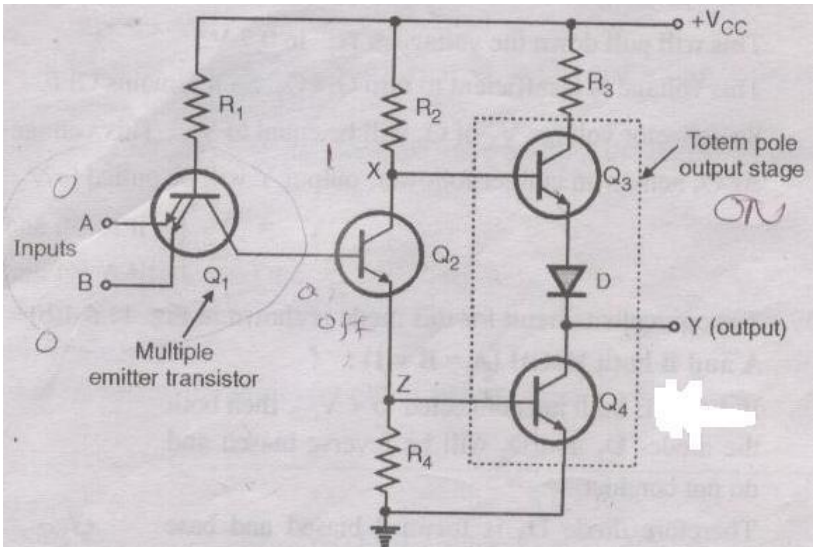


Fig: TTL totem pole two input NAND gate

Truth Table

Input		Output
A	B	Y=A.B
0	0	1
1	0	1
0	1	1
1	1	0

Operating Principle:

1. A and B both LOW (A = B =0):

- If A and B both are connected to ground, then both the B- E junctions of transistors Q1 are forward biased.
- Hence diodes D1 and D2 will conduct to force the voltage at point C to 0.7 V.
- This voltage is insufficient to forward bias base emitter junction of Q2. Hence **Q2 will remain OFF.**
- Therefore its collector voltage Vx rises to Vcc.
- As transistor Q3 is operating in the emitter follower mode, output Y will be pulled up to high voltage. **Therefore, Y =1 (HIGH) …..For A =B= 0 (LOW)**

2. Either A or B LOW (A =0, B=1 or A=1, B=0):

- If any one input (A or B) is connected to ground with the other terminal left open or connected to +Vcc, then the corresponding diode (D1 & D2) will conduct.
- This will pull down the voltage at "C" to 0.7 V.

- This voltage is insufficient to turn ON **Q2. So it remains OFF.**
- So collector voltage Vx of Q2 will be equal to Vcc, voltage acts as base voltage for Q3.
- As Q3 acts as an emitter follower, output Y will be pulled to Vcc.
- **Y= 1 ---- if A=0 and B=1 -----if A=1 and B=0**

3. A and B =1

- If A and B both are connected to +Vcc, then both the diodes D1 & D2 will be reverse biased and do not conduct.
- Therefore diode D3 is forward biased and base current is supplied to transistor Q2 via R1 and D3.
- As Q2 conducts, the voltage at X will drop down and **Q3 will beOFF,** whereas voltage at Z (across R3) will increase **to turn ON Q4.**
- As Q4 goes into saturation, the output voltage Y will be pulled down to a low voltage, **Y=0.**

b) Draw and explain the circuit diagram of 1:4 demultiplexer using logic gates.
Ans:-(Diagram-2mks, Explanation with truth table- 2 mks)

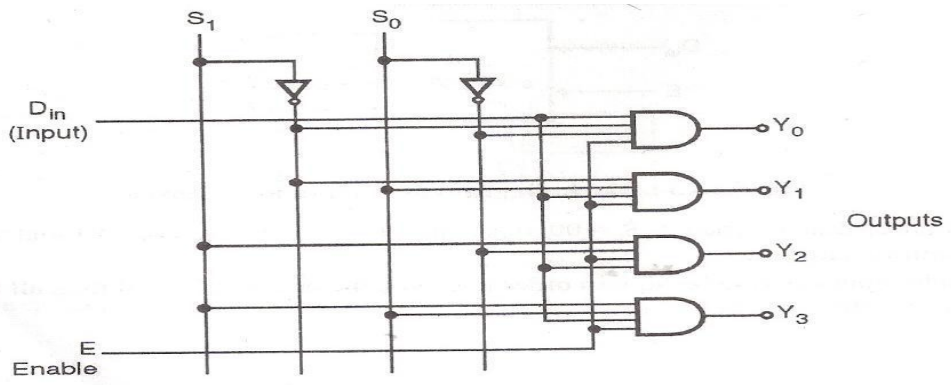


Fig: 1:4 Demultiplexer using logic gates

Explanation:
As shown in figure Din is the data input to Demux.
E is the enable input which needs to be high to enable the working of the Demux .
If E=0 then all the outputs will be low irrespective of the inputs.
S0 to S3 are the select lines. As per the combination of select lines the data Din will be available at one of the Y outputs.
Example Din will be available at Yo when S1S0 =00, it is available at Y1 when S1S0= 01 and so on, as shown in the truth table.

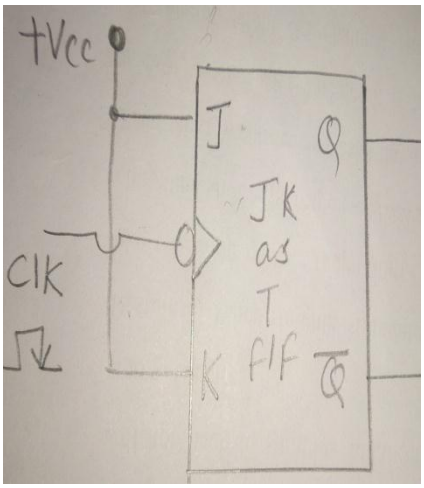
Truth Table for 4:1 MUX.

Din	E	S_0 S_1 Select lines	Y_0 Y_1 Y_2 Y_3 o/p.
1	0	X X	0 0 0 0
1	1	0 0	1 0 0 0
1	1	0 1	0 1 0 0
1	1	1 0	0 0 1 0
1	1	1 1	0 0 0 1

c) Explain with neat diagram how to convert JK flipflop into TFF? Write truth table.
Ans:-(Explanation- 1mks, truth table-1 mks, Diagram- 2 mks)

Explanation- JK flipflop can be converted to T flipflop by connecting both the inputs J and K together to +VCC .

With this connection ,for every clock applied the o/p Q_{n+1} will toggle to the opposite state ie . o/p will change from 0 t1 and from 1 to 0 for every clock. as shownin the truth table as Qn and $Q\bar{n}$.



Clock	T=1	Q_{n+1}
0	0	Q_n
1	0	Q_n
1	1	$\bar{Q}_n$
1	1	Q_n
1	1	$\bar{Q}_n$

d) How can IC 7490 be used as a decade counter with neat block diagram.
Ans:-(Explanation-1 mks , diagram -2 mks, truth table- 1mks)

Explanation- IC 7490-It consists of two counters namely MOD 2 and MOD 5. Thus IC 7490 can be used as MOD 2 or MOD 5 counter independently. Ehen this IC need to be used as MOD 10 ie decade counter, the o/p of MOD 2 counter ie QA need to be connected to the clock i/p of MOD 5 counter as shown below thus acting as a 4 bit MOD 10 counter.

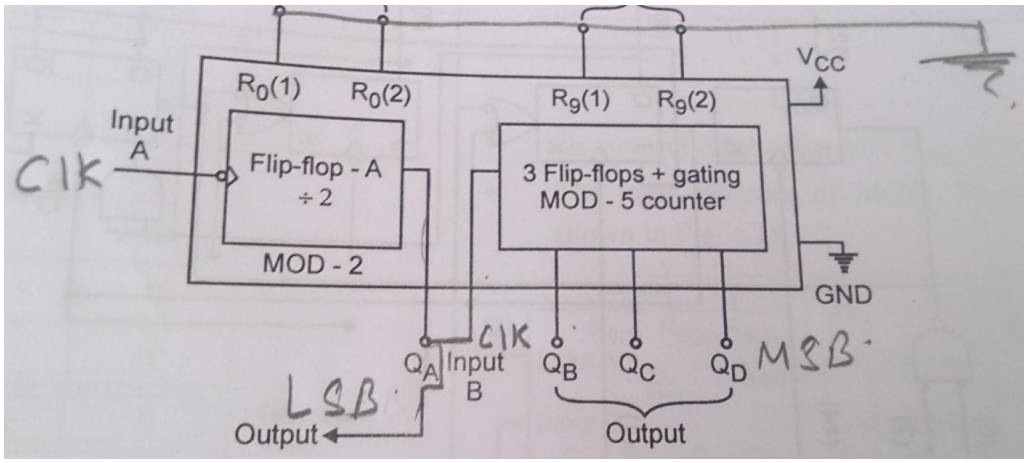


Fig: IC 7490 be used as a decade counter

Truth Table	
Decimal i/p	BCD/decimal o/p: D C B A
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
0	0 0 0 0

e) How many bits are required for a resolution of 5 mV and full scale voltage is 15 V.
Ans:-(Formula 1 mks,proper answer- 3 mks)

Soln. Given : $V_{FS} = 15\,V$

Resolution = 5 mV

To find : n = ?

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

$$5 \times 10^{-3} = \frac{15}{2^n - 1}$$

$$2^n = 1 + \frac{15}{5 \times 10^{-3}} = 1 + 3000 = 3001$$

$$\therefore\ n = \log_2 3001$$

$$= \frac{\log 3001}{\log 2} \approx 12 \text{ bits}$$

$$\therefore\ \boxed{n = 12 \text{ bits}}$$ **Ans.**

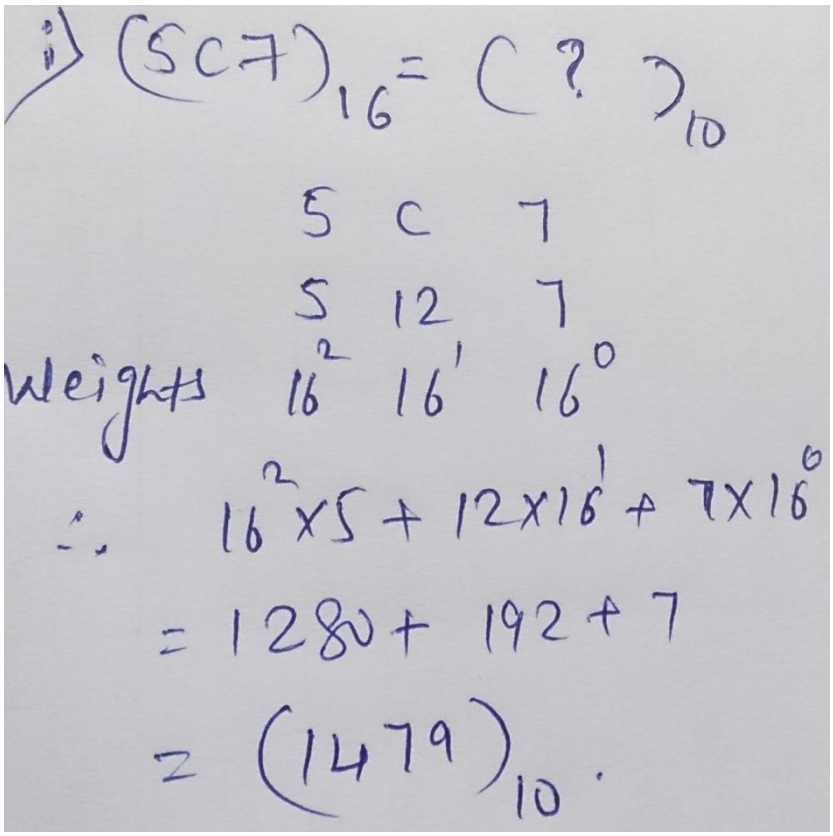
f) Compare volatile and non volatile memory.(any 4 points).
Ans:-(Relevant 4 points- 4 mks)

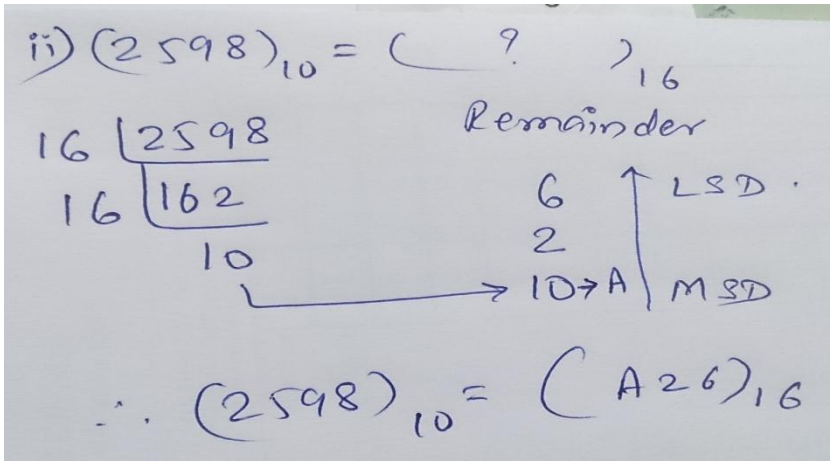
Sr. No.	Parameter	Volatile	Non-volatile
(1)	Definition:	Information stored is lost if power is turned OFF.	Information stored is not lost even if power goes OFF.
(2)	Classification:	All RAMs.	ROMs, EPROMs.
(3)	Effect of power:	Stored information is retained only as long as power is ON.	No effect of power on stored information.
(4)	Application:	For temporary storage of data.	For permanent storage of data

6. Attempt any four **16**

a) Convert the following:
i) $(5C76)_{16}=(?)_{10}$
ii) $(2598)_{10}=(?)_{16}$
iii)$(10110)_2=(?)_{10}+(?)_{16}$

Ans:-(for i) and ii) -1 mks each for proper conversion; for iii) -2 mks for conversion)





iii) $(10110)_2 = (\ ?\ )_{10} = (\ ?\ )_{16}$

1 0 1 1 0

2^4 2^3 2^2 2^1 2^0 Weights.

ie $2^4 \times 1 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$

$16 + 0 + 4 + 2 + 0$

$= (22)_{10}$. Ans

0001 0110 (grouping in a group of 4 bits)

1 6

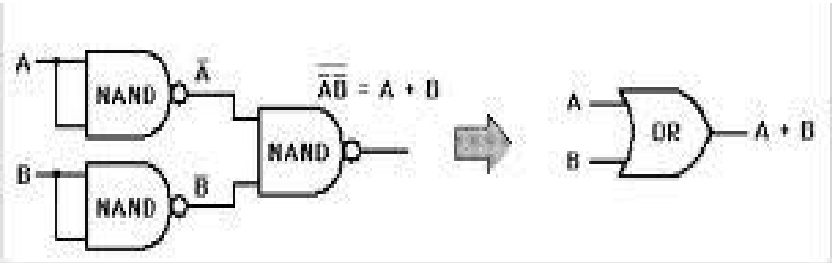
ie $(16)_{16}$.

b) Why NAND and NOR gates are called as an universal gates? Realize OR gate using NAND gate.

Ans:-(Reason- 2 mks, Realisation using NAND gate- 2 mks)

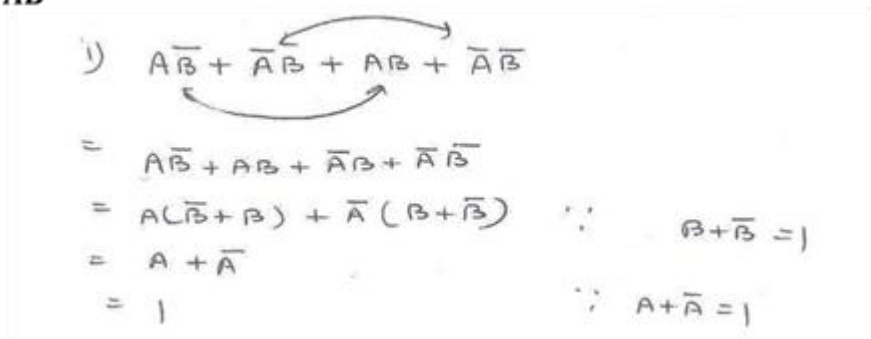
NAND and NOR gates are called as an universal gates because-(2 points)

1. We can implement any other gate (AND, OR, NOT, EX- OR, EX- NOR) using NAND or NOR gates only.
2. It is possible to implement any Boolean expression with the help of only NAND or NOR gates.
3. Hence a user can build any combinational circuit of any complexity with the help of only NAND or NOR gates .

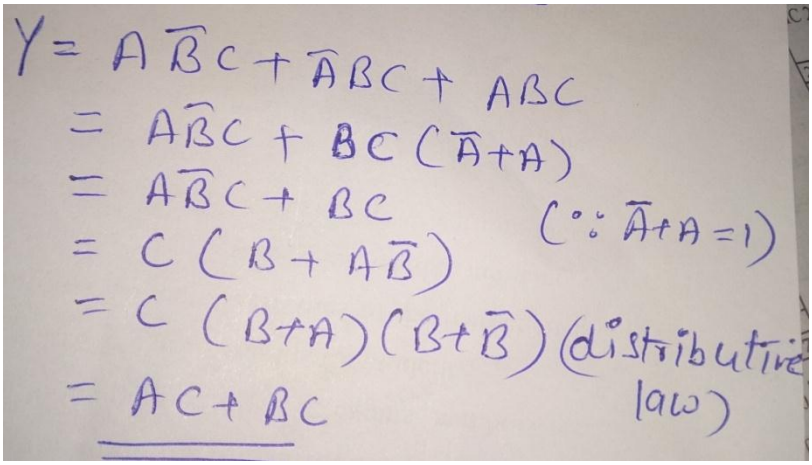


c) Reduce the following Boolean expression using Boolean laws:
Ans:-(proper answer- 2 mks for each)

$A\overline{B} + \overline{A}B + AB + \overline{A}\,\overline{B}$



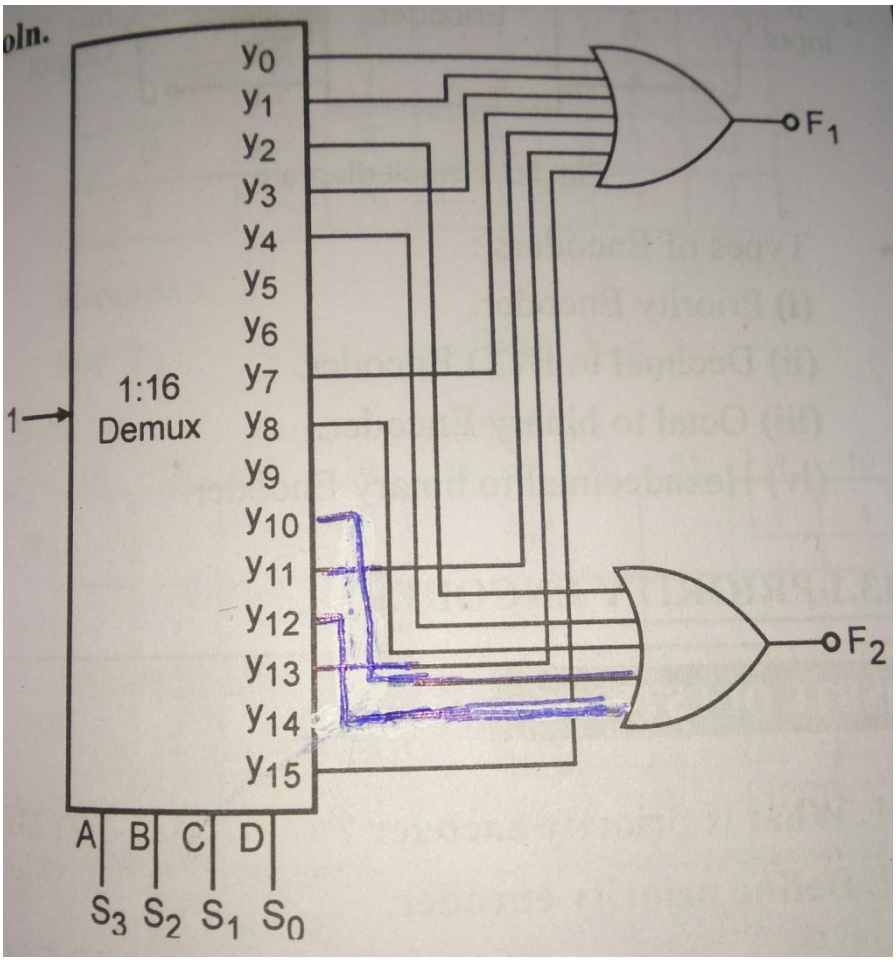
ii)



d) Realize the following function using demultiplexer:
Ans:-(proper answer- 2 mks for each)

i) F1=Σm(0,1,3,7,11,13,15)

ii) F2=Σm(2,4,8,10,12)



e) Design MOD 10 asynchronous up counter,with its truth table and timing diagram.
Ans:-(Diagram – 2 mks, truth table- 1 mks, timing diagram-1 mks)

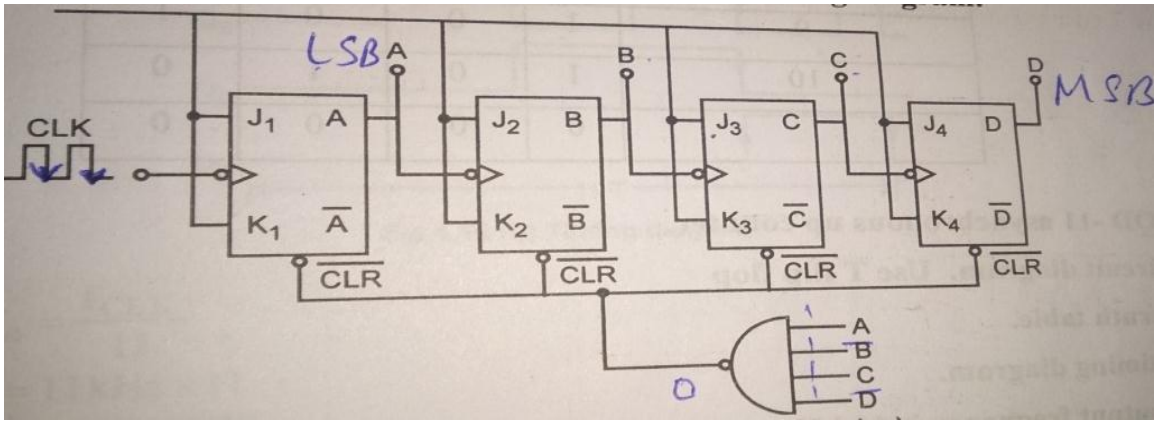


Fig: MOD 10 asynchronous up counter

Number of clock pulses	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

Repeat

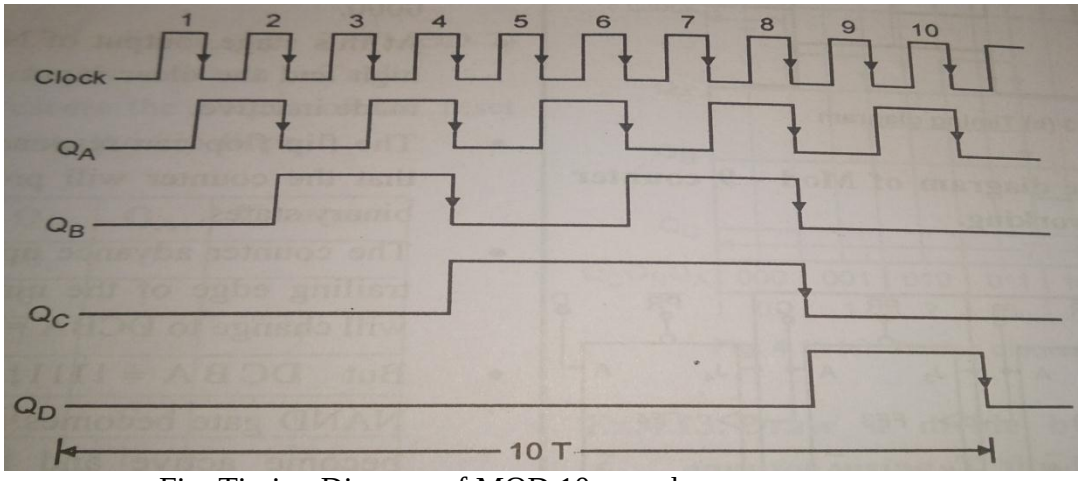


Fig: Timing Diagram of MOD 10 asynchronous up counter

f) Calculate the analog output of a 4 bit DAC if the digital input is 1011. Assume V_{FS}=5V.
Ans:(Formula -1 mks, proper answer – 2 mks)

Given : The 4 bit digital word is

$$d_1\, d_2\, d_3\, d_4 = 1011 \text{ with}$$

$$V_{FS} = 5 \text{ volts}$$

To find : $V_o = ?$

$$V_o = V_{FS}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4}\right]$$

$$V_o = 5[1 \times 2^{-1} + 0 + 1 \times 2^{-3} + 1 \times 2^{-4}]$$

$$= 5[0.5 + 0.125 + 0.0625]$$

$$= 3.4375 \text{ volts.}$$

$$\therefore \boxed{V_o = 3.4375 \text{ Volts}} \quad \textbf{Ans.}$$