

MODEL ANSWER

SUMMER- 17 EXAMINATION

Subject Code:

17658

Subject Title: EMBEDDED SYSTEM

Important Instructions to examiners:

- 1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
- 2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
- 3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
- 4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
- 5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
- 6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
- 7) For programming language papers, credit may be given to any other program based on equivalent concept.

Sub Q.N.	Answe	er		Marking Scheme
a)	Attempt any <u>THREE</u> of the following:			12-Total Marks
(i)	State the interrupts used in 89C51? Give the	ir priorities and vector	r addresses.	4M
Ans:				4 M
	Interrupt	Vector	Priority	
		Address		
	IE0 / (External interrupt 0, INT0)	0003H	1	
	TF0 / (Timer 0 Interrupt)	000BH	2	
	IE1 / (External interrupt 1, INT1)	0013H	3	
	TF1 / (Timer 1 Interrupt)	001BH	4	
	TI or RI (serial port interrupt)	0023H	5	
(ii)	Write difference between synchronous and a	synchronous data com	munication.	4M
Ans:				(Any four points 1 M each)



	Sr. No.	Synchronous	Asynchronous	
	1	Same clock pulse is required at transmitter and receiver	Different clock pulse is required at transmitter and receiver	
	2	Used to transfer group of character	Used to transfer one character at a time	
	3	Synchronous character is required.	Synchronous character is required.	
	4	No start and stop signals are required	Start and stop signals are required.	
	5	Data transmission rate is greater then or equal to 20Kbps	Data transmission rate is less then or equal to 20 Kbps.	
	6	It is less reliable	It is more reliable	
(***)	T . 4 1			43.4
(m)	compiler and	ware development tools in an embe d debugger.	edded system and state the function of	4 <u>M</u>
AIIS:	 Compiler Cross assen Cross comp Locators Loaders Simulators Debugger Integrated d The function 1) Composition 	nbler iler development environment (IDE) a of compiler piler: - It is a computer program the ramming or source language into age i.e. binary code known as object	at transforms the source code written in a another computer language i.e. target t code.	(List: 2M, Explanatio n compiler: 1M, Debugger:1 M)
	The function	n of debugger.		
	2) Debu contr featur chip execu (execu execu	agger: - Allows you to download yo ol all of the functions of the emi- res include the capability to examin registers, data- and program-ma- nating at defined program locations bute one instruction at a time) throu- nated code (trace).	ur code to the emulator's memory and the ulator from a PC. Common debugging he and modify the microcontroller's on- emory; pausing or stopping program by setting breakpoints; single-stepping high the code and looking at a history of	
(iv)	Draw interfa	ncing diagram of 4*4 matrix keybo	oard with 89C51 mico controller (No	4M
	Prostanii)			



Ans:	Matrix Keyboard Connection to portsVcc $3 \times 2 \times 1 \times 0$ $3 \times 2 \times 1 \times 0$ 0×1 <th>(Correct labelled diagram-4 M)</th>	(Correct labelled diagram-4 M)
b)	Attempt any <u>ONE</u> of the following:	6M
(i)	Describe the methods of task synchronization and explain any one in details.	6M
Ans:	 The methods of task synchronization are: Synchronization primitives Semaphore: counting semaphore and binary semaphore A semaphore is created with initial count, which is the number of allowed holders of the semaphore lock. (initial count=1: binary sem). Sem wait will decrease the count; while sem_signal will increase it. A task can get the semaphore when the count > 0; otherwise, block on it. Mutex: similar to a binary semaphore, but mutex has an owner. A semaphore can be "waited for" and "signaled" by any task, while only the task that has taken a mutex is allowed to release it. Spinlock: lock mechanism for multi-processor systems, A task wanting to get spinlock has to get a lock shared by all processors. Read/write locks: protect from concurrent write, while allow concurrent read Many tasks can get a read lock; but only one task can get a write lock. Before a task gets the write lock, all read locks have to be released. Barrier: to synchronize a lot of tasks, They should wait until all of them have reached a certain "barrier." 	(Task synchroniza tion Methods: 3 M and Any one explanation : 3M)
	threads of execution with an application must be able to synchronize their execution & co-ordinate mutually exclusive access to shared resources. To fulfill this requirement RTOS kernel provides a semaphore object that one or more threads of execution can acquire or release for the purpose of synchronization or mutual exclusion. Semaphore is	



like a key that allows a test to carry out some operation or to access a resource A kernel supports many different types of semaphores Binary: Binary semaphores are used for both mutual exclusion and synchronization purposes. A binary semaphore is used to control sharing a single resource between tasks.. Counting: it is a semaphore that increments when an IPC is given by a task. It decrements when a waiting task unblocks and starts running. **Counting Semaphore** Shared Resource Unavailable Shared Resource Available Shared Resource Available Shared Shared Shared Resource Resource Resource Semaphore (count=1) Semaphore Semaphore (count =0) (count=1) (l) Task B attempt to Task A release acquire semaphore semaphore Task A Task A Task B Task A Task B Task B Task A acquired Task A acquired Task B acquired Task B acquired

Task A acquired semaphore

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Mutex:Mutexes are binary semaphores that include a priority inheritance mechanism. Mutexes are the better choice for implementing simple mutual exclusion (hence 'MUT'ual 'EX'clusion). A **mutex** allows exclusive access to the resource. The long form is Mutually Exclusion Semaphores (semaphore value of 0 or 1 but lock count can be 0 or greater for recursive locking). A mutex is intended to protect a critical region. Mutex is similar to a binary semaphore, but mutex has an owner. The main difference is that a semaphore can be "waited for" and "signaled" by any task, while only the task that has taken a mutex is allowed to release it.

semaphore

semaphore

semaphore









1. Embedded processor: It is the heart of the embedded system. It has two essential units : control unit and execution unit. Control unit fetches instructions from memory and execution unit includes ALU and circuits to perform execution of the instructions for a program control task

2. Power supply, reset & oscillator circuit:

- Most of the systems have their own power supply. Some embedded systems do not have their own power supply. These embedded systems are powered by external power supply e.g. USB based embedded system, network interface card, Graphics Accelerator etc. are powered by PC power supply.
- Reset means that processor begins processing of instructions from starting address set by default in program counter on power up.
- The clock circuit controls execution time of instructions, CPU machine cycles.

3. Timers: Timer circuit is suitably configured as system clock or RTC (Real time clock). To schedule various tasks and for real time programming an RTC (Real Time Clock), or system clock is needed.

4. Program & data memory: In embedded system, secondary memory like disk is avoided. Most of the embedded processors have internal memory such as ROM, RAM, flash/EEPROM, EPROM/PROM for storing program and data.

5. Interrupt controller: It is an interrupt handling mechanism which must exist in embedded system to handle interrupts from various processes and for handling multiple



		interrupts simultaneously pending for service	
		6. I/O ports: I/O ports are used to interface external devices like sensors, key buttons, transducers, LEDs, LCD actuators, alarms, motors, values, printer etc. There are two types of ports, parallel and serial port. The parallel ports are used in short distance communication while serial ports are used in long distance communication.	
		7. Input & output device interfacing/driver circuits: Some I/O devices like motors, actuators, valves, sensors are not compatible with the processor. Hence the I/O interface circuits are designed to drive such input and output devices interfaced to the embedded processor	
		8. System Application specific circuits: These are the circuits that can control specific target circuits. They consist of ADC, DAC, relays, sensors etc.	
Q. 2		Attempt any <u>FOUR</u> of the following:	16M
	a)	State any four advantages of an embedded systems.	4M
	Ans:	 Advantages of an embedded systems- 1. Design and Efficiency: The central processing core in embedded system is generally less complicated, making it easier to design. The limited function required of embedded system allows them to design to most efficiently perform their function. 2. Cost: The streamline make-up of most embedded system allows their parts to be smaller less expensive to produce. 3. Accessibility: If something goes wrong with certain embedded systems they can be too inaccessible to repair. This problem is addressed in the design stage, so by programming an embedded system. So that it will not affect related system negatively when malfunctioning. 4. Maintenance: Embedded systems are easier to maintain because the supplied power is embedded in the system and does not required remote maintenance. 5. Redundancies: Embedded system does not involve the redundant programming. 	(Any four- 1 M each)
	b)	Draw the format of TMOD SFR and write significance of each bit.	4M
	Ans:	MSB LSB	(Format- 2M, Description - 2M)
		GATE C/T M1 M0 GATE C/T M1 M0	
		← Timer 1 → ← Timer 0 →	



	GATE : S	Starts an 1 –	nd stop - Timer	s Timer / (/ counter	Counter by means of a signal provided to the pin INT1 / INT0 operates only if the bit INT1 / INT0 is set	
			Timer	/ Counter	constates regardless of the state of the bit INT 1 /INTO	
	<u> </u>	U -	C	/ Counter	Clause 1 for The respective Clause for the bit 11/11/10/10	
	C/I : 1	Set į	for Coun	unter oper	ration (input from Tx input pin).	
	M1, <u>M0 :</u>	Thes	e two b	vits selects	s the Timer operating modes.	
		Ml	M0	Mode	Description	
		0	0	0	13-bit timer	
		0	1	1	16-bit timer	
		1	0	2	8-bit auto-reload	
		1	1	3	Split mode	
c) D fu i	raw the int nction of i. RS ii. EN ii. R/W	erfaci	ing di	agram	of 16*2 LCD display with 89C51 and state the	4M
c) D fu i ii	raw the int nction of i. RS ii. EN ii. R/W	erfaci	ing di	agram	of 16*2 LCD display with 89C51 and state the	4M
c) D fu i i Ans:	raw the int nction of i. RS ii. EN ii. R/W	erfaci	ing di	agram	of 16*2 LCD display with 89C51 and state the	4M (Interfaci g diagra 1M, function each pin
c) D fu j ii Ans:	raw the int inction of i. RS ii. EN ii. R/W	P2. P2. P2.	0 1 2		of 16*2 LCD display with 89C51 and state the	4M (Interfaci g diagra 1M, function each pin M)



	Function:	
	RS: - RS is used to make the selection between data and command register.	
	RS=0, command register is selected	
	RS=1 data register is selected.	
	RW: -R/W gives you the choice between writing and reading.	
	R/W=1, reading is enabled. R/W=0 then writing is enabled.	
	EN: -Enable pins are used by the LCD to latch information presented to its data pins. When data is supplied to data pins, a high to low pulse must be applied to this pin in-order for the LCD to latch in the data present at the data pins.	
d)	Write 89C51 "C" language program to toggle all bits of port P_2 continuously with 500 ms delay.	4M
Ans:	NOTE: Program may change. Student can also use the other logic.	(Correct
	Please check the logic and understanding of students.	program-
		4M)
	#include <reg51.h></reg51.h>	
	void delay (unsigned int);	
	while(1) //repeat loop	
	P2=0xff; //toggle all bits of port2 delay (500), //add delay	
	delay (500) ; //add delay P2=0x00; //toggle all bits of port2	
	delay (500): //add delay	
	} }	
	}	
	Vold delay (unsigned int i)	
	Unsigned int x, y;	
	for(x=0; x< i; x++)	
	for (y=0; y<1275; y++);	
	}	
e)	Differentiate between CAN and I [*] C protocols with respect to	
	1. Data transfer rate	
	II. Number of fields	
	III. Addressing bits	
	IV. Application	



Ans:		I2C	CAN		(1M each
	Data transfer	Synchronous with 3 speeds 100kbps, 400kbps and 3.4mbps	Asynchronous with 250kbps upto 1mbps.		point)
	Number of field	07	08 (including 7 bits of frame end and 3 bits of inter frame gap)		
	Addressing bit	7-bit or 10-bit address	11 bit		
	application	To interface devises like watch dog, flash &RAM memory, Real time clock, Microcontrollers	elevator controllers, copiers, telescopes, production-line control systems, and medical instruments		
f)	Describe semapho	ore with suitable example.			4M
Ans:	Semaphores: It threads of execution co-ordinate mutual RTOS kernel provi acquire or release like a key that allow supports many different Binary: Binary supproves. A binary	is a system of sending mess on with an application must b lly exclusive access to shared vides a semaphore object that for the purpose of synchronic ows a test to carry out some of erent types of semaphores semaphores are used for both y semaphore is used to control	age by using flags. Multiple co e able to synchronize their exec d resources. To fulfill these requires one or more threads of execut zation or mutual exclusion. Seman peration or to access a resource A th mutual exclusion and synchro- sharing a single resource between	ncurrent ution & uirement tion can ohore is A kernel onization n tasks.	(Descript on of semaphore - 3M, Example-1 M)
	Its internal counter A semaphore test p proceed.	er can have only the values passes if the count is 1, in wh	of 1 (available) and 0 (unav hich case, the current task is allo	vailable). wed to	







		token. When it has finished with the resource it must 'give' the token back - allowing other tasks the opportunity to access the same resource.	
		Example of using semaphores for Synchronization:	
		Assume two concurrent processes P1 and P2 having statements S1 and S2. We want in any case S1 should execute first. this can be achieved easily by initialize Sem=0; In process P1 { // Execute whatever you want to do // before executing P2 S1; signal(Sem);	
		<pre>} in process P2 { wait(Sem); S2; }</pre>	
Q. 3		Attempt any <u>FOUR</u> of the following:	16M
	a)	 Find the content of Accumulator after execution of the following code i. ACC = 0*94>>5; ii. ACC = 0*5A<<2; 	4M
	Ans:	i) ACC= 0*94>>5 Ans: ACC= 0*04 ii) ACC= 0*5A<<2 Ans: ACC= 0*68	2 M each
	b)	Write any four feature of RTOS.	4 M
	Ans:	 <u>Reliability:</u> A reliable system is the system which is available all the time. A system that does not fail is a reliable system. RTOS is reliable but it does not guarantee the reliability of an embedded system. The reliability of an ES depends on the hardware, the application code. <u>Predictability:</u> RTOS have predictable behavior in which the completion of OS calls occurs within known time frame. <u>Performance:</u> The system must perform fast enough to fulfil the timing requirements. The performance of RTOS can be measured on a call-by-call basis. Time stamps are produced when a system call starts and when it completes. This method of analyzing is useful in designing stage but the true performance is measured as whole. <u>Compactness:</u> RTOS used in embedded system are extremely constraint as far as resources are concerned. The design requirements limit the system memory which limits the size of the application and the operating system. <u>Scalability:</u> RTOS are most used in variety of embedded system they must be able to scale up/down to suit the application. 	1M each
	c)	Write 89C51 "C" language program to rotate stepper motor by 180 ⁰ in clockwise	4M
		direction motor has step angle 1.8°. Use stepper moter of 4 step pulse sequence.	







e)	 2. Throughput: The system may need to handle a lot of data in a shirt time. 3. Response: The system has to react to the changing events quickly. 4. Memory: Hardware design must make the best estimate of the memory requirement and must make the provision for expansion. 5. Power consumption: Systems generally work on battery and design of both software and hardware must take care of power saving techniques. 6. Number of units: The number of units expected to be produced and sold will dictate the trade-off between production cost and development cost. 7. Expected life-time: Design decisions like selection of components to system development cost will depend upon on how long the system is expected to run. 8. Program Installation: Installation of software on to the embedded system needs special development tools. 9. Testability and Debug ability: Setting up test conditions and equipment will be difficult and determining what is wrong with the software will become a difficult task without a keyboard and usual display. 10 Reliability: It is always required that the system designed must give the output for which it is designed. 	4M
Ans:	 Multiple device connection: Upto 127 different devices can be connected on single USB bus. Transfer rate: The initial USB supported 12 MBps transfer rate where USB 2.0 supports higher rate currently 60 MB/sec. Support for large range of peripherals: Low bandwidth devices such as keyboard, mouse, joystick, and game -port, FDD. Hub architecture: The devices are not daisy chained. Each device is connected to an USB hub. The USB hub interacts with PC on one side and peripheral on other side. Plug ability: The USB device can be connected without powering off a PC i.e. plug and play feature in BIOS together with the device takes care of detection, handling and device recognition. Power allocation: USB controller in the PC detects the presence or absence of the USB devices and does the allocation of power. Ease of installation: There is only one cable. A 4-pin cable carries signals like power signal (-), signal (+), ground. Host centric: The CPU software initiates every transaction on the USB bus. Hence the overhead on the PC increases when there are large number of peripherals involving large number of transactions. 	(Any 4 1 M each)
Q.4 A) i)	Attempt any <u>THREE</u> of the following: Explain I ² C protocols with suitable diagram.	12M 4M



Ans: I²C Bus: In any process plant there are n numbers of device circuits that are used for (Explanatio measurement of temperature, pressure and it is required to connect these ICs through a n:2M, common bus. For this I²C has become a standard. There are three standards: format: 2M) Industrial 100 kbps I²C. • 100 kbps SM I²C. 400 kbps I²C. • The I²C bus has two lines that carry its signals. One line is for the clock and another is for the bi-directional data. Serial data line [SDA] and Serial Clock [SCL]. The voltages used are +5 V and +3.3 V. There is a protocol for the I²C bus. Typical I²C Bus Vdd SDA I²C SCL Master 1 I²C I²C I²C Slave 1 Slave 2 Master 2 The format of bits at the I²C bus is as shown: 1 7 1 1 8 1 s Slave Address Wr Ρ Α Data Byte х х А Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK) Ρ Stop Condition Read (bit value of 1) Rd s Start Condition Repeated Start Condition Sr Wr Write (bit value of 0) х Shown under a field indicates that that field is required to have a value of X Continuation of protocol Master-to-Slave Slave-to-Master



Field and its length	Description
1 st field of 1 bit	It is like a start bit in UART
2^{nd} field of 7 bits	It is address field. It defines the slave address, which is being
	sent the data frame by the master.
3 rd field of 1 control bit	It defines whether a R/W cycle is in progress.
4 th field of 1 control bit	Defines whether the present data is an acknowledgement.
5 th field of 8 bits	It is for the IC device data byte.
6 th field of 1-bit	It is a NACK (No Acknowledgement). If active then ACK is
	not needed from the slave, else ACK is needed.
7 th field of 1 bit	Similar to STOP bit in an UART.

I²C Bus reference design has 7 bit address space with 16 reserved addresses, so a maximum 112 nodes can communicate on the same bus.

Each device has an unique address using which the data transfer is carried out. The master can address have 127 slaves at an instance.

It has a processing element functioning as a bus controller or a microcontroller with I^2C bus interface circuit.

So each slave must have an I²C bus controller and processing element. A number of masters can also connect to bus but there can be only one master which can initiate data transfer on SDA line and which can transmit the SCL pulses.

Common I²C Bus speeds are 100 Kbps standard mode and 10 Kbps low speed mode.

Advantages:

- 1. Multiple slave devices can be accessed with only 2 wires.
- 2. Low cost to implement.
- 3. Implemented in hardware and software.
- 4. Ease to implement.
- 5. Supports multi-master configuration.

Dis-Advantages:

- 1. Short distance.
- 2. Slow speed.
- 3. Limited device addresses.

<u>Applications of I²C Bus</u>: I²C Bus is used for peripherals where simplicity and low manufacturing cost are more important than speed.

- 1. Supporting systems management for PCI cards.
- 2. Accessing NVRAM chips that keep user settings.
- 3. Accessing low speed DAC's and ADC's.
- 4. Changing constrast, hue and colour balance settings in monitors.
- 5. Changing sound volume in intelligent speakers.
- Controlling OLED/OLCD displays in cell phones

ii) Differentiate between General purpose operating system and RTOS (any four 4M points).



Ans:								
	Sr no		OS			RTO	S	(Anv 4
	1	Non-Determ	ninistic time be	ehaviour.	I	Deterministic time	behaviour.	noint·1M
	2	Used in gen	eral desktop c	omputer syste	m. U	Jsed in embedded s	system	for each
	3	Generalized	Kernel.		F	Real time kernel.		point)
	4	OS service	s can inject	random dela	ays into (OS services consun	nes only known	
		application	software,	may cause	e slow a	nd expected amou	nts of time	
		responsivene time.	ess of an app	lication at une	expected r	egardless the numb	per of services.	
	5	Ex: Window	s XP, MS-DO	DS	I	Ex: Windows CE.		
;;;)	Difform	tists botwo	n DISC and		nuton			
Ш) Алас	Differen	mate betwee	en RISC and	I CISC com	puter.			4IVI
Ans:								(INI for each point)
	Sr no.	RISC: R	educed Instr t Computer	uction	CISC: Co	omplex Instruction et Computer	n	
	1	Emphasis	on software.		Emphasis	on hardware		
	2	Single clo	ck, reduced ir	struction.	Multiclock	, complex instruct	ion set.	
	3	Register-I are indepe	Register, load endent of instr	d and store uction.	Memory-N incorporat	Memory, load ed.	and store are	
	4	Large cod	le size.		Small cod	e size.		
	5	Spends m	ore transistors	s on memory	Transistor	s used for s	storing complex	
		registers.			instruction	S.		
iv)	Write tl	he definition	of an embe	dded systen	n? How it i	s classified?		4M
Ans:	An embe	edded system	is a comput	er system wi	ith a dedica	ted function with	in a larger	(Define:1
	mechanic	cal or electric	cal system, o	often with rea	al-time con	nputing constraint	s. It	Μ
	is embed	lded as part	of a complete	device often	n including	hardware and m	echanical parts.	Classificati
	Embedd	ed systems c	ontrol many	devices in co	ommon use	today.	-	on
		2	2	Types Of En	ibedded	2		:3M)
				Syster	ns			, , , , , , , , , , , , , , , , , , ,
		,						
		Base Performance Require	d On & Functional ements		Bas Of 1	ed On The Performa The Microcontroller	nce	
	Ţ	Ļ	+		\mathbf{I}			
	Real Time	e Stand Alone	Networked	Mobile	Small Scale	Medium Scale	Sophisticated	
b)	Attempt	t any <u>ONE</u> o	of the follow	ing:				6M
i)	Draw in	terfacing di	agram of A	DC 0808 wit	h 89C51 r	nicro controller	and write 'C'	6M
	languag	e program	o read data	ITOIN ADC	0000.			



MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION (Autonomous) (IS O/IEC - 27001 - 2005 Certified)





	<pre>#include <reg51.h></reg51.h></pre>			
	spit ALE = PZ 4;			
	sbit $SC = P2^6$:			
	sbit EOC = $P2^7$:			
	sbit ADDR A = $P2^{0}$;			
	sbit ADDR B = P2^1;			
	sbit ADDR $C = P2^2;$			
	sfr MYDATA = P1;			
	void main()			
	{			
	unsigned char value;			
	MYDATA = 0xFF;		//make P1 an input	
	EOC = 1;		//make BOC an input	
	ABB = 0; OE = 0;		//clear OF	
	SC = 0;		//clear SC	
	while(1)		//cicul be	
	{			
	ADDR $C = 0;$		//C=0	
	ADDR B = 0;		//B=0	
	$ADDR_A = 1;$		//A=1 (Select Channel 1)	
	MSDelay(1);		//delay for fast DS89C4x0	
	ALE = 1;			
	MSDelay(1);			
	SC = 1;			
	MSDelay(1);			
	ALE = 0;		//	
	SC = 0;		//start conversion	
	while (EOC==1);		//wait for data conversion	
	OE = 1		//enable PD	
	MSDelay(1):		//enable hb	
	value = MYDATA;		//get the data	
	OE = 0;		//disable RD for next round	
	}			
	}			
ii)	Write 89C51 'C' program to trans	sfer 'YES' ser	ially at baud rate 9600 continuously	6M
	Use 8 bit data and 1 stop bit. Assu	me crystal fre	auency 11.0592MHz	
		inc crystar ne	quency interventing.	
		ine crystai ne		
		ine crystai ne	quency 11.00,20112.	
		ine crystai ire	quency 11100/201112.	
			quency most and z.	
		nik ciystai ne	quency most and z.	
		nik ciystai ne	quency most and z.	
		nik ciystai ne	quency most and z.	
		ink crystar rie	quency most and z.	
		ink crystar rie		
		ink crystar ric		
		ink crystar ric		
		ink erystar ne		
		ine erystar ne		
		ine erystar ne		
		ine erystar ne		



(

	Ans:			(Calculatio
		11.0592×10^{6}		n:
		clock == 921.6 KHz		2M
		921.6×10^{3}		Program:
		$UART = \frac{521.0 \times 10}{32} = 28800 Hz$		4M)
		52		
		28800		
		For Baud rate of 9600: $n = \frac{-3000}{9600} = 3 = ($	(-3) = FDH	
		program		
		<pre>#include <reg51.h></reg51.h></pre>		
		void SerTx(unsigned char):		
		void main(void)		
		1		
		IMOD=0x20;	// use Timer 1, mode 2	
		TH1=0xFD;	// 9600 baud rate	
		SCON=0x50;	// 01010000 Serial mode1	
		TR1=1;	// start timer	
		while (1)		
		{		
		SerTx('v');		
		SerTx('F):		
		SerTy('a')		
		Server S //	11 E- 4 - 614 H	
		3	// End of While	
		}		
		void SerTx(unsigned char x)		
		{		
		SBUF=x;	// place value in buffer	
		while (TI==0);	// wait until transmitted	
		TI=0;	// Clear TI Flag	
		}		
Q.5		Attempt any <u>FOUR</u> of the following:		16M
	a)	Draw the pin out of RS232 and describ	e the function of TXD, RXD, DTE and DCE.	4M
	AIIS:			(21VI IOF Diagram
				with labels
				1⁄2 M for



	RS232 Connector DB-9	RS	232 DB-9 Pins	each functions)
		Pin	Description	
		1	Data carrier detect (-DCD)	
		2	Received data (RxD)	
	0 0000 0	3	Transmitted data (TxD)	
		4	Data terminal ready (DTR)	
	6 7 8 9	5	Signal ground (GND)	
		6	Data set ready (-DSR)	
		7	Request to send (-RTS)	
		8	Clear to send (-CTS)	
		9	Ring indicator (RI)	
	DCE: Data communication equipment such the data.	as mode	m which is responsible for transferring	
b) Ans:	DCE: Data communication equipment such the data. Write 'C' language program to generate Note : Any ports pin can be defined for han combined . #include <reg51.h> unsigned char d; void main(void)</reg51.h>	as mode a triangu ndshakir	m which is responsible for transferring <u>lar waveform of DAC 0808.</u> <i>ng signals. Xfer/wr signal may be</i>	4M (2M for +ve ramp and 2M for -ve ramp Any logic



	OR	
	<pre>#include <reg51.lb> Sbit cs = P3^3; Sbit wr = P3^4; Sbit xfer = P3^5; void main() { unsigned Char x,y: cs = 0; while (1) { for (x=0; x<255; x++) { wr = 1; xfer = 1; P1 = x; xfer = 0; wr = 0; } for (y=255; y>0; y) { wr = 1; xfer = 1; P1 = y; xfer = 0; wr = 0; } }</reg51.lb></pre>	
c)	Describe deadlock in RTOS with suitable example.	4 M
Ans:	A deadlock consists of a <u>set</u> of blocked processes, each <u>holding</u> a resource and <u>waiting</u> to acquire a resource held by another process in the set A deadlock, also called as deadly embrace, is a situation in which two threads are each unknowingly waiting for resource held by other. $\frac{Example #1}{P_1 and P_2 each hold one disk drive and each need the other one.$ $\frac{Example #2}{P_0 \qquad P_1}$ Semaphores <i>A</i> and <i>B</i> , initialized to 1 <i>P</i> ₀ <i>P</i> ₁ wait (A); wait(B) wait (B); wait(A)	(Descriptio n- 3 M, Any one example- 1 M)



	Example 3	
	holds Taak 1 wants wants Task 2	
d) Ans:	 Task #1 wants the scanner while holding the printer. Task #1 cannot proceed until both the printer and the scanner are in its possession. Task #2 wants the printer while holding the scanner. Task #2 cannot continue until it has the printer and the scanner. Draw labelled interfacing diagram of DC Motor with 89C51 microcontroller.	4M
	+5V +5V +0V +0V +0V +0V +0V +0V +0V +0	(Labelled diagram 4M)
	C1 19 30 PF 33 PF X1 C2 11.6692MHz 18 XTAL2 20 20 20 20 20 20 20 20 20 2	



MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION (Autonomous) (IS O/IEC - 27001 - 2005 Certified)





		 This technique is not used for first time embedding of user written firmware. It modifies the program code memory under the control of embedded applications Examples: Updating calibration data, look up tables ,Boot ROM etc. in code 				
		memory.				
Q.6		Attempt any FOUR of the following:	16M			
	a) Ans:	 Attempt any <u>POUK</u> of the following: a) Describe parallel protocols PCI, PCI-X. Ans: PCI: PCI stands for Peripheral Component Interconnect/Interface bus. It is popular for higher bandwidth processor independent which can function as peripheral bus. It is introduced by Intel in 90's It is 32 bit local bus and extended up to 64 bit by processor it requires. It has high speed I/O subsystem performance. The PCI is designed to meet economically the i/o requirement of modern system. It supports ten i/o devices and provides 3 types of synchronous parallel interface It has two versions: 32 bit (33 MHz) ,64 bit (66 MHz) The data transfer rate for synchronous is 132 mbps and for asynchronous it is 528 mbps. The PCI driver can access hardware automatically or by programmer can assign address. The automatic detection and assignment of addresses of various devices simplifies the addition and removal of the system peripheral. PCI is designed to support variety of microprocessor best configuration including single and multi-processing system. PCI - X is revised to double the maximum clock speed to improve the data exchange transfer between processor and peripherals. The data exchange rate is 1.06 gbps. b) Draw labelled interfacing diagram of seven segment display with 89C51 micro 				
-	b)					
	Ans:	Note: Student may draw the interfacing in multiplexed mode with more than one display. Common anode/cathode configuration can be used. $ \begin{array}{c} & & & & \\ & &$	(4M for correct label diagram)			



	c)	State all logical operators used in 'C' and explain any one with example.			4M	
	Ans:		1		(Stating :	
		~	Not	P0=~P0;P0=0xff will give P0=0x00	¹ / ₂ M each,	
		^	XOR	$ACC ^ P1 = 0 \ge 02 ^ 0 \ge 73 = 0 \ge F1$	with	
			OR	$ACC P1 = 0 \ge 02 0 \ge F3 = 0 \ge F3$	example: 1	
		&	AND	ACC & P1 = $0 \times 02 \& 0 \times F3 = 0 \times 02$	M)	
		>	Right shift	P0=P0>>1; $P0=0x01$ will give 0x00;		
		<	Left shift	P0=P1<<1; $P0=0x01$ will give 0x02;		
-	d)	Draw inte	erfacing diag	gram of LED to port pin P2.4 of 89C51 write 'C' language and OFF LED after 20 ms delay	4M	
	Ans:	#include <r< th=""><th>eg51.h></th><th></th><th>(2M for</th></r<>	eg51.h>		(2M for	
		sbit led=P2	2^4; //make]	P2.4 as LED	Program	
		void delay	(void);		,2 M for	
		mid main	()		interfacing	
			0		with Port	
		l			pin is	
		led=1;			expected.)	
		delay();				
		ed=0; while(1):				
		$\{$				
		,				
		void delay	(void)			
			0 10			
		IMOD = 0	0x10;			
		TL1=0x00	C,):			
		TR1=1	,			
		while(TF1==0);				
		TR1=0;				
		TF1=0;				
		ĵ				
				OR		
<pre>#include<reg51.h> sbit led=P2^4; //make P2.4 as LED upid_delay(_upgignedint);</reg51.h></pre>				P2.4 as LED		
		voia delay	(unsigned in	u <i>)</i> ;		
		void main {	0			
		led=1;				



```
delay(20);
led=0;
while(1);
}
void delay (unsigned int itime)
{
unsigned intx,y;
for(x=0; x<itime; x++)
for (y=0; y<1275; y++);
}
                                             OR
Note : If student has written program to on-off LED continuously, marks can be given
#include<reg51.h>
sbit led=P2<sup>4</sup>; //make P2.4 as LED
void delay( unsigned int);
void main ()
{
While(1)
{
led=1;
delay(20);
led=0;
delay(20);
}
}
void delay (unsigned int itime)
{
unsigned intx,y;
for(x=0; x<itime; x++)
for (y=0; y<1275; y++);
}
```



