17659

15162

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions : (1) All Questions are *compulsory*.

(2) Illustrate your answer with neat sketches wherever necessary.

(3) Figures to the right indicate full marks.

(4) Assume suitable data, if necessary.

(5) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. Attempt any TEN of the following : **(10 × 2) = 20**

(a) Define the term 'Noise Margins'.

(b) Draw the block diagram of Mealy Machine.

(c) Define 'skew' w.r.t. sequential logic.

(d) State applications of finite state machines.

(e) Draw two input NOR Gate using CMOS technology.

(f) List different capacitances related to CMOS transistor.

(g) List different Data types used in VHDL.

(h) Give the syntax of signal used in VHDL.

(i) Write the syntax of CASE statement.

(j) List the different sequential statements used in VHDL.

(k) What do you mean by 'simulation' ?

(l) List the different softwares related to VHDL.

(m) State the advantages of PLD's.

(n) State any four features of XILINX.

P.T.O.

2. Attempt any FOUR of the following : **16**

(a) Distinguish asynchronous sequential circuit and synchronous sequential circuits.

(b) Explain estimation of channel resistance of CMOS.

(c) Draw CMOS AND Gate and write it with Truth Table. (2 input)

(d) State the various features of VHDL.

(e) Write VHDL code for half adder.

(f) List different levels of simulation and explain in brief.

3. Attempt any FOUR of the following : **16**

(a) Compare Mealy machine with Moore Machine.

(b) Explain fabrication using N-well process.

(c) Design $Z = \overline{XY + UV}$ using CMOS logic.

(d) Give the syntax of Entity and Architecture using in VHDL programming.

(e) Draw 3 : 8 decoder and write VHDL code for it.

(f) Explain event scheduling with suitable example.

4. Attempt any FOUR of the following : **16**

(a) Define the following terms :

(i) Meta stability

(ii) Set-up time

(iii) Hold time

(iv) Fan-out

(b) Explain Twin-tube process with suitable diagram.

(c) Explain various operators used in VHDL.

(d) Explain, how to write test bench for any VHDL code.

(e) Explain Event based and cycle based simulator.

(f) Explain sensitivity list and zero modelling.

5. Attempt any FOUR of the following : **16**

(a) Write various steps of well process.

(b) List different concurrent statements and explain any two.

(c) Draw full Adder using gates and write VHDL code for it.

(d) Write the various steps of synthesis and explain in short.

(e) Explain efficient coding styles.

(f) Draw design flow of ASIC and explain it.

6. Attempt any FOUR of the following : **16**

(a) Compare CMOS and BJT Technology.

(b) Explain the shift operations and logical operations.

(c) Write VHDL programme for 1 : 4 Demux using when-else statement.

(d) Draw FPGA configurable logic block diagram.

(e) Write various factors for selection of FPGA.

(f) Draw architecture of CPLD and explain in brief.