WINTER – 15 EXAMINATION

Model Answer

Subject Code: 17333 **Subject Name: DIGITAL TECHNIQUES**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may tryto assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Marks

1. A) Attempt any six: **12**

a) Define positive and negative logic digital system.

(Definition – 1 Mark each)

Ans:

Positive Logic system- Logic system in which the higher of two levels is represented by 1 and the lower level is represented by 0

Negative Logic system- Logic system in which the lower of two levels is represented by 1 and the higher level is represented by 0

b) Define:

i). Fan In
ii). Fan Out

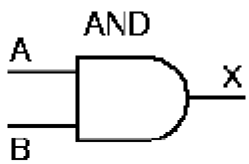
(1 Mark each)

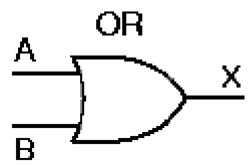
Ans:

Fan in-The number of inputs of a logic gate
Fan out- The Maximum number of similar logic gates which can be driven by a logic gate.

c) **Draw the symbol and truth label of AND and OR gate.**
(Correct symbol and Truth table - 1 Mark each)

Ans:





A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

d) **Give the name of universal gate. Why they called as universal gate?**
(Naming – 1 Mark, Reason – 1 Marks) (Any relevant definition – 1 Mark)

Ans:

NAND and NOR gates are called as Universal gates.

NAND and NOR gates can perform all basic logical operations, hence they are called as universal gates

e) Perform the following conversion

i. $(25.45)_D = (?)_B$

ii. $(11011010)_B = (?)_H$

(1 Mark each for correct conversion)

Ans:

e)- Perform following conversion.

i) $(25.45)_D = (?)_B$

2	25	1
2	12	0
2	6	0
2	3	1
	1	1

$(25)_{10} \approx (11001)_2$

$(0.45)_D = (?)_B$

$0.45 \times 2 = 0.9 \rightarrow 0$

$0.9 \times 2 = 1.8 \rightarrow 1$

$0.8 \times 2 = 1.6 \rightarrow 1$

$0.6 \times 2 = 1.2 \rightarrow 1$

$0.2 \times 2 = 0.4 \rightarrow 0$

$(0.45)_{10} \approx (01110)_2$

i.e $(25.45)_D \approx (11001.01110)_B$

1. A) e)

ii) $(11011010)_B \approx (?)_H$

Make a group of four from right to left and add zero's to MSB (if needed) and write equival. Hex. No.

$(\underbrace{1101}_{D}\,\underbrace{1010}_{A}) = (DA)_H$

f) **List any four Boolean laws.**

(Any Four Boolean Law - 2 Marks)

Ans:

$A \cdot B = B \cdot A$ $A + B = B + A$
$A \cdot (B \cdot C) = A \cdot B \cdot C$ $A + (B + C) = A + B + C$
$A \cdot A = A$ $A + A = A$
$\overline{\overline{A}} = A$
$A \cdot \overline{A} = 0$ $A + \overline{A} = 1$
$A \cdot 1 = A$ $A \cdot 0 = 0$
$A + 1 = 1$ $A + 0 = A$
$\overline{AB} = \overline{A} + \overline{B}$ $\overline{A + B} = \overline{A}\,\overline{B}$
$A \cdot (B + C) = (A \cdot B) + (A \cdot C)$ $A + (BC) = (A + B) \cdot (A + C)$
$A \cdot (A + B) = A$ $A + (AB) = A$
$A \cdot (\overline{A} + B) = AB$ $A + (\overline{A}B) = A + B$

g) Give the function of IC74147 & IC74181.

(Correct function - 1 Mark each)

Ans:

1. **IC 74147-** Decimal to BCD Encoder.
   Encoder IC 74147 converts Decimal number to BCD.

2. **IC 74181-** Arithmetic Logic Unit (ALU)

   ALU IC 74181 performs various Arithmetic and Logical operations.

h) List any two advantages of R-2R ladder DAC.

(Any two advantages - 1 Mark each)

Ans:

1. It is slightly complicated in construction.
2. It requires resistors of only two values, hence easy to build circuit.
3. It can be easily expanded o handle more number of bits by adding more sections of the R-2R resistors.
4. It requires two resistors per bit
5. Due to small resisters can be fabricated monolithically with high accuracy and stability

B) Attempt any two: 8

a) Compare TTL and CMOS (any four points).

(Any Four points - 1 Mark each)

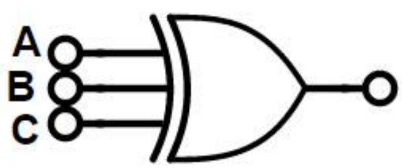
Ans:

Parameter	TTL	CMOS
Propagation Delay	10ns	70ns
Noise Margin	Moderate	High
Fan Out	10	20 -50
Figure of Merit	100pJ	0.7pJ
Power dissipation per gate	10mW	0.1mW
Speed power product	100pJ	0.7pJ
Circuit complexity	Complex	Moderately Complex
Basic Gates	NAND	NAND /NOR
Applications	Lab and demonstration equipments	Portable equipment as they consume less power

b) Draw truth table of 3 inputs EX-OR gate. Draw its symbol. Also give its output expression.

(Symbol – 1 Mark, Expression - 1 Mark, truth table - 2 Marks)

Ans:



Inputs			outputs
W	X	Y	Q = A⊕B⊕C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Output Expression: Q = A⊕B⊕C

c) Perform $(9)_{10} - (4)_{10}$ using 1's and 2's complement method.

(2 Marks each)

Ans:

c) $(9)_{10} = (1001)_2$

$(4)_{10} = (0100)_2$

i) 1's complement of $(0100)_2 = (1011)_2$

By Adding $(9)_{10}$ & 1's complement of $(4)_{10}$

$(9)_{10}$ 1001

1's complement of $(4)_{10}$ + 1011

[1] 0100 result

Carry is generated, hence answer is positive & in its true form.

By adding final carry to the result,

1001
+ 1011
[1] 0100
+ 1
0101

Ans = 0101

ii) Using 2's complement method.

2's complement of $(4)_{10}$ ⇒ 1011 1's complement of $(4)_{10}$

+ 1
1100

By Adding $(9)_{10}$ & 2's complement of $(4)_{10}$

$(9)_{10}$ 1001

2's complement of $(4)_{10}$ 1100

Discard carry → [1] 0101

Ans = 0101

Final carry indicates that the answer is positive & in its true form ∴ $(9)_{10} - (4)_{10} = (5)_{10}$

2. Attempt any four: 16

a) Define De-Morgan's theorem and prove it.

(Theorem – 1 Mark each, Proof/Verification - 1 Mark each)

Ans:

Theorem1: It state that the, complement of a sum is equal to product of complements

Verification of the second theorem :

A	B	$\overline{A+B}$	$\bar{A}$	$\bar{B}$	$\bar{A}\cdot\bar{B}$
0	0	**1**	1	1	**1**
0	1	**0**	1	0	**0**
1	0	**0**	0	1	**0**
1	1	**0**	0	0	**0**

LHS $\overline{A+B} = \bar{A}\cdot\bar{B}$ RHS

Truth table to verify De-Morgan's second theorem

Theorem2: It states that, the complement of a product is equal to sum of the complements.

A	B	$\overline{AB}$	$\bar{A}$	$\bar{B}$	$\bar{A}+\bar{B}$
0	0	**1**	1	1	**1**
0	1	**1**	1	0	**1**
1	0	**1**	0	1	**1**
1	1	**0**	0	0	**0**

LHS $\overline{AB} = \bar{A}+\bar{B}$ RHS

: Verification of the theorem $\overline{AB} = \bar{A}+\bar{B}$

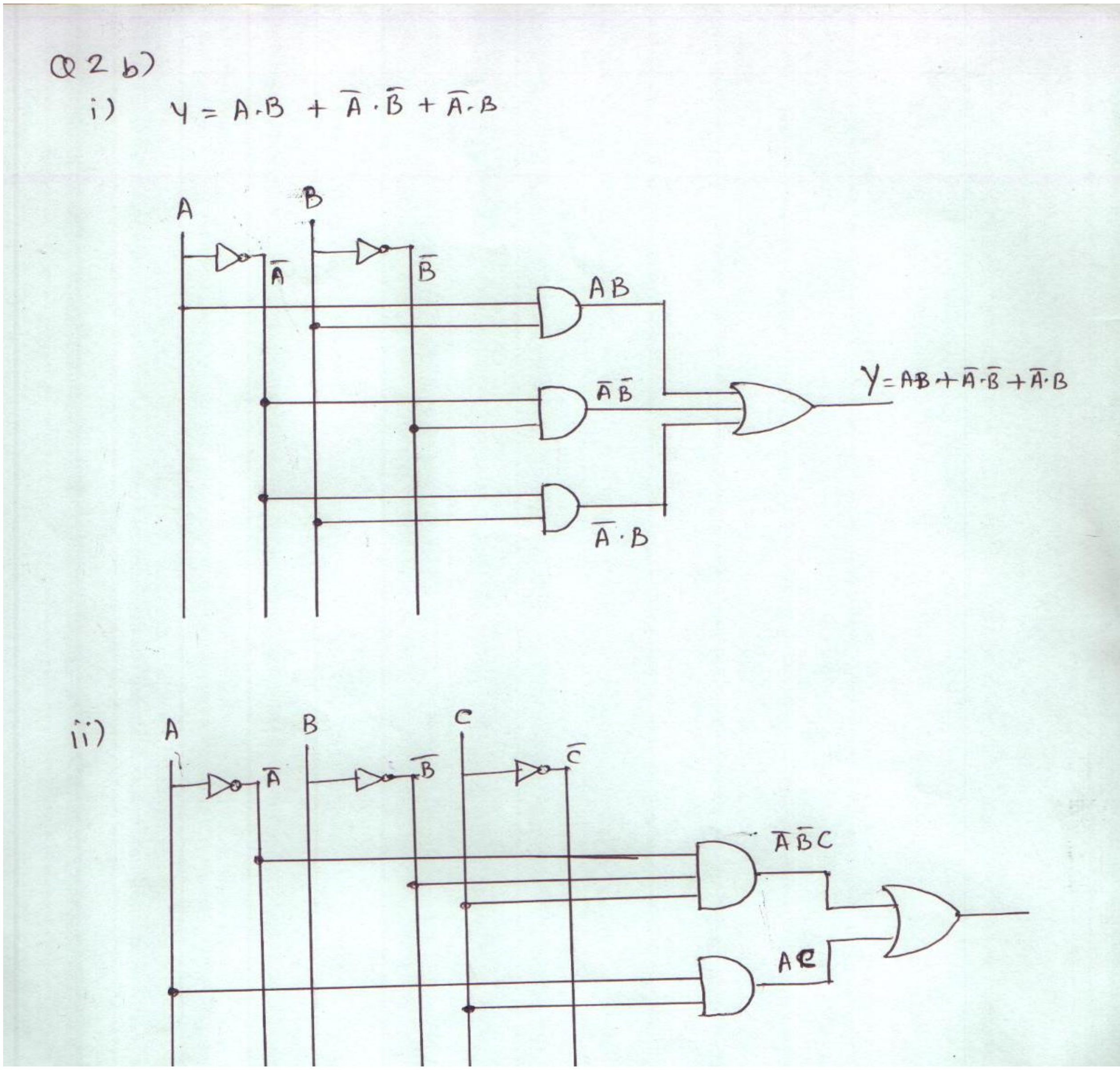
b) **Implement the following logical expression using gates**

i). $Y=AB+\bar{A}.\bar{B}+\bar{A}.B$

ii). $Y=\bar{A}\bar{B}C+AC.$

(2 Marks for each Correct Implementation)

Ans:



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c) Add $(83)_{10}$ and $(34)_{10}$ in BCD.

(1 Mark for BCD, 1 Mark for Addition, 1 Mark, Valid conversion, 1 Mark for Correct answer)

Ans:

$$
\begin{array}{lr}
(83)_{10} & (1000\ \ 0011)_{BCD} \\
+\ (34)_{10} & +\ (0011\ \ 0100)_{BCD} \\
\hline
 & 1011\ \ 0111
\end{array}
$$

1011 → Invalid BCD; 0111 → Valid BCD

Add 6 to invalid BCD

$$
\begin{array}{r}
1011\ \ 0111 \\
+\ 0110\ \ 0000 \\
\hline
0001\ \ 0001\ \ 0111 \\
1 \quad\ \ 1 \quad\ \ 7
\end{array}
$$

$(83)_{10} + (34)_{10} = (117)_{10}$

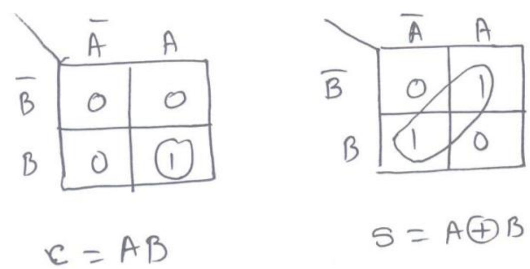
d) Design Half adder circuit using K-Map technique.

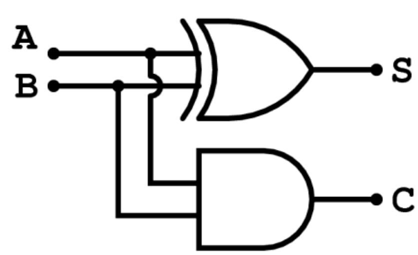
(Truth Table – 2 Marks, k-map- 1 Mark, basic gates – 1 Mark)

Ans:

Truth Table

A	B	C	S
o	o	o	o
o	1	o	1
1	o	o	1
1	1	1	o

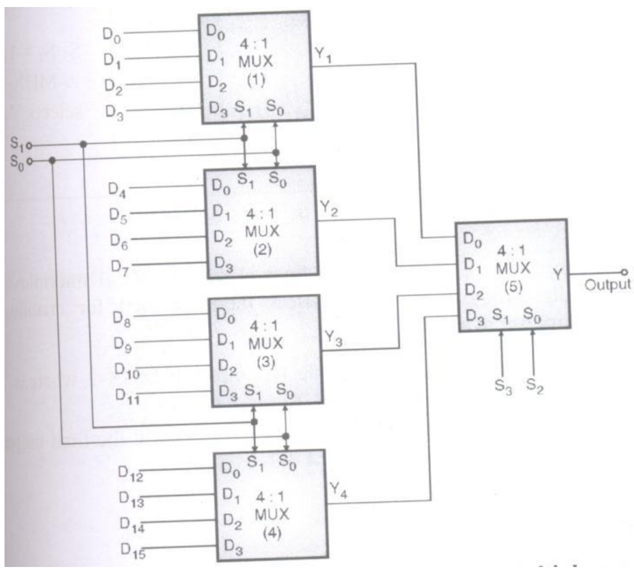




e) Draw 16:1 MUX using 4:1 MUX

(Correct implementation - 4 Marks)

Ans:



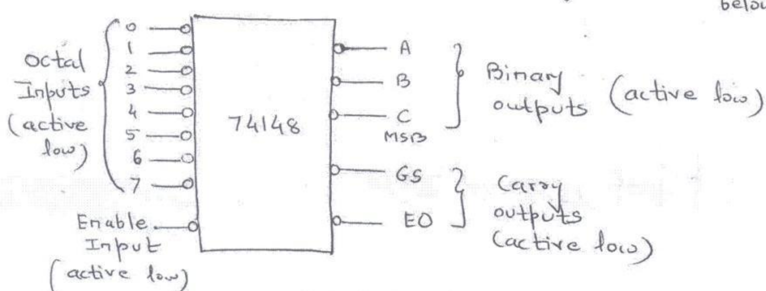
f) **Draw the block diagram and truth table of Octal to Binary encoder IC 74148.**

(Block diagram - 2 Marks, Truth table - 2 Marks)

Ans:

Block Diagram of octal to Binary Encoder

Priority encoder IC 74148 is used for the above conversion. Its block diagram is given below



Truth Table

Inputs									Outputs				
EI	0	1	2	3	4	5	6	7	C	B	A	GS	EO
1	x	x	x	x	x	x	x	x	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	x	0	1	1	1	1	1	1	1	1	0	0	1
0	x	x	0	1	1	1	1	1	1	0	1	0	1
0	x	x	x	0	1	1	1	1	1	0	0	0	1
0	x	x	x	x	0	1	1	1	0	1	1	0	1
0	x	x	x	x	x	0	1	1	0	1	0	0	1
0	x	x	x	x	x	x	0	1	0	0	1	0	1
0	x	x	x	x	x	x	x	0	0	0	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0

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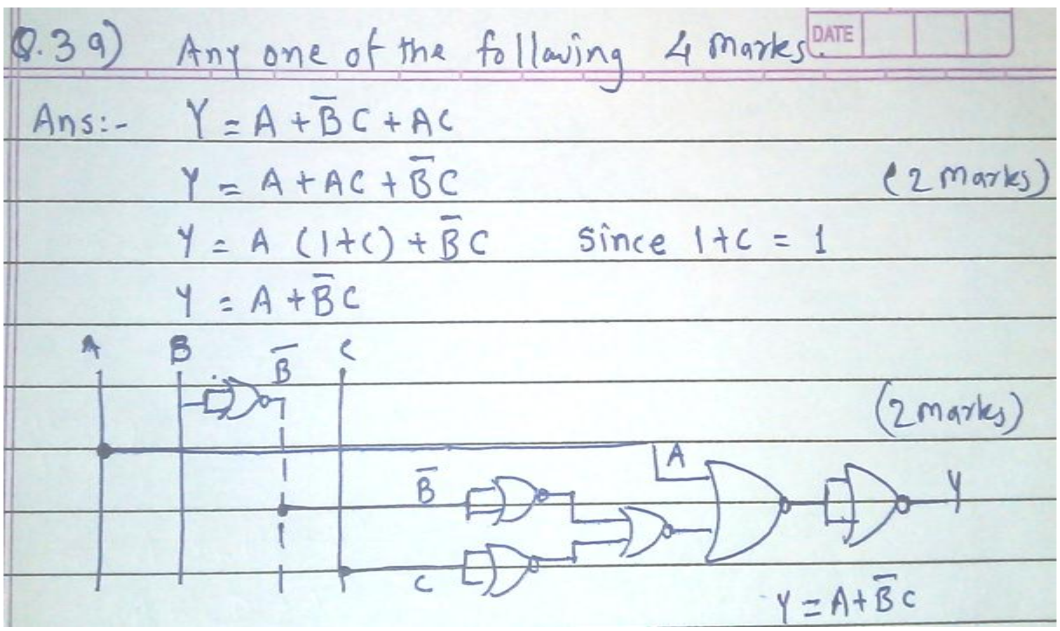
3. Attempt any four : **16**

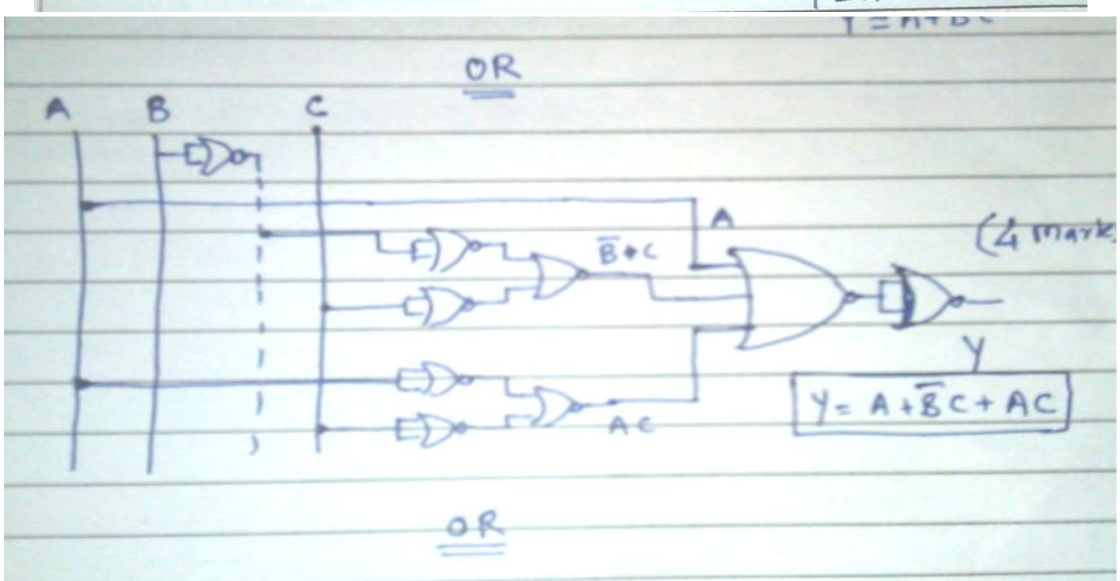
a) Implement the Boolean expression using NOR gate only

$Y=A+\overline{B}C+AC$

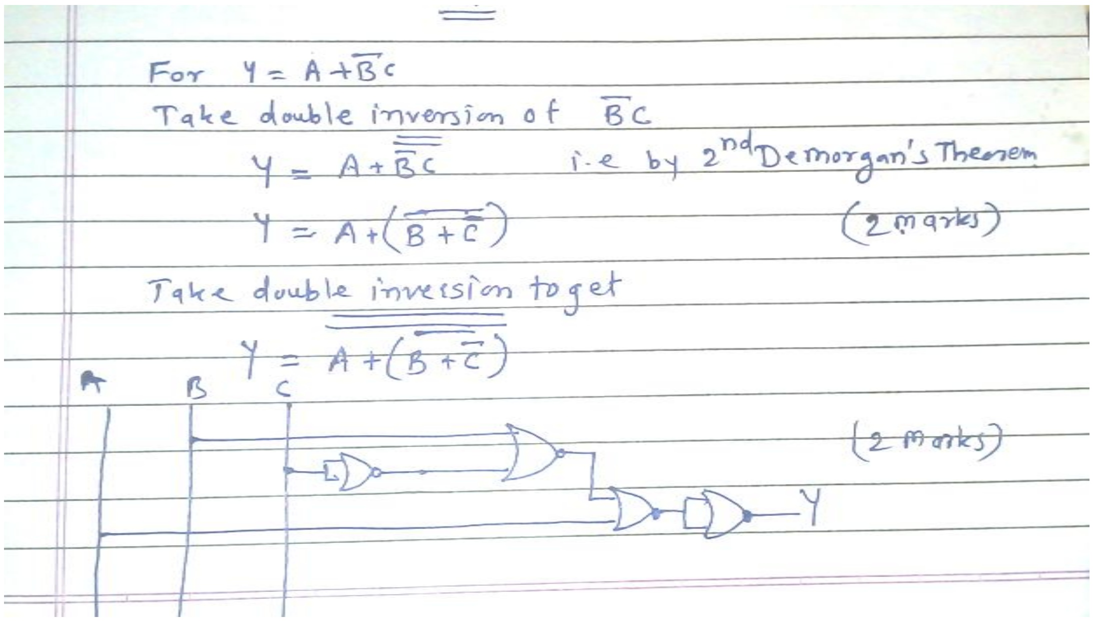
(Proper correct labeled diagram using NOR gate. - 4 Marks)

Ans:





OR



For $Y = A + \bar{B}C$

Take double inversion of $\bar{B}C$

$Y = A + \overline{\overline{\bar{B}C}}$ i.e by 2nd De Morgan's Theorem

$Y = A + (\overline{B + \bar{C}})$ (2 marks)

Take double inversion to get

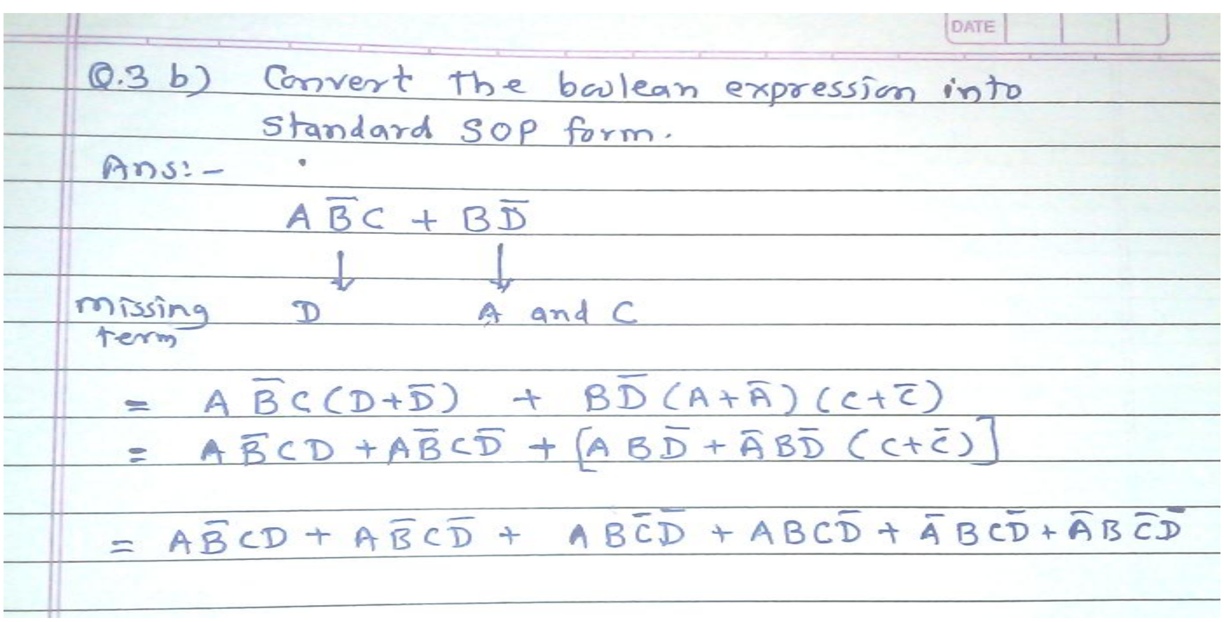
$Y = \overline{\overline{A + (\overline{B + \bar{C}})}}$

b) **Convert the Boolean expression into standard SOP form**

$Y=A\bar{B}C+B\bar{D}$

(Properly converted expression - 4 Marks, can give Marks to steps)

Ans:



Q.3 b) Convert the boolean expression into standard SOP form.

Ans:-

$A\bar{B}C + B\bar{D}$

missing term: D (for $A\bar{B}C$); A and C (for $B\bar{D}$)

$= A\bar{B}C(D+\bar{D}) + B\bar{D}(A+\bar{A})(C+\bar{C})$

$= A\bar{B}CD + A\bar{B}C\bar{D} + [AB\bar{D} + \bar{A}B\bar{D}(C+\bar{C})]$

$= A\bar{B}CD + A\bar{B}C\bar{D} + AB\bar{C}\bar{D} + ABC\bar{D} + \bar{A}BC\bar{D} + \bar{A}B\bar{C}\bar{D}$

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c) In the following circuit as shown in fig.No.1. What will be the output 'X'?

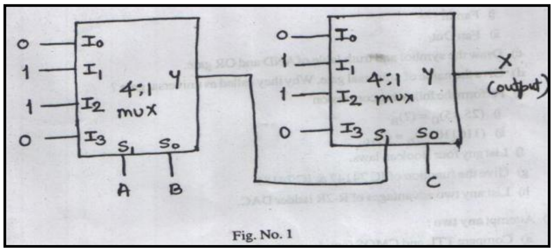

Fig. No. 1

(Proper correct labeled diagram using NOR gate - 4 Marks)

Ans

A	B	Y1
0	0	0
0	1	1
1	0	1
1	1	0

Y1=S1	C=0	Xi
0	0	0 (I_0)
1	0	1 (I_2)
1	0	1 (I_2)
0	0	0 (I_0)

Y1=S1	C=1	Xi
0	1	1 (I_1)
1	1	0 (I_3)
1	1	0 (I_3)
0	1	1 (I_1)

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d) Minimize the following expression using K-Map

$Y=\sum m\ (1, 5, 6, 7, 11, 12, 13, 15)$

(Stepwise solution - 4 Marks)

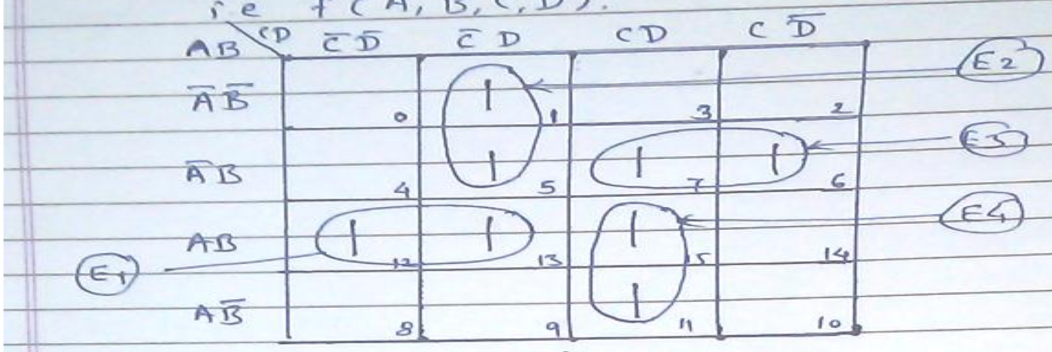
[Note: Probable grouping of 1's can be considered]**

Ans:

Q.3 d) Minimize the following expression using k-map

$Y = \Sigma m(1, 5, 6, 7, 11, 12, 13, 15)$

Ans:- There are four variables in K-map.
i.e f(A, B, C, D).

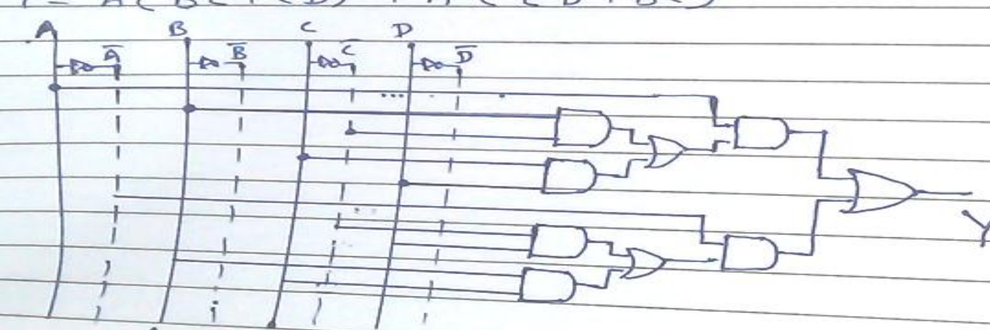


$E_1 = AB\bar{C}$
$E_2 = \bar{A}\bar{C}D$
$E_3 = \bar{A}BC$
$E_4 = ACD$

$Y = AB\bar{C} + ACD + \bar{A}\bar{C}D + \bar{A}BC$

OR

$Y = A(B\bar{C} + CD) + \bar{A}(\bar{C}D + BC)$



(Logic diagram is optional)

e) Give any four differences between combinational and sequential logical circuit.

(Any 4 points can be considered - 1 Mark for each difference point)

Ans:

	Combinational Circuit	**Sequential Circuit**
1	Here the output at any instant of time depends upon the inputs present at that instant	Here the output at any instant of time depends upon the inputs present as well as past input/outputs.
2	Memory element is not required	Memory element is required to provide previous input ,,outputs
3	i.e. Adder, Subtractor, Multiplexer, De-multiplexer, Code converters	i.e. Flip-flop, Shift registers, counters
4	As there is no memory element previous state of input does not have any effect on present state of the circuit.	Memory element is included in feedback path.
5	The sequence in which the inputs are being applied has no effect on the output of combinational circuit.	The sequence in which the inputs are being applied should be maintained as output depends on previous state of circuit
6	Clock input is not required	Click input required

f) How many flip-flops are required to build a shift register to store following number

i) Decimal 28 **ii) Binary 6 bits**

iii) Octal 17 **iv)Hexadecimal A.**

(Basic Diagram of biometric authentication – 2 Marks, explanation of process - 2 Marks)

Ans:

Situation	**Situation**	**No. of flip-flops**
Decimal 28	i.e. 2^5 = 32 states	5
Binary 6 bit	i.e. 2^6 = 64 states	6
Octal 17	i.e. 8^2 =64 states	4
Hexadecimal A	i.e. 16^1 = 16 states	4

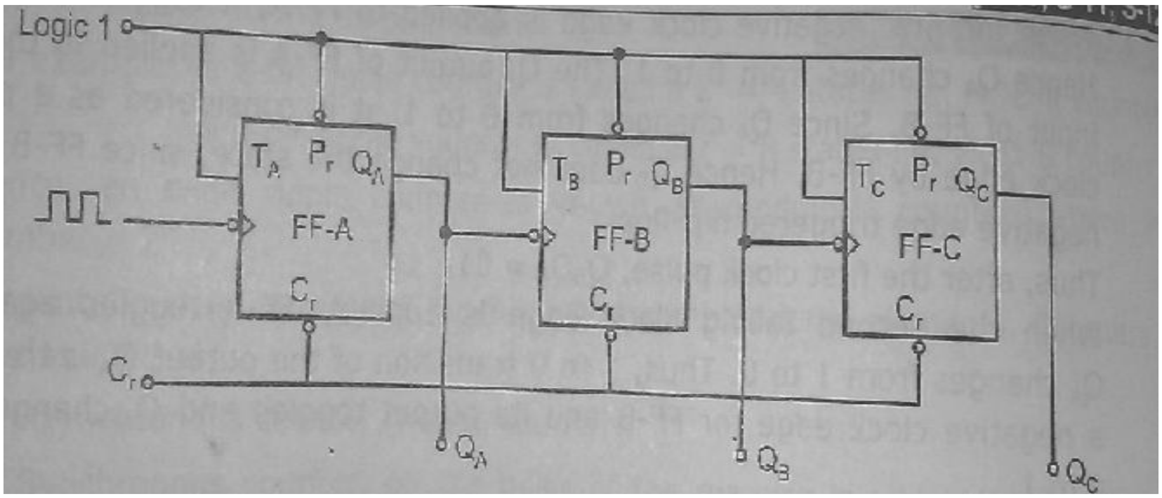
4. Attempt any four: 16

a) Design a 3 bit asynchronous counter. Draw its truth table.

(Explanation, Diagram - 3 Marks, Truth table - 1 Mark)

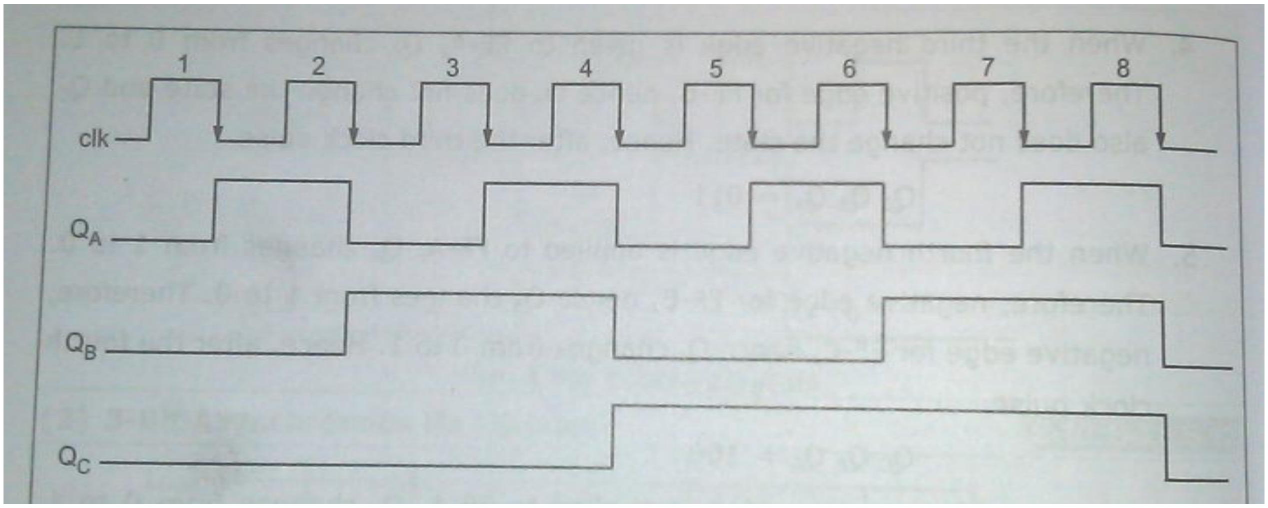
Ans:

Following figure shows 3-bit asynchronous counter. It uses 3 flip-flops, i.e. it has 2^3 = 8 states The clock pulse is applied to flip-flop A and Q_A output of flip-flop A acts as a clock input for Flip-flop B and Q_B output of flip-flop B acts as a clock input for Flip-flop C.



TRUTH TABLE FOR 3-BIT ASYNCHRONOUS COUNTER				
DECIMAL COUNT	**QC**	**QB**	**QA**	**STATE**
0	0	0	0	1
1	0	0	1	2
2	0	1	0	3
3	0	1	1	4
4	1	0	0	5
5	1	0	0	6
6	1	1	0	7
7	1	1	1	8
0	0	0	0	1

Timing diagram is OPTIONAL



b) Explain any four specification of DAC.

(1 Mark for each detail specification (Any Four) in short)

Ans:

1. **<u>Resolution:</u>** of a **DAC** can be defined in two different ways:

a. Resolution is the number of different analog output voltage values that can be provided by a DAe. For an n-bit DAe

Resolution= 2

b. Resolution is defined as the ratio of change in analog output voltage resulting from a change of 1 LsB at the digital input

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

V_{FS} is defined as the full scale analog output voltage i.e the analog output voltage when all the digital input with all digits 1.

2. **<u>Accuracy:</u>**

- Accuracy indicates how close the analog output voltage is to its theoretical value. It indicates the deviation of actual output from the theoretical value. Accuracy depends on the accuracy of the resistors used in the ladder, and the precision of the reference voltage used. Accuracy is always specified in terms of percentage of the full scale output that means maximum output voltage

Example: - If the full scale output is 15 V and accuracy is ± 0.1 percent then the

Maximum error is 0.001 x 15 = 0.015V or 15 mV.

3. **Linearity:**

- The relation between the digital input and analog output should be linear.
- However practically it is not so due to the error in the values of resistors used for the resistive networks.

4. **Temperature sensitivity:**

- The analog output voltage of D to A converter should not change due to changes in temperature.
- But practically the output is a function of temperature. It is so because the resistance values and OPAMP parameters change with changes in temperature.

5. **Settling time**:

- The time required to settle the analog output within the final value, after the change in digital input is called as settling time.
- The settling time should be as short as possible.

6. **Long term drift**

- Long term drift are mainly due to resistor and semiconductor aging and can affect all the characteristics.
- Characteristics mainly affected are linearity, speed etc.

7. **Supply rejection**

- Supply rejection indicates the ability of DAe to maintain scale, linearity and other important characteristics when the supply voltage is varied.
- supply rejection is usually specified as percentage of full scale change at or near full scale voltage at 25^{o}e

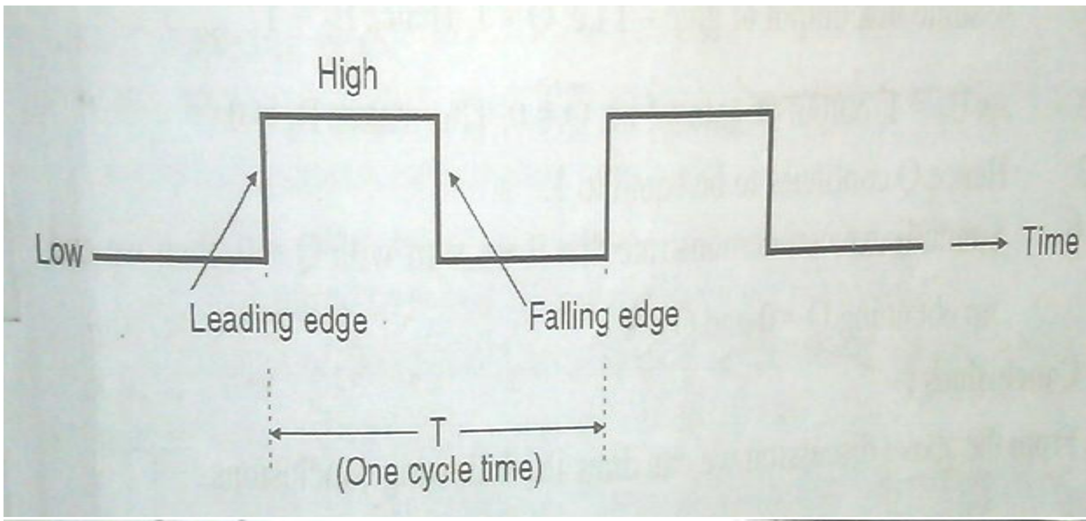
8. **Speed:**

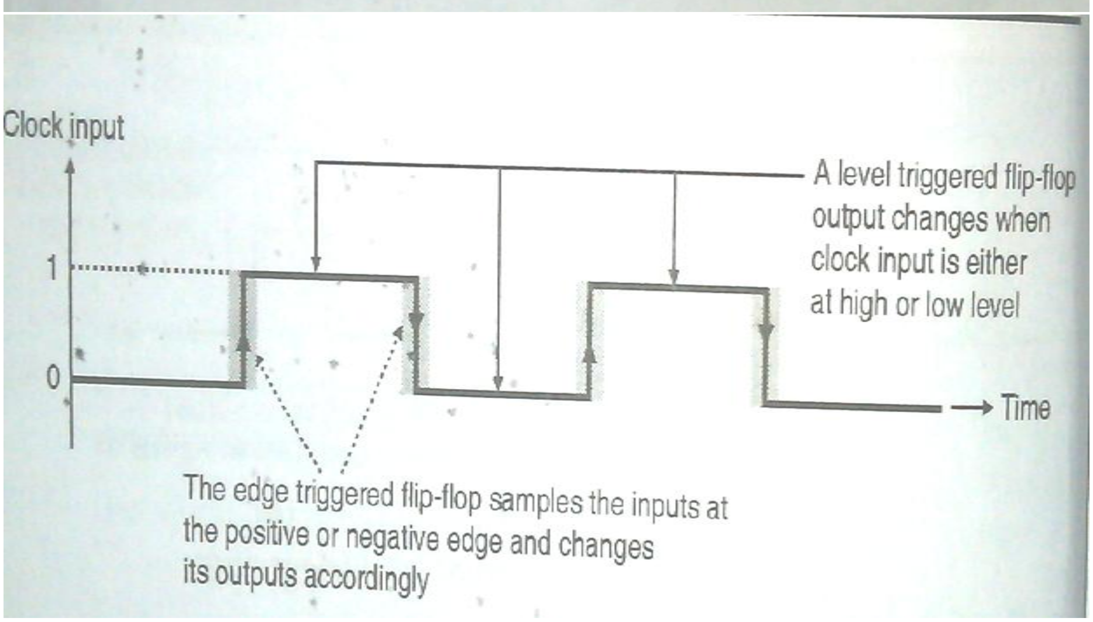
- It is defined as the time needed to perform a conversion from digital to analog.
- It is also defined as the number of conversions that can be performed per second.
- The speed of DAC should be as high as possible

c) Draw clock signal. Explain various triggering methods.

(Clock signal - 1 Mark, each triggering method 1 and ½ Mark each)

Ans:





There are following types of triggering:

Level Triggering:

In this the result of digital circuit responding to the level of clock input.

There are two sub types:

- High level triggering
- Low Level Triggering

Edge Triggering:

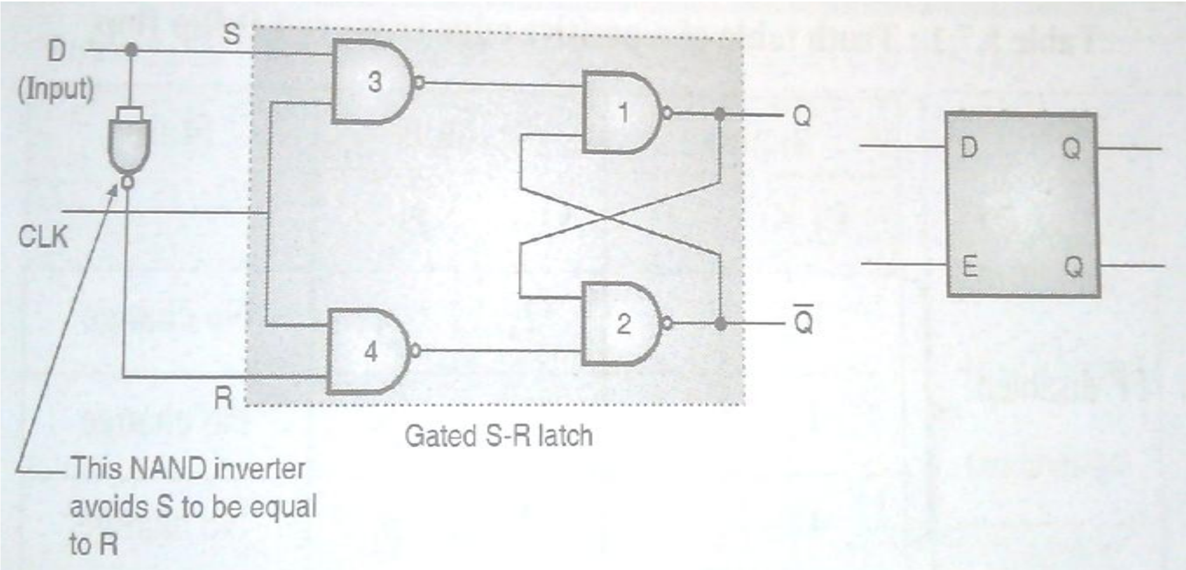
The result of digital circuit is responding to the negative or positive edge.

- Positive edge triggering **(Rising)**
- Negative edge triggering **(Falling)**

d) Draw and explain D flip-flop using SR flip-flop. Also draw truth table

(Explanation - 2 Marks, Diagram – 2 Marks)

Ans:



(a) Circuit diagram (b) Logic symbol

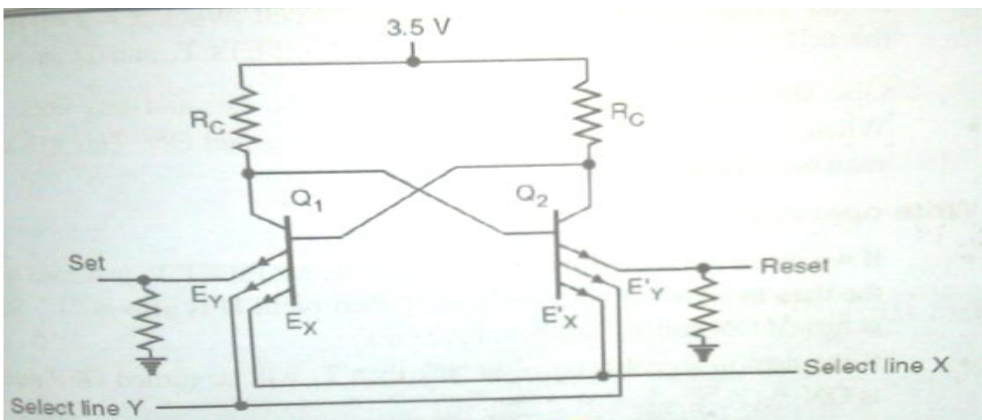
Due to Inverter S and R will always be the complements of each other hence S=R=0 or S=R=1 conditions never appear.

D	S	R	Qn+1	Qn+1
0	0	1	0	1
1	1	0	1	0

e) Draw a neat labeled diagram of static RAM Cell and explain it.

(Explanation – 2 Marks, Diagram - 2 Marks)

Ans:



Each bit in an SRAM is stored on four transistors (M1, M2, M3, M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional *access* transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 8T, 10T, or more transistors per bit.

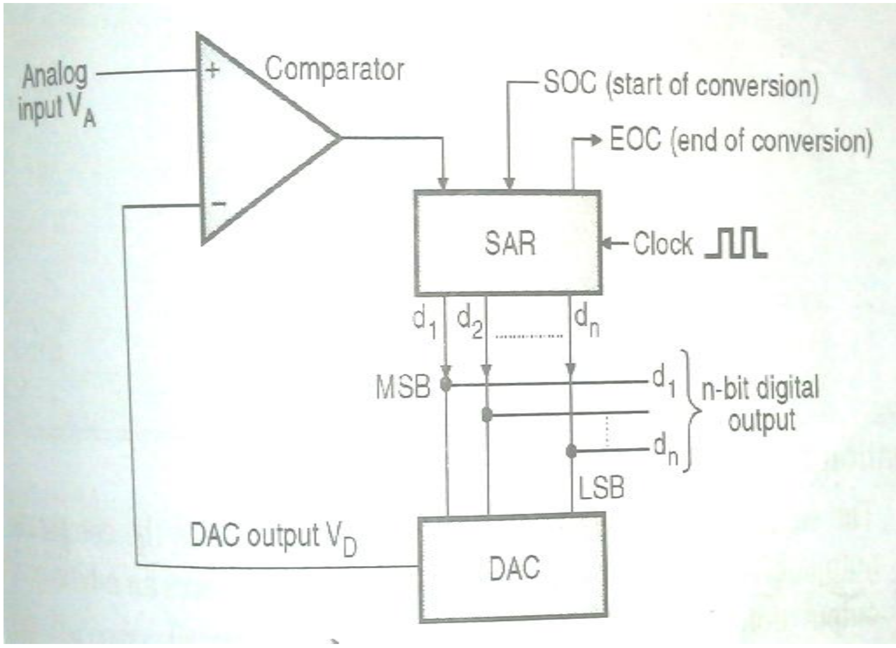
Access to the cell is enabled by the word line (WLin figure) which controls the two *access* transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL. They are used to transfer data for both read and write operations.

During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. The size of an SRAM with *m* address lines and *n* data lines is 2^mwords, or 2^mx *n* bits.

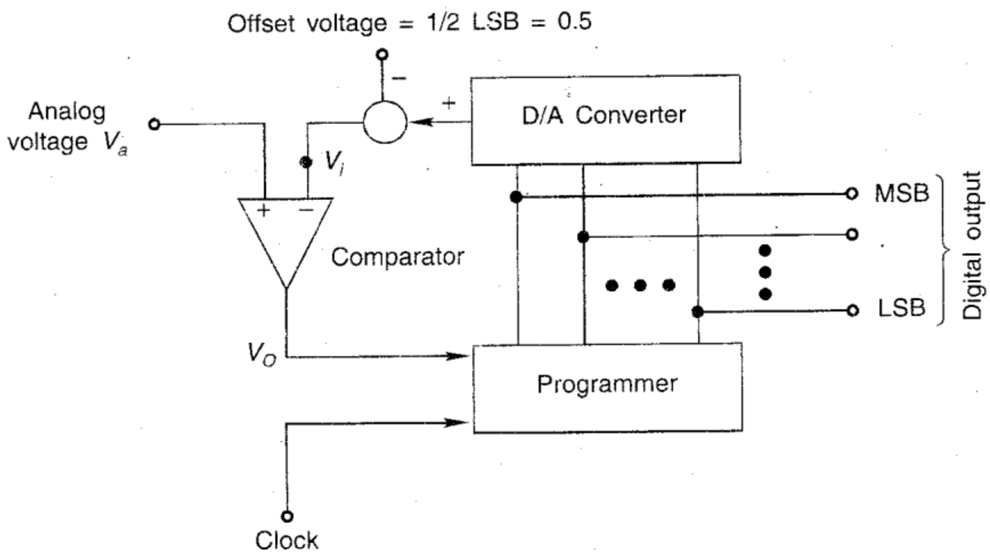
f) **Draw the circuit diagram of successive approximation ADC and explain it.**

(Explanation – 2 Marks, Diagram - 2 Marks)

Ans:



OR



Working: The comparator serves the function of the scale, the output of which is used for setting / resetting the bits at the output of the programmer. This output is converted into equivalent analog voltage from which offset is subtracted and then applied to the inverting input terminal of the comparator. The outputs of the programmer will change only when the clock pulse is present.

To start the conversion, the programmer sets the MSB to 1 and all other bits to O. This is converted into analog voltage by the DAC and the comparator compares it with the analog input voltage. If the analog input voltage Va >= Vi, the output voltage of the comparator is HIGH, which sets the next bit also. On the other hand if Va <= Vi, Then the output of the comparator is LOW which resets the MSB and sets the next bit. Thus a 1 is tried in each bit of DAC until the binary equivalent of analog input voltage is obtained.

5. Attempt any four: **16**

a) Perform $(22)_{10}$-$(54)_{10}$ in BCD using 10's complement method.

Ans:

Let A=22 and B=54

Step 1: Find 10's compliment of B

Subtract 54 from 99 and then add 1

```
  9 9
- 5 4
  4 5
+   1
  4 6
```

So 10's(B)= 46 **(1 mark)**

Step 2: Add A and 10's of (B)

```
 2 2          0 0 1 0       0 0 1 0
+4 6    +     0 1 0 0       0 1 1 1
           0  0 1 1 0       1 0 0 0
              Valid         Valid
Carry
```

(1 mark)

Step 3: As carry generated is Zero, The answer is in negative form and not in its true form so we have to take its 10's Compliment

```
      1 0 0 1         1 0 0 1
      0 1 1 0         1 0 0 0
     0 0 1 1          0 0 0 1
+                           1
      0 0 1 1         0 0 1 0

     -  3               2
```

(2 mark)

So, $(22)_{10} – (54)_{10} = (-32)_{10}$

b) **List different types of flip-flop. Draw the diagram of master Slave JK flip -flop.**

(Types - 2 Marks, Diagram - 2 Marks)

Ans:

Types of Flip-Flops

- RS flip-flop
- JK flip-flop
- D flip-flop
- T flip-flop

Circuit Diagram

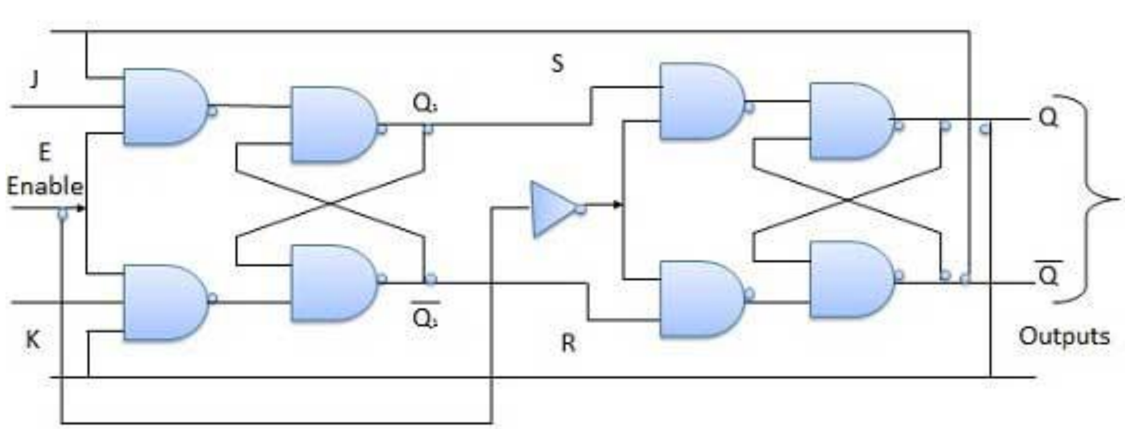


Fig: Master Slave JK Flip-Flop

c) **Simplify $Y = (\overline{\overline{AB}+\bar{A}+AB})$.**

(Simplification - 4 Marks)

Ans:

5) c) Simplify $Y = (\overline{\overline{AB}+\bar{A}+AB})$

Ans:- $Y = (\overline{\overline{AB}+\bar{A}+AB})$ — ①

Apply De'morgans theorem to eq^n ①

$Y = (\overline{\overline{AB}}) \cdot (\bar{\bar{A}}) \cdot (\overline{AB}) \quad (\because \overline{A+B} = \bar{A} \cdot \bar{B})$

$Y = (AB) \cdot (A) \cdot (\overline{AB}) \quad (\because \bar{\bar{A}} = A)$

$Y = (AAB) \cdot (\overline{AB}) \quad$ (multiply)

$Y = (AB) \cdot (\overline{AB})$ — ②

Let $AB = C$

② ⇒ $Y = C \cdot \bar{C}$

$Y = 0 \quad (\because C \cdot \bar{C} = 0)$

$\therefore Y = (\overline{\overline{AB}+\bar{A}+AB}) = 0$

OR

OR

$Y = AB \cdot (\overline{AB})$ — ②

Apply De-morgans theorem

$Y = AB \cdot (\bar{A}+\bar{B})$

$Y = A\bar{A}B + AB\bar{B}$

$= 0 \cdot B + A \cdot 0 \quad (\because A\bar{A} = 0,\ B\bar{B} = 0)$

$= 0 + 0$

$= 0$

d) Draw the diagram of serial in parallel out (SIPO) shift register. Also draw timing diagram.

(Diagram -2 Marks, Timing Diagram - 2 Marks)

Ans:

A serial-in/parallel-out shift register is similar to the serial-in/ serial-out shift register in that it shifts data into internal storage elements and shifts data out at the serial-out, data-out, pin. It is different in that it makes all the internal stages available as outputs. Therefore, a serial-in/parallel-out shift register converts data from serial format to parallel format. If four data bits are shifted in by four clock pulses via a single wire at data-in, below, the data becomes available simultaneously on the four outputs Q_A to Q_D after the fourth clock pulse.

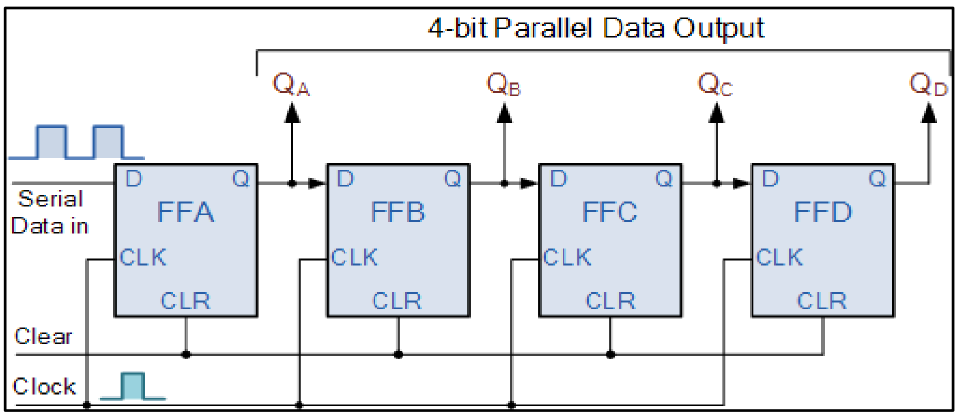


Figure: Serial in parallel out

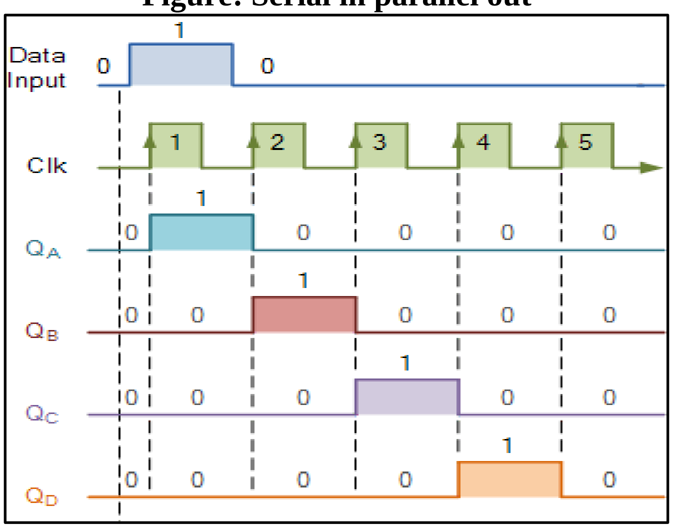


Figure: Timing Diagram

e) Draw the block diagram of ALV 74181 and explain each block.

(Diagram - 2 Marks, Blocks Explanation – 2 Marks)

Ans:

Arithmetic Logic Unit (ALU):

1. The heart of every computer is an Arithmetic Logic Unit (ALU). This is the part of the computer which performs arithmetic as well as logical operations 74181 is a 24-pin IC in dual in line (DIP) package.
2. A (A0 — A3) and B (B0 — B3) are the two 4 bit variables. It can perform a total of 16 arithmetic operations which includes addition, subtraction, compare and double operations. It provides many logic operations such as AND, OR, NOR, NAND, EX-OR, compare, etc. on the two four bit variables.
3. 74181 is a high speed 4 bit parallel ALU. It is controlled by four function select inputs (S0-S3). These lines can select 16 different operations for one mode (arithmetic) and 16 another operations for the other mode (logic).
4. M is the mode control input. It decides the mode of operation to be either arithmetic or logic. Mode M= 0 For arithmetic operations. M = 1 For logic operations.
5. G and P outputs are used when a number of 74181 circuits are to be used in cascade along with 74182 the look ahead carry generator circuit to make the arithmetic operations faster
6. A=B it is Equality output
7. F (F0-F3) 4-bit binary Data Output
8. $\overline{C}_n$: carry input (active-low)
9. $\overline{C}_{n+4}$ carry output (active-low)

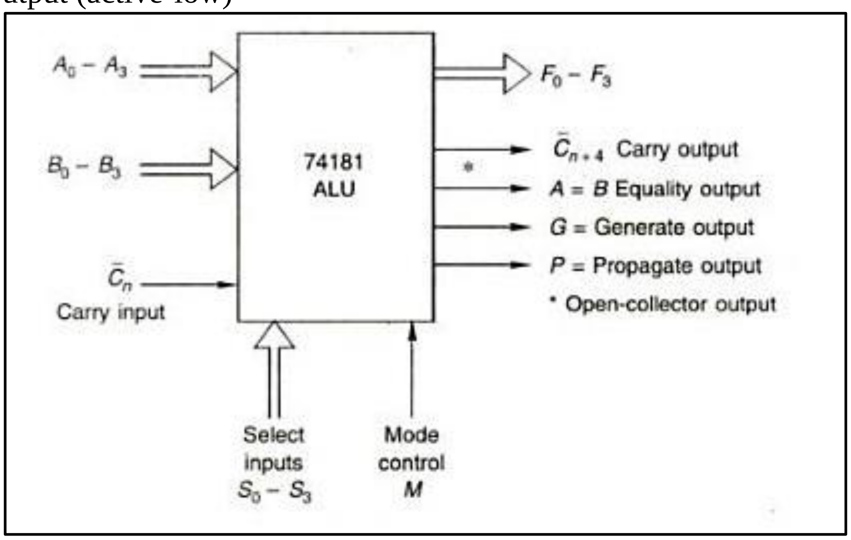


Figure: 74181 ALU

f) **Draw the pin diagram of universal shift register IC 7495.List any two applications of shift register.**

(Pin diagram - 2 Marks, Applications - 2 Marks (any 2))

Ans:

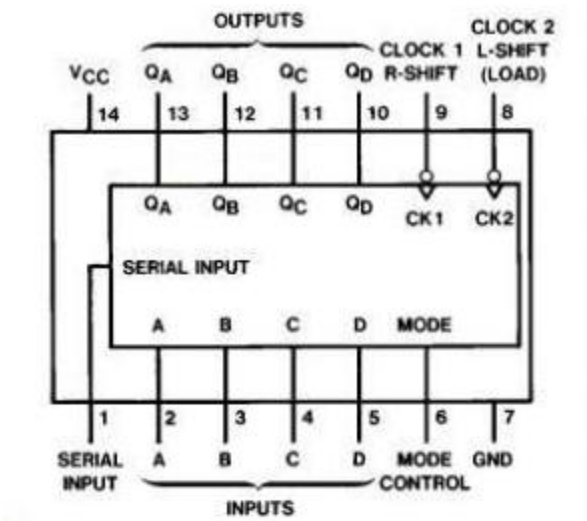


Figure: Pin diagram of IC 7495

Application of Shift Registers

1. Delay line
2. Serial to parallel converter
3. Parallel to serial converter
4. Ring counter
5. Twisted Ring counter
6. Sequence generator

6. Attempt any two: 16

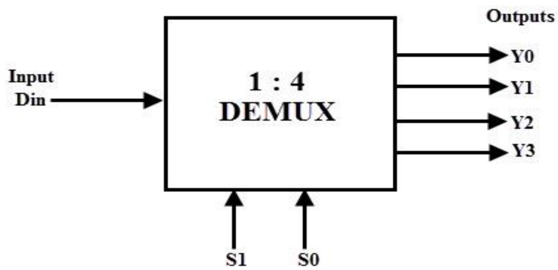
a) i) Draw block diagram and truth table of 1:4 demultiplexer.

(Diagram - 1 Mark, Truth table – 1 Mark)

Ans:

1-to-4 Demultiplexer has a single input (D), two selection lines (S1 and S0) and four outputs (Y0 to Y3). The input data goes to any one of the four outputs at a given time for a particular combination of select lines.

The block diagram of 1:4 DEMUX is shown below.



The truth table of this type of demultiplexer is given below.

From the truth table it is clear that, when S1=0 and S0= 0, the data input is connected to output Y0 and when S1= 0 and s0=1, then the data input is connected to output Y1.

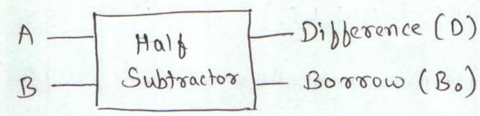
Similarly, other outputs are connected to the input for other two combinations of select lines.

Data Input	Select Inputs		Outputs			
D	S_1	S_0	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

ii) Design half-substractor using NAND gate only.

(Diagram – 1 Mark, Truth table – 1 Mark, Equations – 2Marks – Implementation – 2 Marks)

Ans:



Truth Table

A	B	Diff (D)	Borrow(B_o)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

From the above truth table, we can compute the following equation

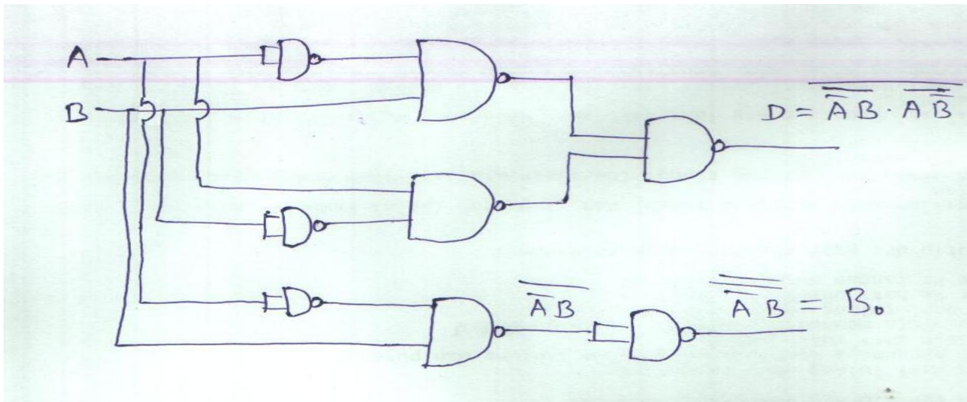
$$\text{Difference } (D) = A \oplus B$$
$$= \bar{A}B + A\bar{B} \quad \text{— (1)}$$
$$\text{Borrow } (B_o) = \bar{A}B \quad \text{— (2)}$$

$$(1) \Rightarrow D = \bar{A}B + A\bar{B}$$

Taking Double Compliment

$$= \overline{\overline{\bar{A}B + A\bar{B}}}$$
$$= \overline{\overline{\bar{A}B} \cdot \overline{A\bar{B}}} \quad (\because \overline{A+B} = \bar{A}\cdot\bar{B}) \text{ — (3)}$$

$$(2) \Rightarrow B_o = \bar{A}B$$
$$= \overline{\overline{\bar{A}B}} \quad \text{— (4)}$$

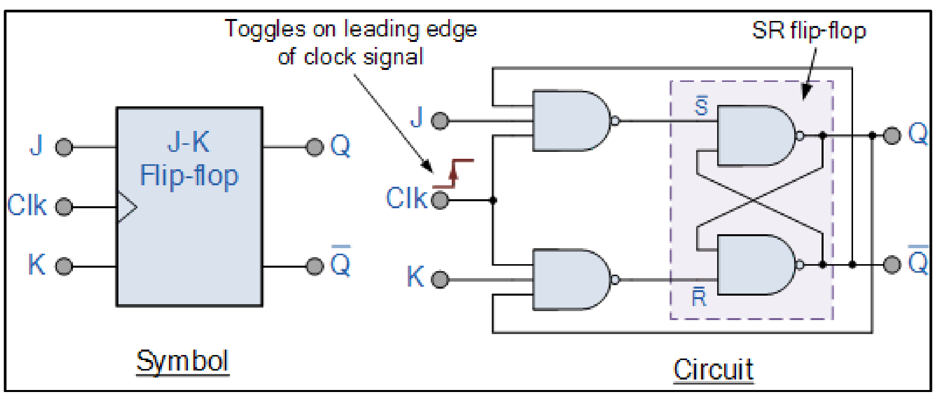


b) i) Draw symbol and truth table of JK flip flop.

(Symbol - 1 Mark, Truth Table - 1 Mark)
(Circuit diagram is Optional)

Ans:

JK FF:



Truth Table

Inputs			Outputs		
J	K	C	Q	Q'	Comments
0	0	↑	Q	Q'	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	Q'	Q	Toggle

OR

Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

OR

	Input		Output		Description
	J	K	Q	Q	
Same as for the SR Latch	0	0	0	0	Memory no change
	0	0	0	1	
	0	1	1	0	Reset Q » 0
	0	1	0	1	
	1	0	0	1	Set Q » 1
	1	0	1	0	
Toggle action	1	1	0	1	Toggle
	1	1	1	0	

ii) Define modulus of counter.

(Definition - 2 Marks)

Ans:

Modulus Counter (MOD-N Counter)

Modulus of a counter is the no. of different states through which the counter progress during its operation. It indicates the no. of states in the counter; pulses to be counted are applied to counter. The circuit comes back to its starting state after counting N pluses in the case of modulus N counter.

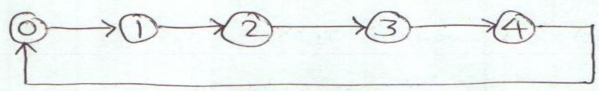
The 2-bit ripple counter is called as MOD-4 counter and 3-bit ripple counter is called as MOD-8 counter. So in general, an n-bit ripple counter is called as modulo-N counter. Where, MOD number = 2^n.

iii) Design a MOD-5 ripple counter.

(State Diagram – 1 Mark, Truth table – 1 Mark, Equation – 1 Mark, Logical Representation – 1 Mark)

Ans:

1) State Diagram



2) Truth table for Reset Logic

Flip Flop output				Output (Y) of Reset Logic
State	Q_C	Q_B	Q_A	
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0

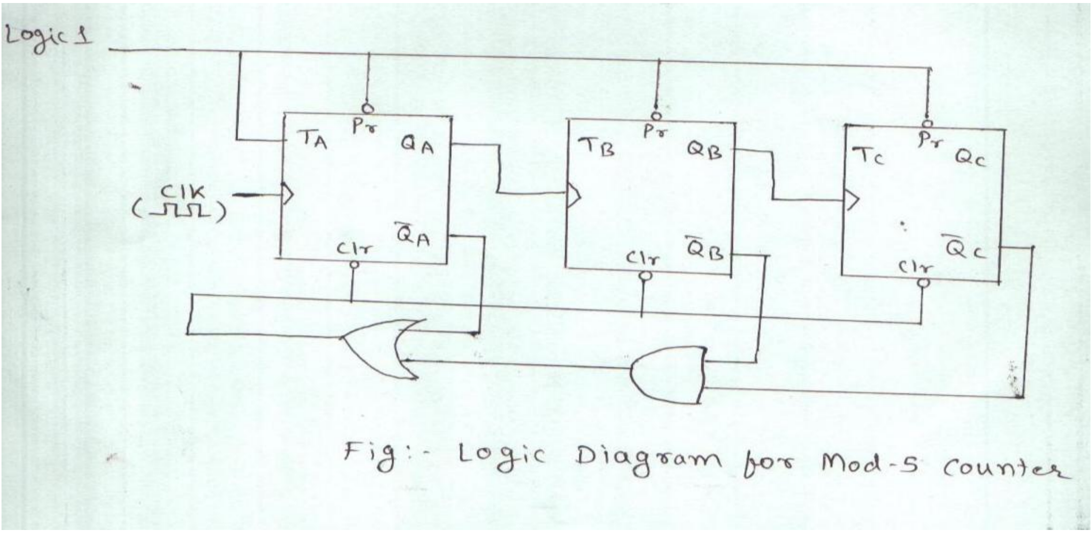
3) K-Map Simplification

Q_A \ Q_BQ_C	$\overline{Q}_B\overline{Q}_C$	$\overline{Q}_BQ_C$	Q_BQ_C	$Q_B\overline{Q}_C$
$\overline{Q}_A$	1	1	1	1
Q_A	1			

$\overline{Q}_A$

$\overline{Q}_B\overline{Q}_C$

$$Y = \overline{Q}_A + \overline{Q}_B\overline{Q}_C$$



c) i) List two advantages and two disadvantages of ADC

(Any two advantages - 2 Marks, Any two disadvantages - 2 Marks)

Ans:

Advantages

1. High Resolution
2. High Stability (averages and filters out noise)
3. Low Power
4. High accuracy
5. Capable of high speed
6. Good tradeoff between speed and cost

Disadvantages

1. Cycle-Latency
2. Low Speed
3. Cost is high
4. Complex in design
5. Long conversion time

ii) Draw circuit diagram of weighted register DAC & explain its function.

(Circuit diagram - 2 Marks, Function - 2 Marks)
[Note: Expressions are Optional]**

Ans:

Following figure shows the circuit diagram of weighted resistor DAC. This DAC circuit uses weighted values of resistor like 2R, 4R, 6R, 8R and so on depending on the digital inputs available therefore such type of network is known as weighted resistor DAC.

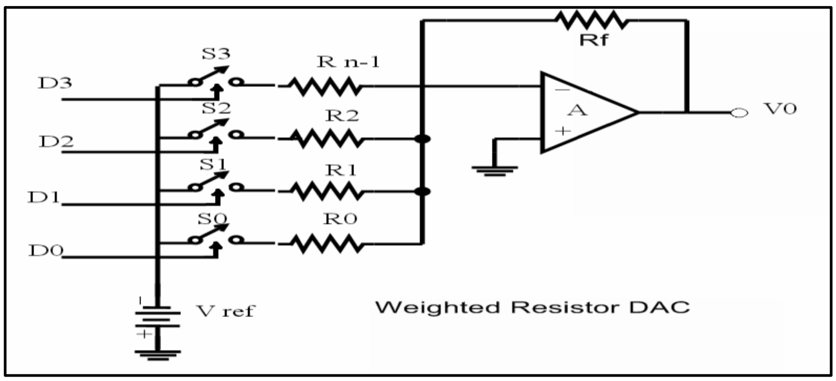


Figure: Weighted Resistor DAC

OR

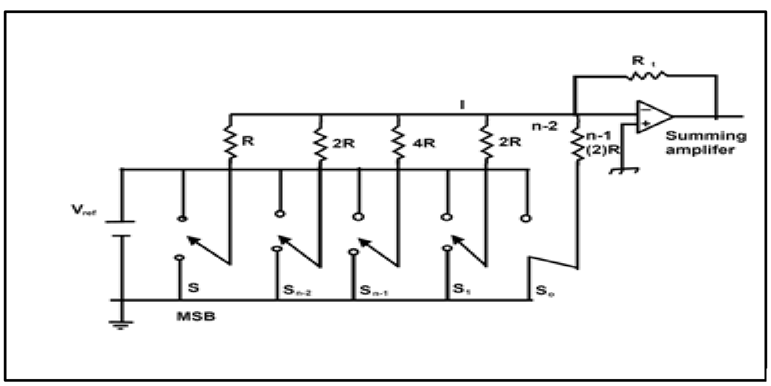


Figure: Weighted Resistor DAC

This circuit consist of a transistor switch (shown by the upward arrow) which turns on the switch when digital input is ‘1’ and if digital input becomes ‘0’ it will opens the switch. When transistor switch gets closed a current flows through the weighted resistor due to reference voltage as shown in circuit diagram. When all such currents from different weighted resistors get added at summing point (which is also known as virtual ground) of operational amplifier it will produce proportional voltage as its output.

For a 4 bit DAC the output V0 is given as follows:

$$V_o = -V_{ref}\left(S_3 \times \frac{Rf}{R3} + S_2 \times \frac{Rf}{R2} + S_1 \times \frac{Rf}{R1} + S_0 \times \frac{Rf}{R0}\right)$$

Where S3, S2, S1 and S0 represents the status of the switches i.e. on or off (1 or 0).If resistors are in binary weights i.e. R3=2Rf, R2=4Rf, R1=8Rf and R0=16Rf, the above equation can be written as,

$$V_o = -V_{ref}\left(\frac{S3}{2^1} + \frac{S2}{2^2} + \frac{S1}{2^3} + \frac{S0}{2^4}\right)$$

From the above equation we can say that for a 4 bit DAC, 4 switches produces 16 different combinations of output and hence produces 16 different output voltage. in general n-bit DAC produces 2^n different discrete analog voltages.