Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q.1.

a) Attempt any six of the following: (12M)

i. Compare the digital system with analog system on four points. (Any four points 1M each)

Sr no	Parameter	Analog systems	Digital systems
1.	Type of signals processed	Analog signals	Digital signals
2.	Type of display	Analog meters	Digital displays using LED and LCD
3.	Accuracy	Less	More
4.	Design complexity	Difficult to design	Easier to design
5.	Memory	No memory	They have Memory
6.	Storage of information	Not Possible	Possible
7.	Effect of noise	More	Less
8.	Versatility	Less	More
9.	Distortion	More	Less
10.	Effect of temperature and ageing on performance	More	Less
11.	Communication between systems	Not easy	Easy
12.	Examples	Filters, amplifiers, power supplies, signal generators	Counters, resisters, microprocessors, Computers

ii. Define:
(1 M each)

1. Propagation delay
It is the time gap between the change of input and corresponding change in output of gate or FF.

2. Noise margin
A quantitative measure of noise margin is called as noise margin.

iii. Draw the symbol and truth table of :
(1 M each)

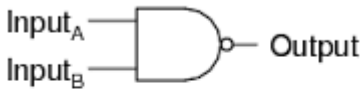
1. EX-OR gate

$$Y = A \oplus B = \bar{A}B + A\bar{B} \ldots LOGICAL\ EXPRESSION$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

2. NAND gate

NAND gate



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

iv. State the meaning of universal gate. Name the universal gates.
(1m each)
Meaning: Universal gate is the one tat can be used for implementing any logic expression and any basic gate.
Names of Universal gates: NAND gate, NOR gate

v. Write the binary addition rules. (2M)

Rule	A		B		Sum	carry
1	0	+	0	=	0	0
2	0	+	1	=	1	0
3	1	+	0	=	1	0
4	1	+	1	=	0	1

vi. Define Duality theorem and give example.
(Theorem 1M, example 1M)

Theorem: Starting with a boolean relation, another boolean relation can be derived by

1. Changing each OR sign to an AND sign
2. Changing each AND sign to an OR sign
3. Complementing any 0 or 1 appearing in the expression

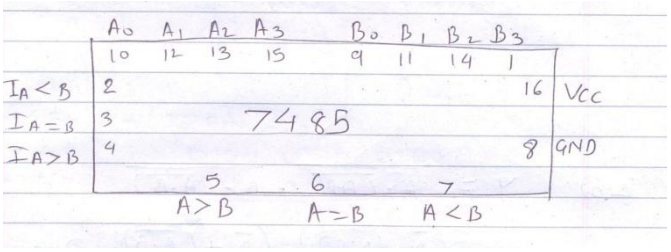
Example:

A.0 = 0

The dual relation is

A = 1 = 1

vii. Draw the logic diagram of IC 7485.
(2M)



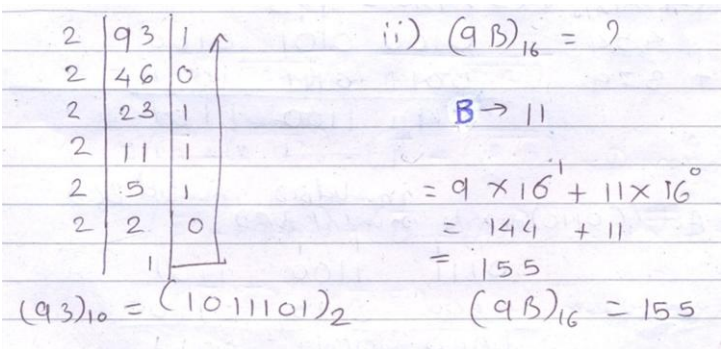
viii. Compare R-2R and weighted resistor DAC on four points.
(1M each point)

Weighted Resistor Type	Binary (R-2R) Ladder Type
1. It is simple in construction	1. It is slightly complicated in construction.
2. It requires more than two resistor values.	2. It requires resistors of only two values.
3. It is not easy to extend for more number of bits.	3. It can be easily expanded to handle more number of bits by adding the resistors.
4. It requires only one resistor per bit	4. It requires two resistors per bit

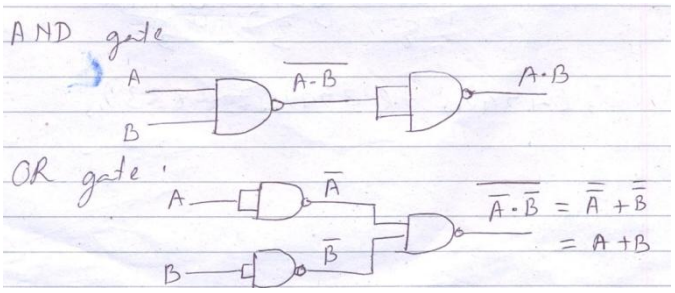
b) Attempt any two of the following: (8M)

i. Convert the following:
(2M each)

1. **$(93)_{10}=(?)_2$**
2. **$(9B)_{16}=(?)_{10}$**



ii. Construct the AND and OR gate using NAND gate. Write necessary outputs of gates. (2M each)



iii. Perform the BCD arithmetic:
(2M each)

1. **$(264)_{10}+(668)_2$**

2 marks each
264 0010 0110 0100 1 mark
+668 0110 0110 1000
1000 1100 1100
Invalid BCD, invalid BCD
Add $(0110)_{BCD}$ to invalid BCD: 1000 1100 1100 1 mark
+ 0000 0110 0110
1001 0011 0010
9 3 2
$\therefore (264)_{10}+(668)_{10}=(932)_{10}$

2. **$(454)_{10}+(379)_{10}$**

$(454)_{10}+(379)_{10}=$
454 0100 0101 0100
+379 0011 0111 1001
0111 1100 1101
invalid BCD, invalid BCD
Add $(0110)_{BCD}$ to invalid BCD
0111 1100 1101
+ 0000 0110 0110
1000 0011 0011
8 3 3
$\therefore (454)_{10}+(379)_{10}=(833)_{10}$

Q.2. **Attempt any four of the following:**

a) State De-Morgan's theorems and prove for two inputs.
(Theorem 1M each, Proof/Verification 1M each)

Theorem 1: $\overline{A+B} = \bar{A}.\bar{B}$

The theorem state that the, complement of a sum is equal to product of complements

Verification of the second theorem :

A	B	$\overline{A+B}$	$\bar{A}$	$\bar{B}$	$\bar{A}\cdot\bar{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

LHS $\overline{A+B} = \bar{A}\cdot\bar{B}$ RHS

Truth table to verify De-Morgan's second theorem

Theorem 2: $\overline{A.B} = \bar{A} + \bar{B}$

This theorem states that, the complement of a product is equal to addition of the complements.

A	B	$\overline{AB}$	$\bar{A}$	$\bar{B}$	$\bar{A}+\bar{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

LHS $\overline{AB} = \bar{A} + \bar{B}$ RHS

: Verification of the theorem $\overline{AB} = \bar{A} + \bar{B}$

b) Reduce the following logic expression using Boolean laws and D-Morgan's Theorems.
(4 M- 1M each step)

$$Y = \overline{A.\overline{(A.B)}}.\overline{B.\overline{(A.B)}}$$

$$= (\bar{A} + \overline{(A.B)}).(\bar{B} + \overline{(A.B)}) \ldots\ldots\ldots \text{Demorgan's theorem}$$

$$= (\bar{A} + (A.B)).(\bar{B} + (A.B)) \ldots . \bar{\bar{X}} = X$$

$$= (\bar{A}.\bar{B}) + (A.B) \ldots\ldots x + yz = (x+y)(x+z)$$

$$= A \odot B$$

c) Perform 2's complement subtraction:
$(59)_{10}$-$(62)_{10}$
(Finding binary representation -1M, Finding 2's compliment-1M, Addition-1M, Interpretation of Result-1M)

$(59)_{10} \rightleftharpoons (111011)_2$

2	59	1
2	29	1
2	14	0
2	7	1
2	3	1
	1	1

$(62)_{10} \rightleftharpoons (111110)_2$

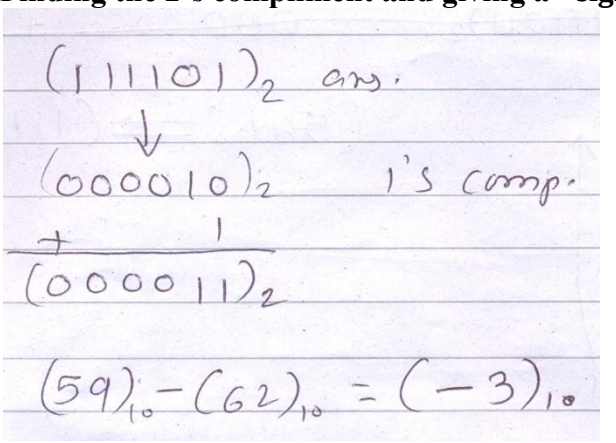
2	62	0
2	31	1
2	15	1
2	7	1
2	3	1
	1	1

1's complement of $(111110)_2$=$(000001)_2$
2's compliment=

```
0  0  0  0  0  1
+              1
-----------------
   (000010)2
```

```
         1
   1  1  1  0  1  1
  +0  0  0  0  1  0
-------------------
0 | 1 | 1 | 1 | 1 | 0 | 1 |
```

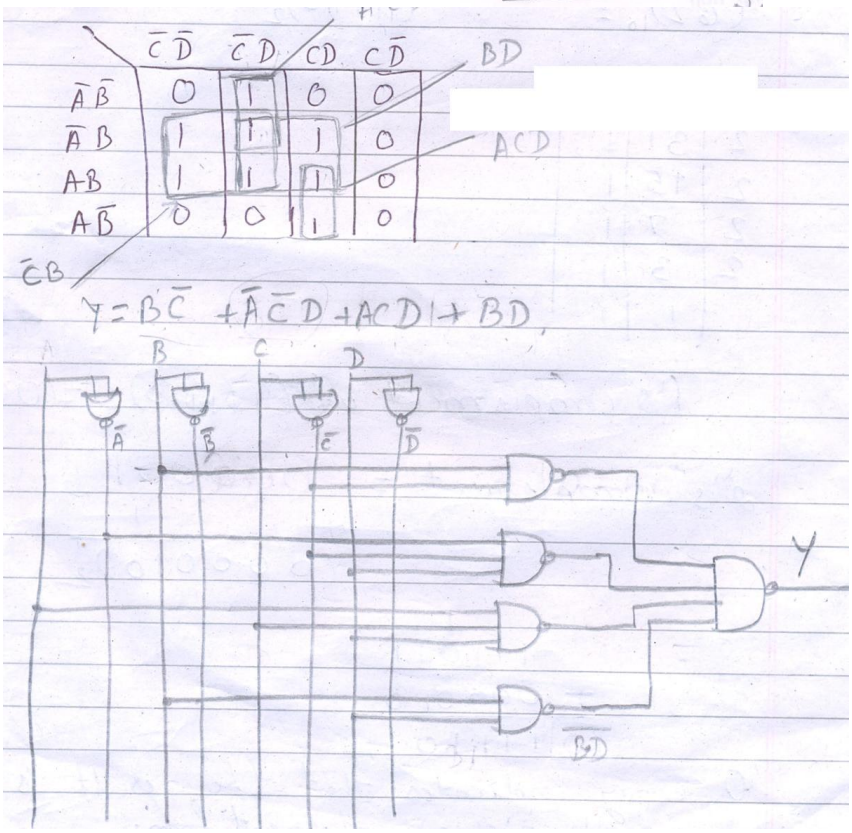
'0' carry indicates that the result is negative & in its 2's compliment form.
Finding the 2's compliment and giving a - sign



d) For the given K-map in Figure No. 1, write minimized SOP expression and for the same draw NAND-NAND l0gic circuit.
(Formation of groups 1M, Minimized SOP expression-1M, logic circuit-2M)

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$A\bar{B}$	0	1	0	0
$\bar{A}B$	1	1	1	0
AB	1	1	1	0
$A\bar{B}$	0	0	1	0

Fig. No. 1

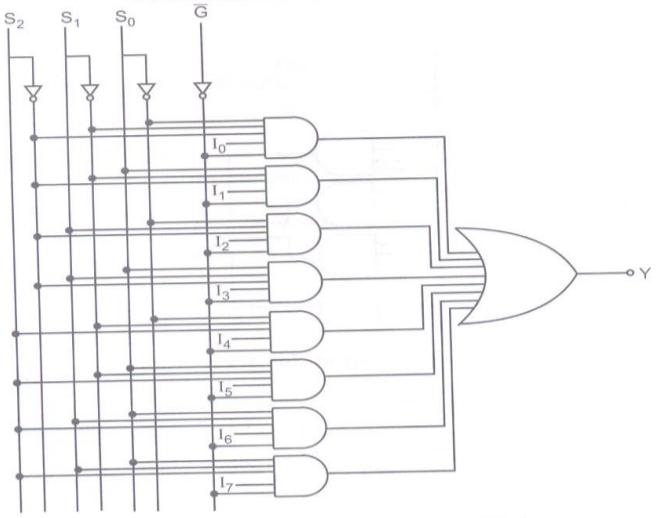


e) Draw 8:1 multiplexer using basic logic gates.
(Boolean Expression optional, Diagram 4M)

The Boolean expression for output

$$Y = \bar{S}_2\bar{S}_1\bar{S}_0I_0 + \bar{S}_2\bar{S}_1S_0I_1 + \bar{S}_2S_1\bar{S}_0I_2 + \bar{S}_2S_1S_0I_3 + S_2\bar{S}_1\bar{S}_0I_4 + S_2\bar{S}_1S_0I_5 + \bar{S}_2\bar{S}_1S_0I_6 + S_2S_1S_0I_7$$

The logic diagram for 8:1 multiplexer is shown in Fig. 3.45.



Logic diagram of 8:1 multiplexer

f) Construct full adder using basic logic gates and K-Map technique.
(Truth Table 1M, K maps 1M, Expressions for sum and carry-1m, Logic circuit 1M)

Truth Table

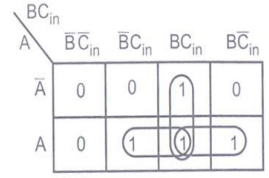
Inputs			Outputs	
A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

K-map for sum:

A \ BC_{in}	$\bar{B}\bar{C}_{in}$	$\bar{B}C_{in}$	BC_{in}	$B\bar{C}_{in}$
$\bar{A}$	0	(1)	0	(1)
A	(1)	0	(1)	0

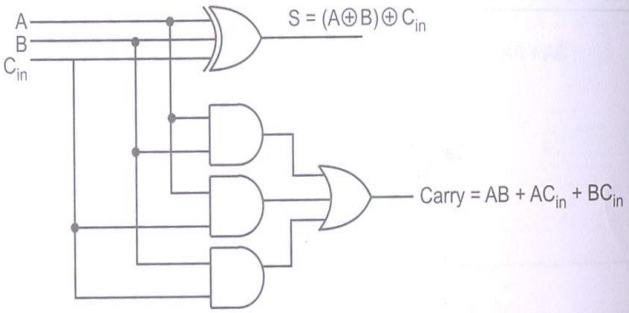
$$Sum = \bar{A}\bar{B}\,C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$

K-map for carry C_{out}



$C_{out} = AB + AC_{in} + BC_{in}$

Logic implementation of full adder:



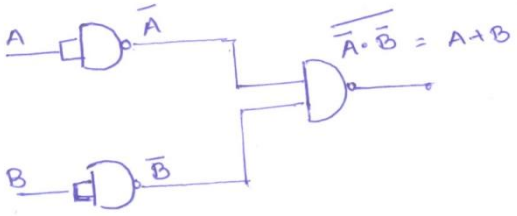
Q.3. **Attempt any four of the following: (16M)**

a) Reduce the given logic expression using Boolean law and draw NAND logic circuit.
$Y = A + \overline{A}.B + A.B$
(2M expression, 2M diagram)

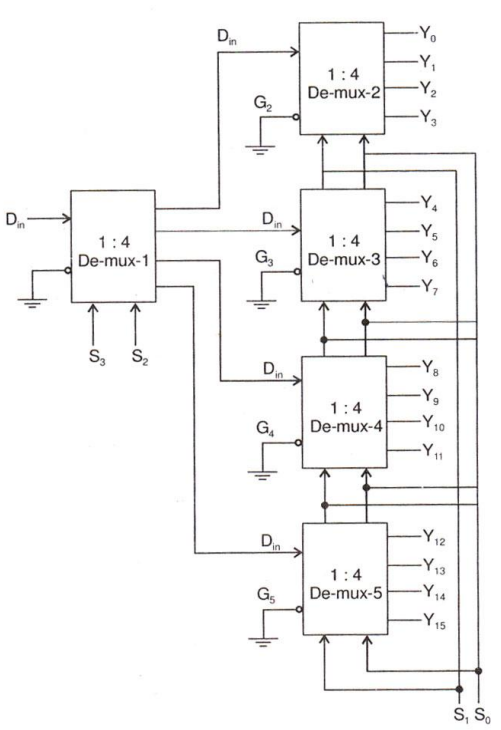
$Y = A + \overline{A} \cdot B + A \cdot B$

$= A + B \cdot (A + \overline{A})$

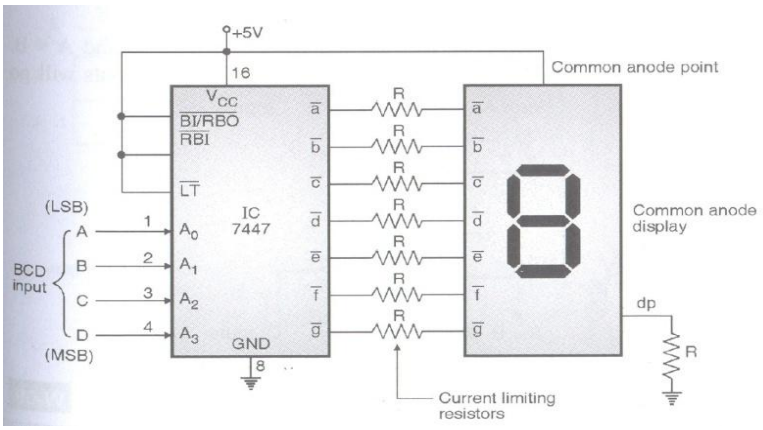
$= A + B$ $\quad (A + \overline{A} = 1)$



b) Construct 1:16 demultiplexer using only 1:4 demultiplexer.(4M)



c) Draw the block diagram of BCD to seven segment decoder/driver using IC 7447. Also draw it's truth table.(2M truth table, 2M diagram)



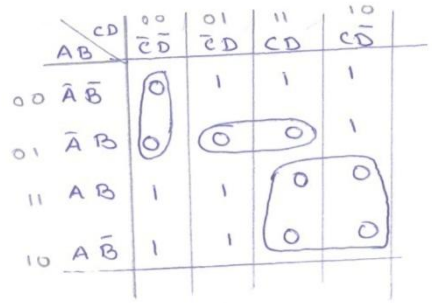
Truth Table of BCD to seven segment decoder

Decimal	Inputs				Outputs						
	B3	B2	B1	B0	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	0	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	1	0	0

d) For the given K-Map in figure No.2 , write the POS expression and draw NOR-NOR logic circuit for same.(1M Grouping, 1M expression, 2M diagram)

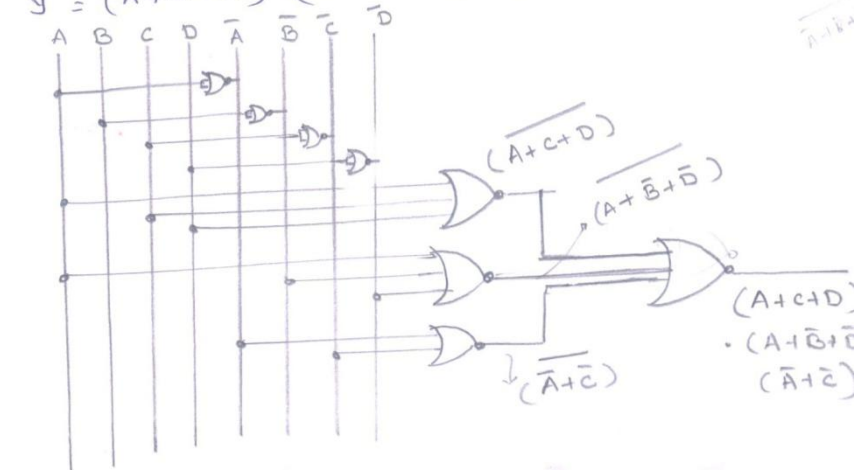
	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	1	1
$\bar{A}B$	0	0	0	1
AB	1	1	0	0
$A\bar{B}$	1	1	0	0

Fig. No. 2



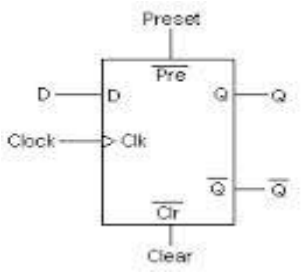
POS Expression

$Y = (A+C+D)\cdot(A+\bar{B}+\bar{D})\cdot(\bar{A}+\bar{C})$



e) Draw the symbol and truth table of followings:

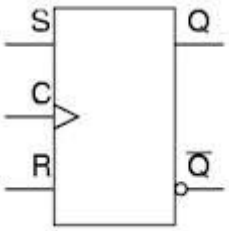
i. D-flip flop (1M Diagram, 1M truth table)



Truth Table

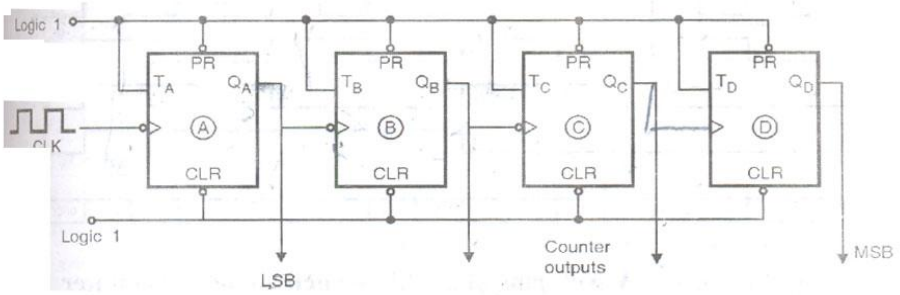
Input Dn	Output Q_{n+1}
0	0
1	1

ii. R-S flip flop
(1M Diagram, 1M truth table)



Inputs			Outputs		Comments
E	S	R	Q_{n+1}	$\overline{Q}_{n+1}$	
1	0	0	Q_n	$\overline{Q}_n$	No change
1	0	1	0	1	Rset
1	1	0	1	0	Set
1	1	1	x	x	Indeterminate

f) Draw the circuit diagram of 4 bit asynchronous counter and explain with timing diagram.(2M diagram,1M explanation, 1M timing diagram)
Note: Mark should be given to asynchronous down counter also)



4 bit asynchronous up counter

- Since it is 4 bit ripple up counter, we need to use four flip flops
- Initially all the flip flops have zero output

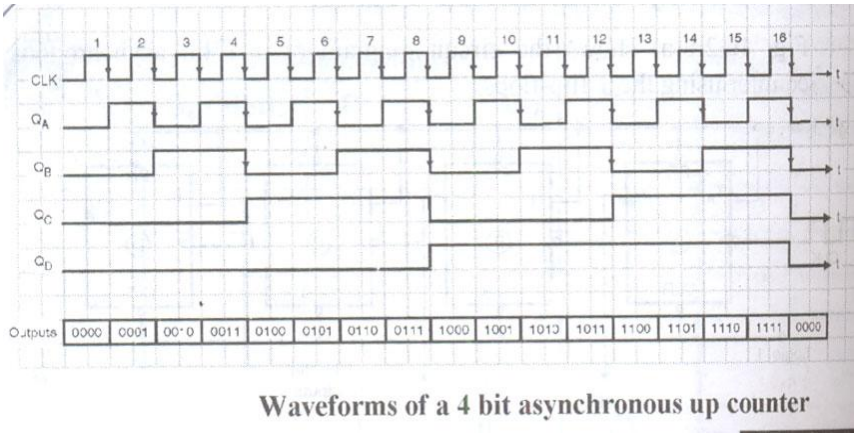
$$\therefore Q_D Q_C Q_B Q_A = 0000$$

- All the flip flops are negative edge triggered CLK is applied to the clock input of FF-A whereas Q outputs of every F/F is applied to the clock input of next F/F.
- The truth table for 4 bit asynchronous up counter is given below
- At every negative clock edge, the first flip flop is triggered.
- When the output of first flip flop goes from 1 to 0, the second flip flop is triggered.
- When the output of second flip flop goes from 1 to 0, the third flip flop is triggered.
- When the output of third flip flop goes from 1 to 0, the fourth flip flop is triggered.
- After 1111, the outputs again become 0000 and the operation repeats itself.

- Figure shows the timing diagram for the operation repeats it counter.
- Q_D acts as MSB of the output whereas Q_A act as the LSB

Truth table for a 4-bit asynchronous up counter

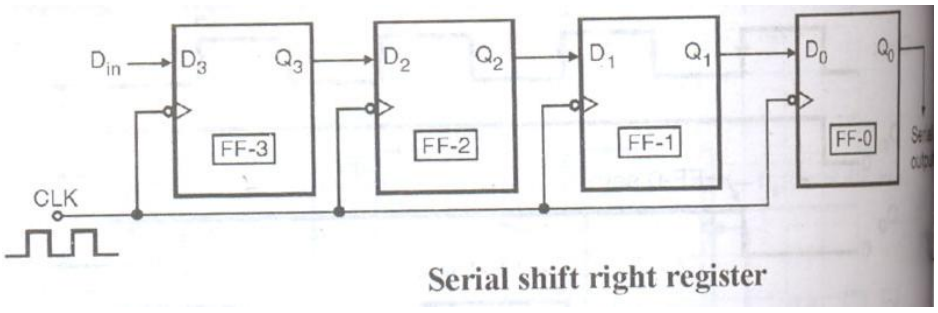
Clock	FF outputs.			
	Q_D	Q_C	Q_B	Q_A
Initially	0	0	0	0
1 (↓)	0	0	0	1
2 (↓)	0	0	1	0
3 (↓)	0	0	1	1
⋮ ⋮		⋮		
14 (↓)	1	1	1	0
15 (↓)	1	1	1	1
16 (↓)	0	0	0	0



Waveforms of a 4 bit asynchronous up counter

Q.4. **Attempt any FOUR of the following:**

a) Draw 4 bit SISO shift register using D-flip-flop and explain it's working with timing diagram.
(2M diagram, 1M explanation, 1M timing diagram)



Serial shift right register

Operation:

- **Before application of clock signal let** $\therefore Q_3Q_2Q_1Q_0 = 0000$ and apply LSB bit of the number to be entered to $D_{in}=D_3=1$.
- **Apply the clock. On the first falling edge of clock, the FF-3 is set and the stored word in the register is**

$$Q_3Q_2Q_1Q_0 = 1000$$

- **Apply the next bit to D_{in} so D_{in}=1**
- **As soon as the next negative edge of the clock hits, FF-2 will set and the stored word changes to,**

$$Q_3Q_2Q_1Q_0 = 1100$$

- **Apply the next bit to be stored i.e. 1 to D_{in}.**
- **Apply the clock pulse. As soon as the third negative clock edge hits, FF-1 will be set and the output get modified to,**

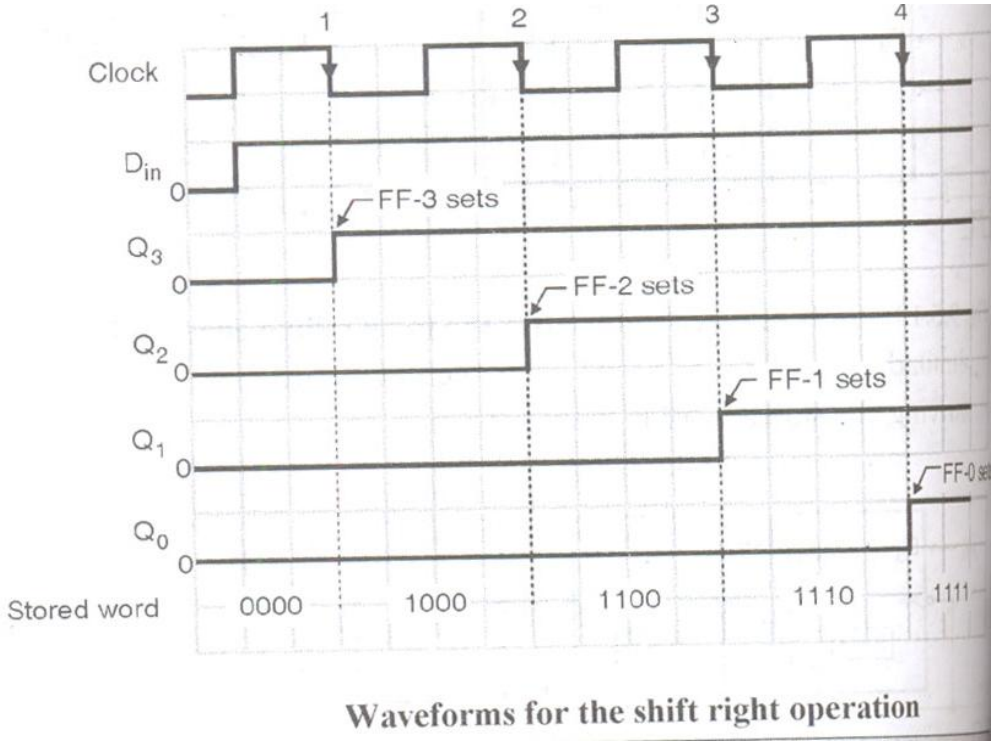
$$Q_3Q_2Q_1Q_0 = 1110$$

- **Similarly with D_{in} =1 and with the fourth negative clock edge arriving the stored word in the register is**

$$Q_3Q_2Q_1Q_0 = 1111$$

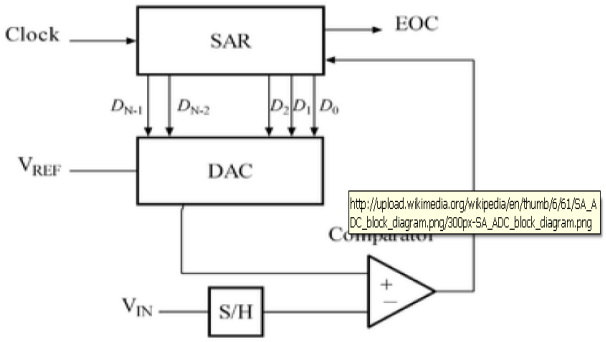
Summary of shift right operation

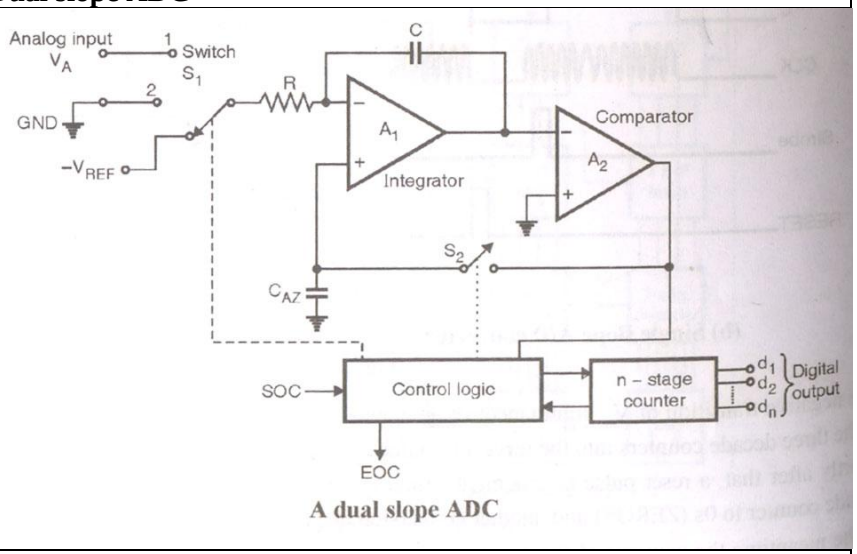
CLK	$D_{in} = Q_3$	$Q_3 = D_2$	$Q_2 = D_1$	$Q_1 = D_0$	Q_0
		0	0	0	0
↓	1	1	0	0	0
↓	1	1	1	0	0
↓	1	1	1	1	0
↓	1	1	1	1	1



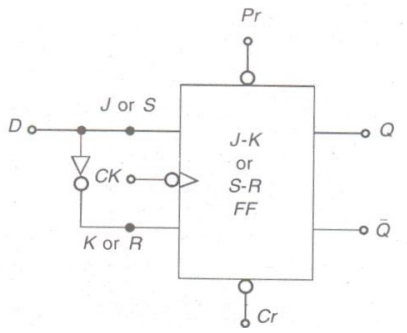
Waveforms for the shift right operation

b) Compare dual slope and successive approximation ADC on: (1M for each)

	Successive approximation ADC
Diagram	
Working Principle	This conversion technique involves comparing the output of DAC with the analog input signal V_{in}. The digital input to the DAC is generating by using successive approximation method. When the DAC output matches the analog signal the input to DAC is the equivalent digital signal. The successive approximation register SAR receives the comparator output, clock and start conversion signals and produces an n-bit digital output along with the end of conversion i.e. EOC signal**.**

	Dual slope ADC
Diagram	 **A dual slope ADC**
Working Principle	In this ADC, an unknown analog voltage and a known reference voltage are converted into equivalent time period using the integrator. These time period are then measured by a counter which gives the digital output. This circuit is called as Dual slope ADC because analog voltage VA and the reference voltage are converted into ramp signals of different slope by the integrator.

c) Construct D-flip flop using R-S flip flop and explain it's working along with truth table.(1M diagram, 2M working, 1M truth table)



Working:

The SR flip flop can be converted into D flip flop by simply the addition of an inverter.
This flip flop has only one input that is D input. The output Q will go to the same state that is present on the D input when negative edge of clock occurs.
The output Q_{n+1} at the end of the clock pulse equal the input D_n. hence we can say that the input data appears at the out put at the end of the clock pulse.
Thus the transfer of data from input to the output delayed and hence the name delay (D)flip flop.

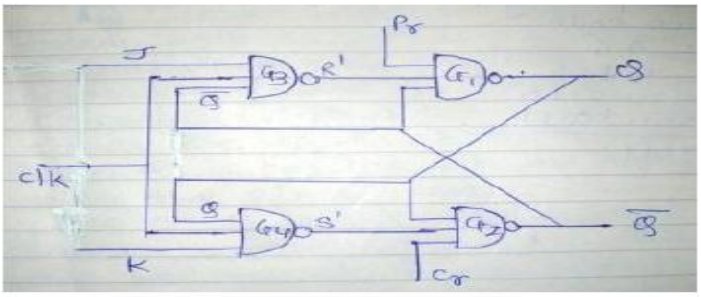
Truth table of a *D*-type FLIP-FLOP

Input D_n	*Output* Q_{n+1}
0	0
1	1

d) Draw and explain working of J-K flip flop with it's truth table. (1M diagram, 2M working, 1M truth table)

Truth Table

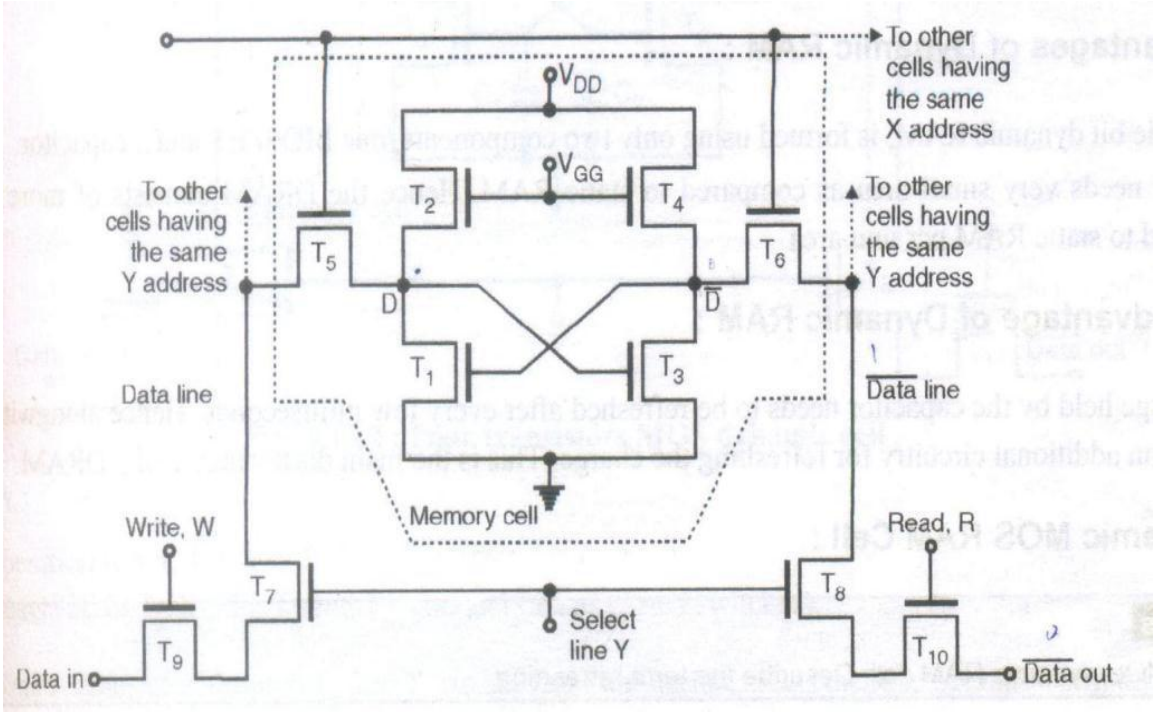
CLK	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q_n}$



The clock signal is applied to CK input. NAND gates G1 and G2 form an SR latch. The other two NAND gates G3 and G4 have three inputs which are J, Q and CK and K, Q and CK respectively.

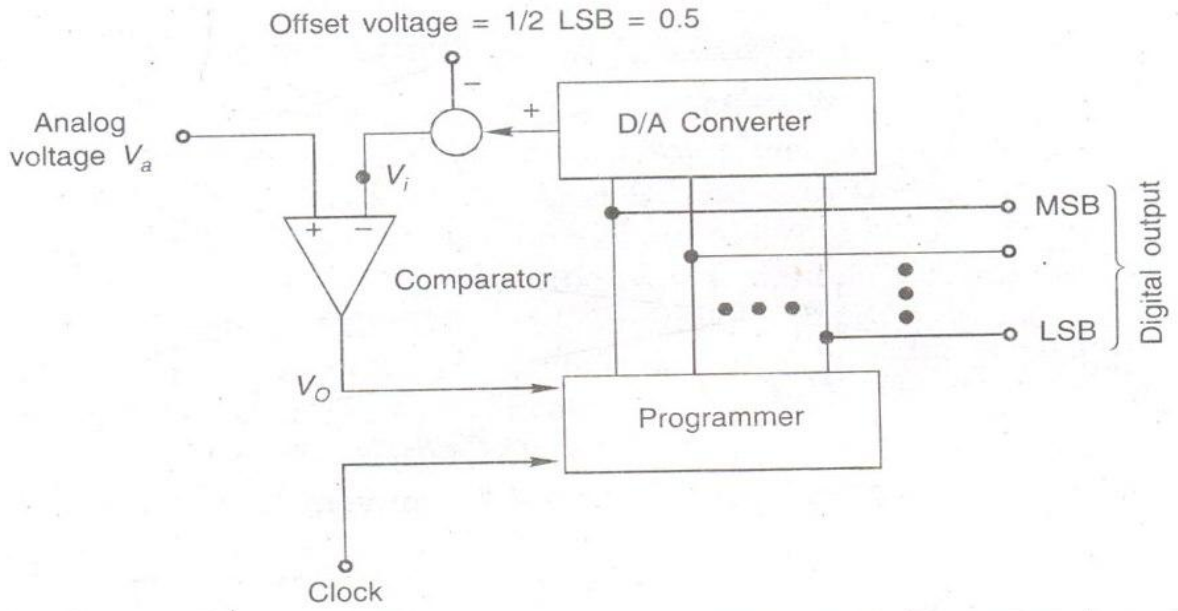
IF CK =0 than F/F is disabled and O/P Q and Q do not change
If CK= 1 and J=K=O then as $S^{\text{‟}}=R^{\text{‟}}=1$ the output Q and Q will not change their state.
If J=0 and K= 1 then JK flip flop will reset and Q= 0 & Q=1
If J=1 and K=0 then output will be set and Q=1 & Q=0
If J= K=1 then Q & Q outputs are inverted and FF will toggle

e) Draw and explain working of static RAM cell.
(2M diagram, 2M explanation)
Static RAM cell with NMOS CELL



T2 & T4 are acting as resistances. X & Y lines are used for addressing cell.
When X=Y=1 (high) ,the cell is selected . When X=1, the MOSFETS T5 & T6 are turned ON .,which will connect memory cell to the data line and data bar line.
When Y=1, the MOSFETS T 7 & T8 are turned ON. Which will make read & write operation possible
f) Study the given circuit as shown in fig no.1 intial o/p condition is QA QB QC = 010, write truth table of output $Q_AQ_BQ_C$

f) With neat circuit diagram, explain the working of successive approximation ADC.(2M diagram, 2M explanation)



Successive-approximation A/D converter.

The comparator does the work of comparing the analog voltage and the output of DAC. The output of the comparator is used to set or reset the bits at the output of the programmer. This output is converted into equivalent analog voltage from which the offset voltage is subtracted and then applied to the inverting input terminal of the comparator.

To start the conversion, the programmer sets the MSB to 1 and all other bits to zero. This is converted into analog signal by the DAC and the comparator compares it with the analog input voltage. If the analog input voltage Va >= Vi, the output of the comparator is HIGH which sets the next bit also. Otherwise output of the comparator is LOW which resets the MSB and sets the next bit. Thus a 1 is tried in each bit of the DAC until the binary equivalent of analog input voltage is obtained.

Q.5. Attempt any FOUR f the following: 16 Marks

a) Perform the binary arithmetic:

i) $(11011.11)_2 + (11011.01)_2$ ***(2 marks)***

Ans:

Carry:		**1**		**1**	**1**	**1**		**1**	
Binary Number:		**1**	**1**	**0**	**1**	**1**	**.**	**1**	**1**
Binary Number:	**+**	**1**	**1**	**0**	**1**	**1**	**.**	**0**	**1**
Addition	**=**	**1**	**1**	**0**	**1**	**1**	**1**	**.**	**0**	**0**

ii) $(11101.1101)_2 - (101.011)_2$ ***(2 marks)***

Ans:

Borrow:									1	1	
Binary Number:		1	1	1	0	1	.	1	1	0	1
Binary Number:	-			1	0	1	.	0	1	1	
Subtraction	=	1	1	0	0	0	.	0	0	0	1

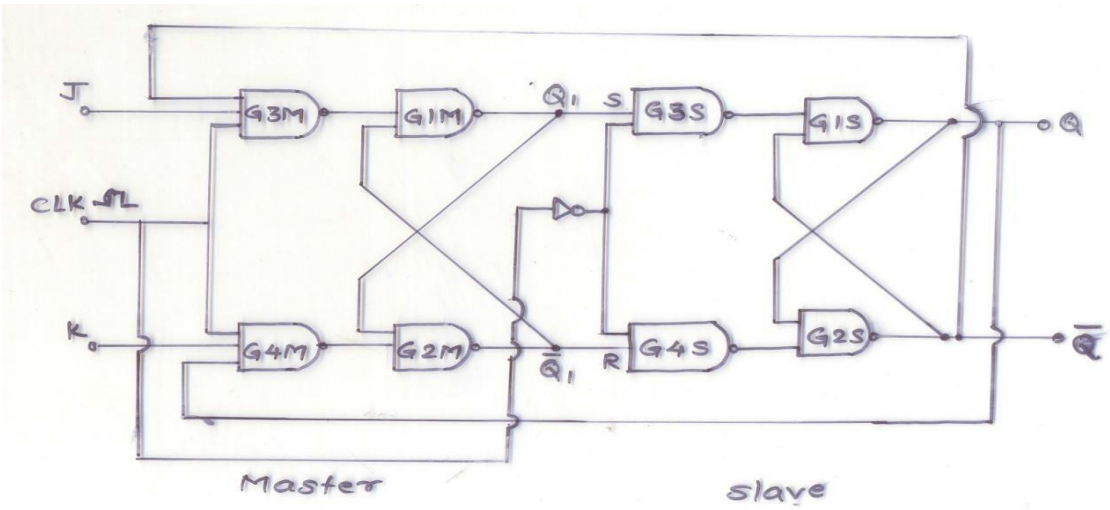
b) Explain the techniques used in elimination of Race –around condition.

The race around condition in JK flip-flop can be avoided by:

1) **Using the edge triggered JK flip flop.** ***(2 marks)***

- For the racing around to take place, it is necessary to have the enable input high aong with J=K=1.
- As the enable input remains high for a long time in a JK latch, the problem of multiple toggling arises.
- But in edge triggered JK flip flop, the positive clock pulse is present only for very short time.
- Hence by the time the changed output return back to the inputs of NAND gates 3 and 4, the clock pulse has died down to zero. Hence the multiple toggling can not take place.
- Thus the edge triggering avoids the race around condition.

2) **Using the master slave JK flip-flop.** ***(2 marks)***



Master slave JK FF.

Master Slave flip flop, the master directly gets the clock pulse, where as the slave gets the clock pulse through a NOT gate. Hence even if the output of slave is connected to input of master, the output of slave cannot change as it does not get the clock transition.

c) Using Boolean laws, simplify the expression:
(One of the possible solution other correct solution can give 4 marks)
Ans.:

$Y = A(\bar{A}C)(\bar{A}B+\bar{C})$

$Y = A(\bar{A}C\bar{A}B + \bar{A}C\bar{C})$

Since $\bar{A}\bar{A} = \bar{A}$ & $C\bar{C} = 0$

$Y = A(\bar{A}BC + 0)$

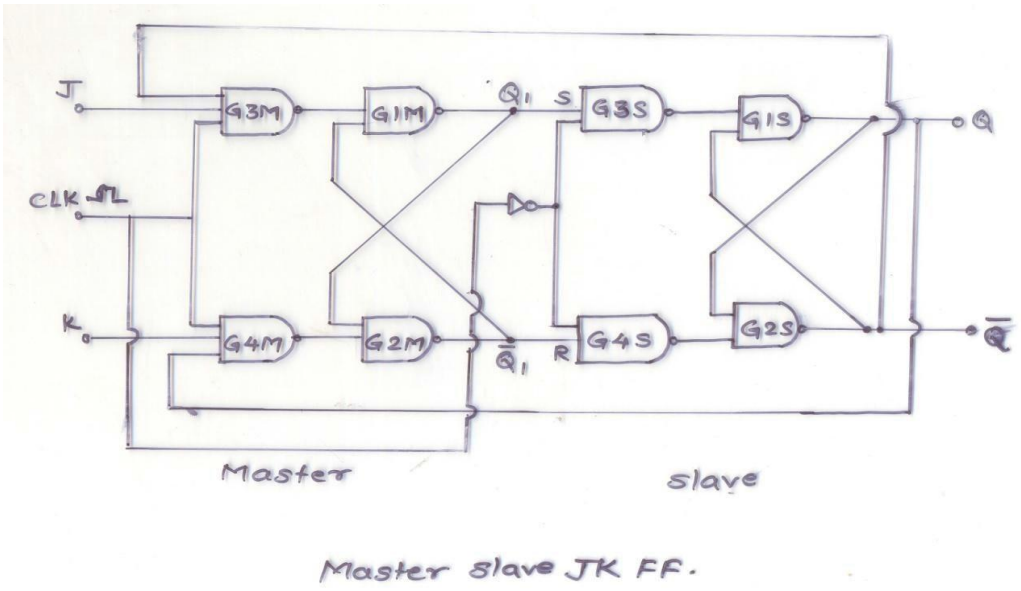
$Y = A\bar{A}BC + 0$

Since $A\bar{A} = 0$

$Y = 0 + 0$

$Y = 0$

d) Draw Master- slave J-K flip-flop and explain it`s working.
(Diagram 2Marks, Truth Table 1 Mark, Explanation 1Mark)



Master slave JK FF.

Truth table:

Case	Inputs			Outputs		Remark
	CLK	J	K	Q_{n+1}	$\bar{Q}_{n+1}$	
I	X	0	0	Q_n	$\bar{Q}_n$	No change
II	⎍ (1)	0	0	Q_n	$\bar{Q}_n$	No change
III	⎍ (1)	0	1	0	1	Reset
IV	⎍ (1)	1	0	1	0	Set
V	⎍ (1)	1	1	$\bar{Q}_n$	Q_n	Toggle

Case I: Clock=x, J=K=0

For clock=1 the master is active, slave in active. As J=K=0.There fore Output of master i.e. Q1 and will not change. Hence $\overline{Q_1}$ the S and R inputs to the slave will remain unchanged.

As soon as clock=0, the slave becomes active and master is inactive. But since the S and R inputs have not change the slave outputs will also remain unchanged.
There fore the output will not change if J=K=0

Case II: clock =⎍ , J=K=0

This condition has been already discussed in case I.

Case III: Clock= ⎍ , J=0 and K=1

- Clock=1: Master active, slave inactive.
- Output of the master become Q1=0 and $\overline{Q_1}$=1.That means S=0and
- R=1Clock =0slave active master inactive
- Outputs of the slave become Q=0and=$\overline{Q_1}$ =1
- Again if clock=1: master active, slave inactive.
- Even with the change output Q=0and $\overline{Q_1}$=1fed back to master, its outputs will Q1=0and $\overline{Q_1} = 1$ that means S=0and R=1.
- Hence with clock=0 and slave becoming active, the outputs of slave will remain Q=0and $\bar{Q} = 1$.
- Thus we get a stable output from the Master Slave.

Case iv: CLK=⎍ , J=1, K=0

- Clock =1 master active, slave inactive
- Outputs of master become Q1=1and $\overline{Q_1}$=0 i.e. S=1,
- R=0Clock=0:master inactive slave active.
- Outputs of slave become Q=1and $\overline{Q_1}$=0.
- Again if clock=1then it can be shown that the outputs of the slave are stabilized to Q=1and $\overline{Q_1} = 0$

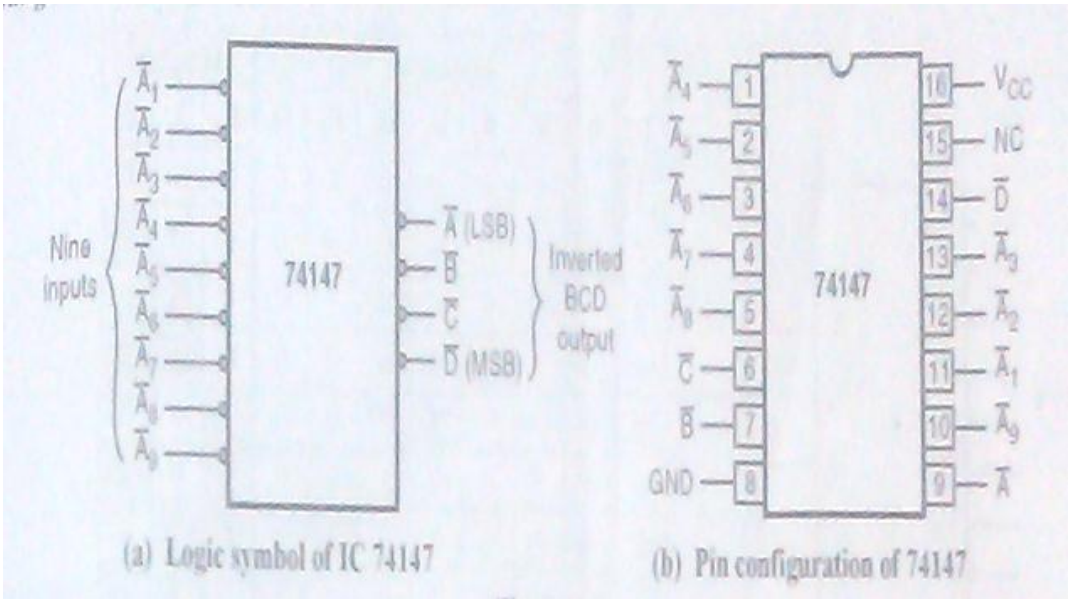
Case V: CLK: =⎍, J=1, K=1

- Clock =1: master will be active, slave inactive.
- Outputs of master will toggle so S and R also will be inverted. Clock=0: master inactive, slave active
- Outputs of the slave will toggle.
- These changed outputs are returned back to the master inputs.
- But since clock=0,the master is still inactive. So it does not respond to these changed outputs.
- This avoids the multiple toggling which leads to the race around condition. Thus the master slave flip flop will avoid the race around condition

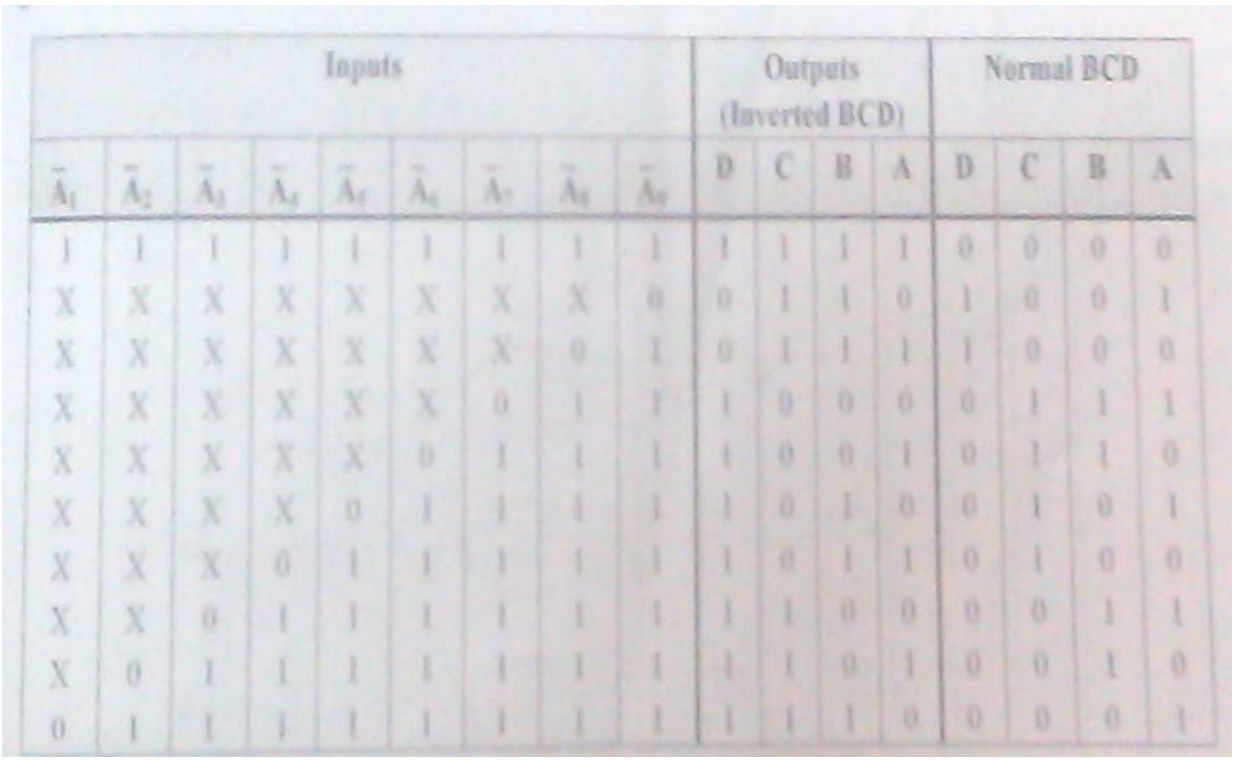
e) Describe the operation of decimal to BCD encoder IC 74147 with its truth table and pin diagram.

Ans: ***(Diagram 2 mark, Explanation 1 Mark, Truth table 1 Mark, can be given for active low input and active low output truth table also)***

- IC 74147 is basically a 10:4 encoder or decimal to BCD encoder.
- A1 to A9 are Active low inputs and A,B,C D are the active low outputs.



One of the most commonly used input device for a digital system is a set of ten switches, one for each numeral between 0 to 9. These switches generate 0 or 1 logic levels in response to turning them OFF or ON respectively. When a particular number is to be fed to the digital circuit in BCD code the switch corresponding to that number is pressed. The block diagram is as shown above and truth table for active high input and active high output is as shown below.



Inputs									Outputs (Inverted BCD)				Normal BCD			
$\bar{A}_1$	$\bar{A}_2$	$\bar{A}_3$	$\bar{A}_4$	$\bar{A}_5$	$\bar{A}_6$	$\bar{A}_7$	$\bar{A}_8$	$\bar{A}_9$	D	C	B	A	D	C	B	A
1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
X	X	X	X	X	X	X	X	0	0	1	1	0	1	0	0	1
X	X	X	X	X	X	X	0	1	0	1	1	1	1	0	0	0
X	X	X	X	X	X	0	1	1	1	0	0	0	0	1	1	1
X	X	X	X	X	0	1	1	1	1	0	0	1	0	1	1	0
X	X	X	X	0	1	1	1	1	1	0	1	0	0	1	0	1
X	X	X	0	1	1	1	1	1	1	0	1	1	0	1	0	0
X	X	0	1	1	1	1	1	1	1	1	0	0	0	0	1	1
X	0	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0
0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1

f) Define 'Modulus of counter'. Determine number of flip flops to be used in MOD-21 counter.
Modulus of a counter is the no. of different states through which the counter progress during its operation. It indicates the no. of states in the counter, pulses to be counted are applied to counter. The circuit comes back to its starting state after counting N pluses in the case of modulus N counter.
(2 Marks)

In general m number of flip-flops are required to construct MOD-n counter, where $n <= 2^m$

(2 Marks)

MOD n Counter = 2^m

Where **m** is no. of flipflops and **n** is No. of couners.

MOD 21= 2^m Hence **m=5**

(5 flip flops are required for MOD 21)

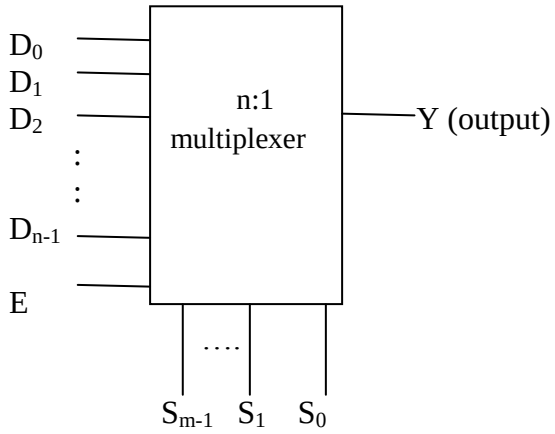
MOD n counter	Number of flip-flops(m)
21	**5**

Q 6. Attempt any <u>TWO</u> the following: 16 Marks

a) (i) Define and draw the logical symbol of multiplexer.

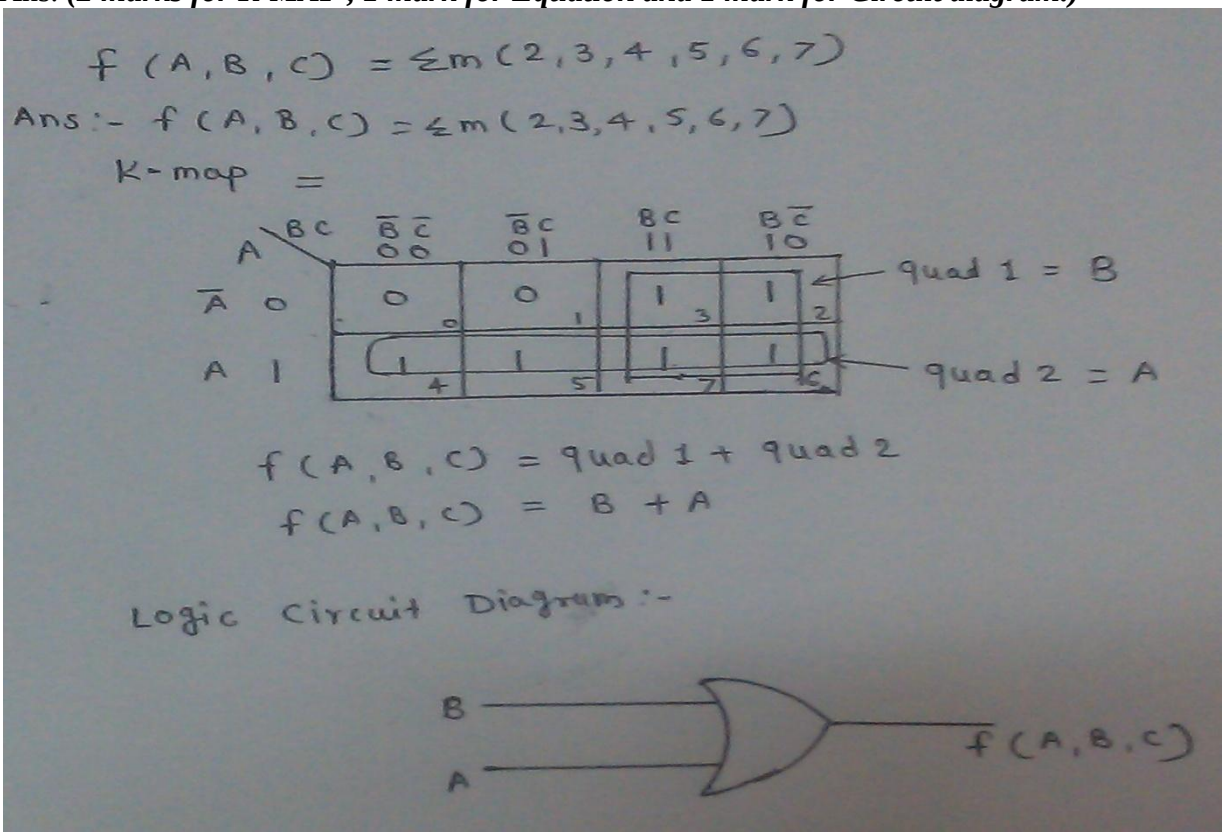
(Definition and short explanation 2 marks, Symbol 2 marks)

- Multiplexer is a special type of combinational circuit.
- A multiplexer is a digital circuit which selects one of the n data inputs and routes it to the output. The selection of one of n inputs is done by the select inputs.
- Symbol with n data inputs, one output, m select inputs.



(ii) Find the reduced form of following function.
f(A,B,C) = ∑m(2, 3, 4, 5, 6, 7) using K-map and draw logic circuit.

Ans. ***(2 marks for K-MAP , 1 mark for Equation and 1 mark for Circuit diagram.)***

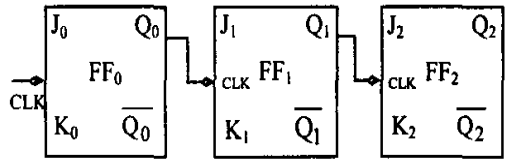
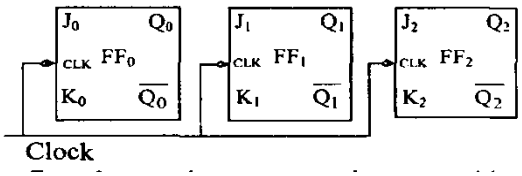


b) **(i) List four applications of flip flops.** ***(2 marks)***
(Any four ½ marks for each)

1. Elimination of keyboard debounce.
2. As a memory elements.
3. In various types of registers.
4. In counters/timers.
5. As a delay elements

.

(ii) Compare synchronous and asynchronous counter on any two points.
(2 marks) (Any two points of the following 1 mark for each point)

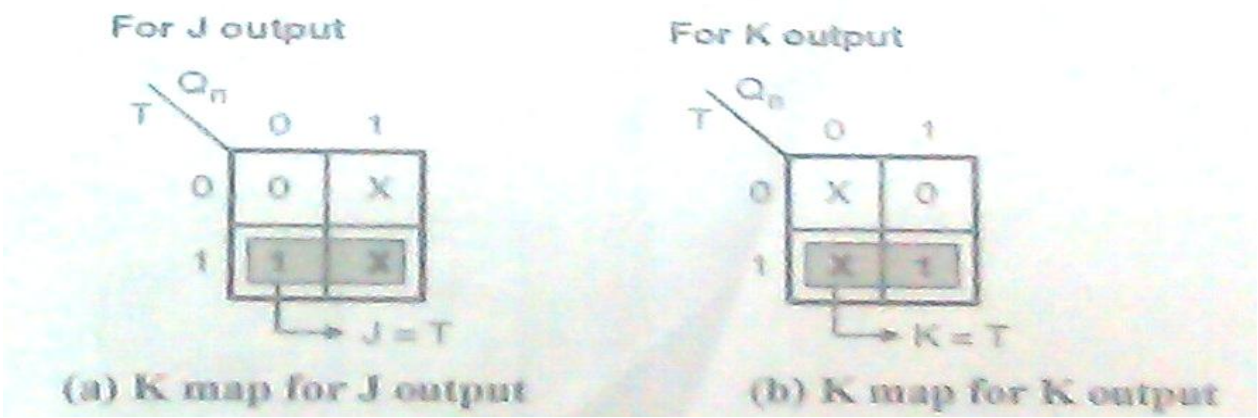
No.	Asynchronous Counter	Synchronous Counter
1.	In an Asynchronous Counter the output of one Flip Flop acts as the clock Input of the next Flip Flop.	In a Synchronous Counter all the Flip Flop's are Connected to a common clock signal.
2.	Speed is Low	Speed is High
3.	Only J K or T Flip Flop can be used to construct Asynchronous Counter	Synchronous Counter can be designed using JK,RS,T and D FlipFlop.
4.	Problem of Glitch arises	Problem of Lockout
5.	Only serial count either up or down is possible.	Random and serial counting is possible.
6.	Settling time is more	Settling time is less
7.	Also called as serial counter	Also called as Parallel Counter
8.		

(iii) Convert JK- flip flop in to T-flip flop. Write it`s truth table and explain.
Ans: ***(1 mark truth table, 1 mark K-MAP, 2 marks diagram)***

Truth table for conversion:

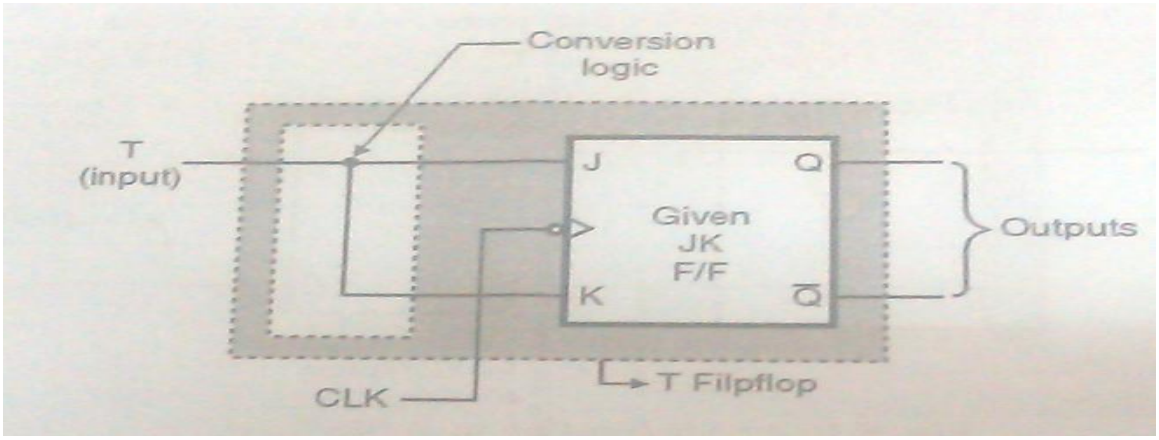
Inputs			Outputs	
T	Present state of Q	Next state of Q	J	K
0	0	0	0	X
1	0	1	1	X
1	1	0	X	1
0	1	1	X	0
← Excitation table of T FF →				
← Excitation table of JK FF →				

K map and simplification:



(a) K map for J output (b) K map for K output

Logic diagram:



c) (i) List any four specifications of DAC.

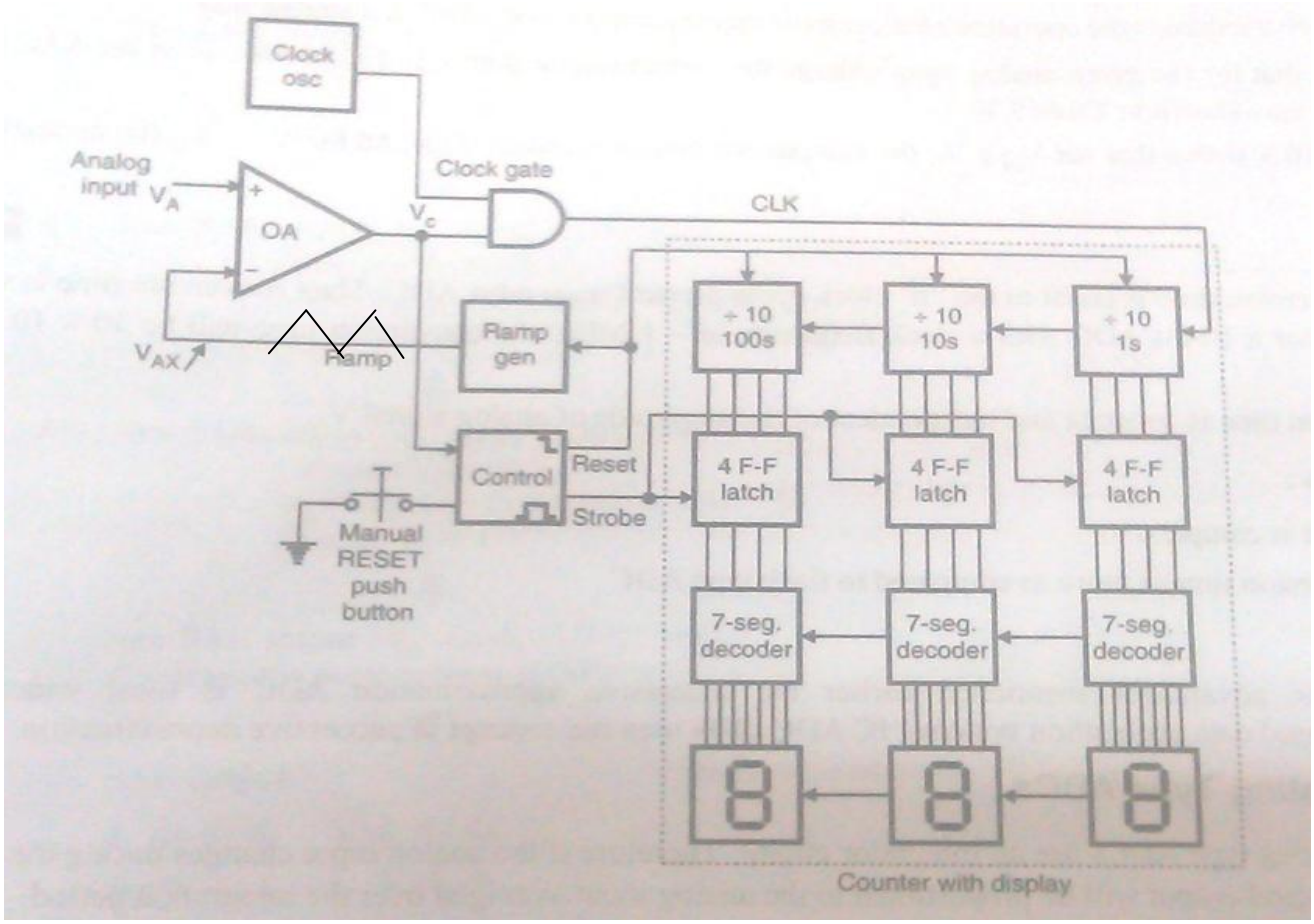
(Any 4 specification – 1/2 mark each specification) (2 Marks)

1. Resolution
2. Accuracy
3. Linearity

4. Temperature sensitivity
5. Settling time
6. Speed
7. Long term Drift
8. Supply rejection

(ii) Draw neat block diagram of Ramp ADC and explain its working.

Ans. ***(3 marks for circuit diagram and 3 marks for working) (6 marks)***

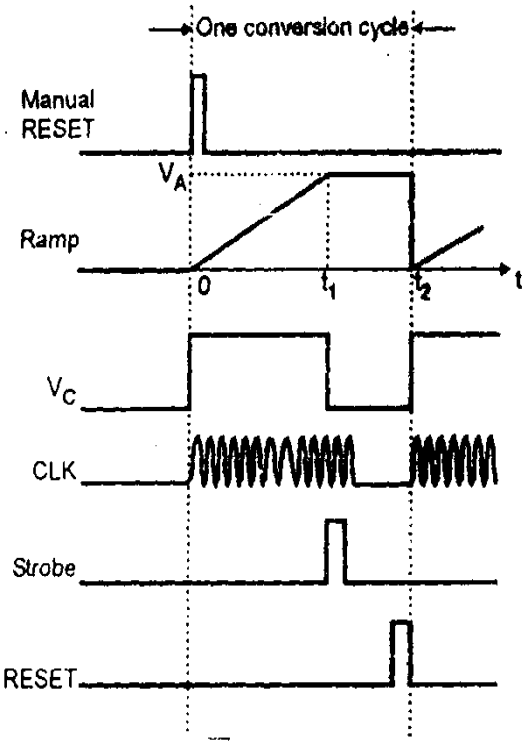


- The single slope ADC consists of a counter with display unit.
- The display unit consists of 7-segment decoder and 7 segment display.
- The circuits also contain a Control block, Ramp generator and OP-AMP as a comparator.
- The output of ramp generator is fed to comparator which compares the same with analog input voltage. Vc(output of comparator)controls the gating to the clock and also informs control circuit about completion of the conversion

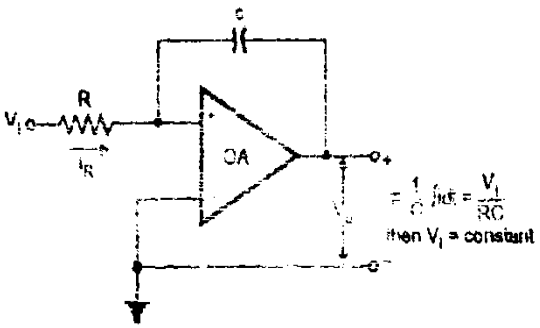
WORKING

1. Manual RESET, will reset ramp generator as well as counter.
2. The analog voltage $V_A$has to be positive. Hence the RAMP begins at 0V.
3. Since $V_{AX}<V_A$, the output of the comparator Vc=1 (HIGH).
4. This will enable CLOCK gate allowing the CLK input, to be applied to the counter.
5. The ramp generator may make use of counter type ADC or simple integrator.

6. As counter receives clock pulses, it will count up; and the RAMP continues upward. RAMP voltage rises till it reaches to VAinput voltage.
7. When the ramp voltage reaches the input analog voltage, the output Vc = 0(LOW) and it will disable CLOCK gate and counter cease to advance.
8. The negative transition of Vc simultaneously generates a strobe signal in the CONTROL box that shifts the contents of the three decade counters into the three 4 FF latch circuit.
9. After the generation of STROBE signal, a reset pulse is generated by the CONTROL box that resets the RAMP and clears the decade counter to 0's(ZEROS) and another conversion cycle begins.
10. During this time the contents of the previous conversion, are contained in the latches and are displayed on the seven segment display.



(a) Single slope A/D converter



(b) An integrating circuit