WINTER – 19EXAMINATION

Subject Name:Digital Technique **Model Answer** Subject Code: 17333

Important Instructions to examiners:

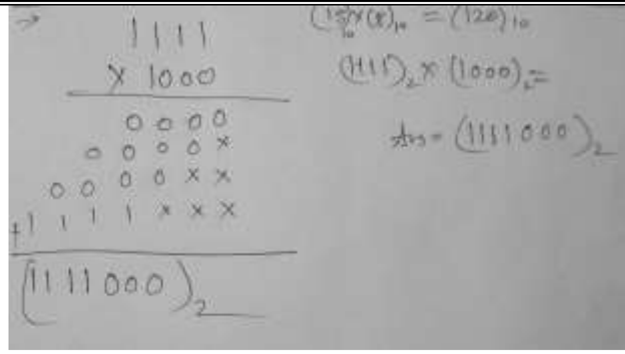
1) The answers should be examined by key words and not as word-to-word as given in themodel answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may tryto assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given moreImportance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in thefigure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constantvalues may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q. N.	Answer	Marking Scheme
Q.1	**(A)**	**Attempt any SIX of the following:**	**12Marks**
	(a)	**Compare analog system with digital system. (any 4 points)**	**2M**
	Ans:	(see table below)	**2M(1/2 each)**

Parameter	Analog systems	Digital systems
1. Type of signals processed	Analog signals	Digital signals
2. Type of display	Analog meters	Digital displays using LED and LCD.
3. Accuracy	Less	More
4. Design complexity	Difficult to design	Easier to design
5. Memory	No memory	They have Memory
6. Storage of information	Not Possible	Possible
7. Effect of noise	More	Less
8. Versatility	Less	More
9. Distortion	More	Less

	(b)	**Perform the following multiplication in binary number system:** **$(15)_{10} \times (8)_{10}$**	**2M**

Ans: **2M**



(c) **Define following characteristics of IC's** **2M**

(i) Propagation delay
(ii) Noise immunity

Ans: **(i) Propagation delay:** **1M each**

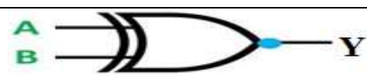
Propagation delay is the average transition delay time for the signal to Propagate from input to output when the signals change in value. It is expressed in ns.

(ii) Noise immunity:

The circuit's ability to tolerate noise signals is referred to as noise immunity. It is generally expressed in terms of high level and low level noise margins (expressed in voltage)

(d) **Draw logic symbol and truth table of two i/p Ex-NOR gate.** **2M**

Ans: **1M each**



Y= $\bar{A}\bar{B}$ + AB

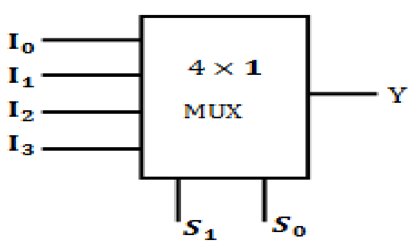
Y = A $\odot$ B

TRUTH TABLE:

A	B	Y= A $\odot$ B
0	0	1
0	1	0
1	0	0
1	1	1

(e) **Draw block diagram of 4:1 Mux and give its truth table.** **2M**

Ans: **1M each**



Truth table

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(f) **How many filp-flop are required to construct following modulus counter** **2M**

		(i) 56 **(ii) 83** **(iii) 99** **(iv) 10**	
	Ans:	The Number of flip flops are calculated from the formula: 2 n ≥ m Where n= no of flip flops and m is the number of states. i) 56= 6 ii) 83 = 7 iii) 99 = 7 iv) 10 = 4	**½ each**
	(g)	**List any four applications of A/D converter.**	**2M**
	Ans:	1. In a digital signal processing system, an ADC is required if the input signal is analog. For example, a fast video ADC is used in TV tuner cards. 8, 10, 12, or 16 bit analog to digital controllers are common in microcontrollers. 2. They are also needed in digital storage oscilloscopes. 3. Analog to digital converters are used in music reproduction technology when done using computers. In such an application, an ADC is needed when an analog recording is used in order to create the PCM data stream that goes onto a CD or a digital music file. 4. ADC is used in Cell phones 5. Computers use analog-to-digital converters in order to convert signals from analog to digital before they can be interpreted. For example, a modem will convert signals from digital to analog before transmitting them over telephone lines that carry only analog signals. These signals are then converted back into digital form at the receiving end so that the computer can interpret the data in digital format. 6. ADC is used in digital voltmeters 7. ADC is used in digital oscilloscope	**Any four Applications 2M**
	(h)	**Write any four Boolean laws used to reduce Boolean Expression.**	**2M**
	Ans:	Boolean laws: A + 1 = 1 A + 0 = A A . 1 = A A . 0 = 0 A + A = A A . A = A A+B = B+A A.B = B.A (A + B) + C = A + (B + C) (A B) C = A (B C) A (B + C) = A B + A C A + (B C) = (A + B) (A + C)	**Any 4 Boolean laws ½ each**

	b)	**Attempt any TWO of the following:**	**8 Marks**
	(a)	**Define the following terms with reference to logic families:** **(i) Threshold voltage**	**4M**

(ii) Power dissipation
(iii) Operating speed
(iv) Logic voltage level

Ans:

1M each

(i) Threshold voltage: Threshold voltage is defined as the minimum voltage that required to make the transistor ON.

(ii) Power dissipation:
It is the amount of power dissipated in an IC.
Power Dissipation is given by P = Vcc X Icc
This power is in milliwatts.

(iii) Operating speed:
Speed of Operation: Speed of a logic circuit is determined by the time between theapplication of input and change in the output of the circuit.

(iv) Logic voltage level:
<u>Positive Logic</u>: A Logic 1 level represents a more positive of the two voltage levels while the least positive of the two voltage levels represents a logic 0 level.
Example, If +5 V represents a logic 1 level And 0 V represents a logic 0 level Logic 1 = +5V Logic 0 = 0V Or if logic 1= +5V, logic 0 = +2V
<u>Negative Logic</u>: A Logic 1 level represents a most negative of the two voltage levels while the least negative of the two voltage levels represents a logic 0 level.
Example, If 0V represents a logic 1 level And +5V represents a logic 0 level Logic 1 = 0V Logic 0 = +5V Or if logic 1= +2V, logic 0 = +5V

(b) State and prove De Morgan's theorems **4M**

Ans:

Theorem1: It state that the, complement of a sum is equal to product of its complements.

A	B	$\overline{A+B}$	$\bar{A}$	$\bar{B}$	$\bar{A}\cdot\bar{B}$
0	0	1	1	1	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	0

LHS $\overline{A+B} = \bar{A}\cdot\bar{B}$ RHS

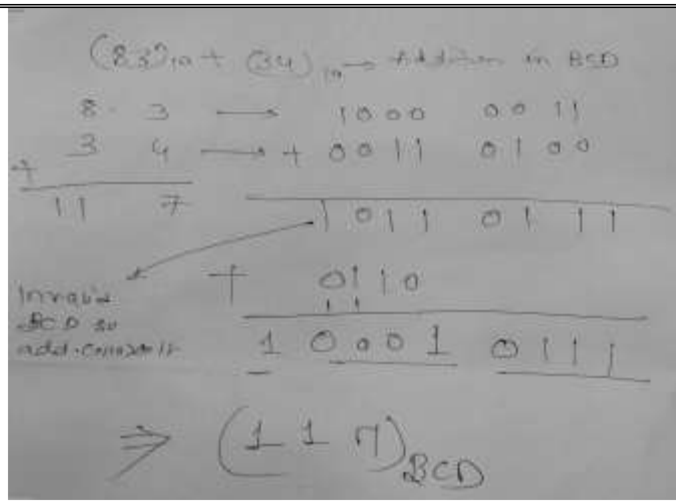
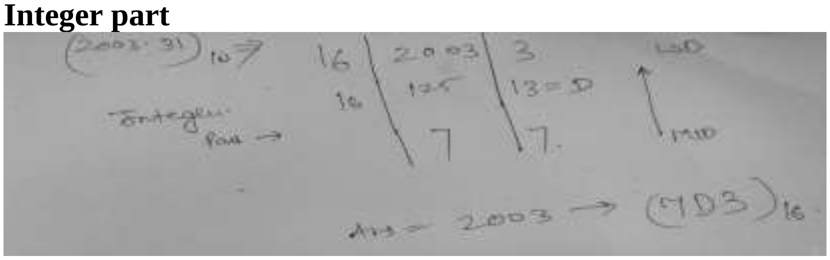
Theorem2: It states that, the complement of a product is equal to sum of the complements.

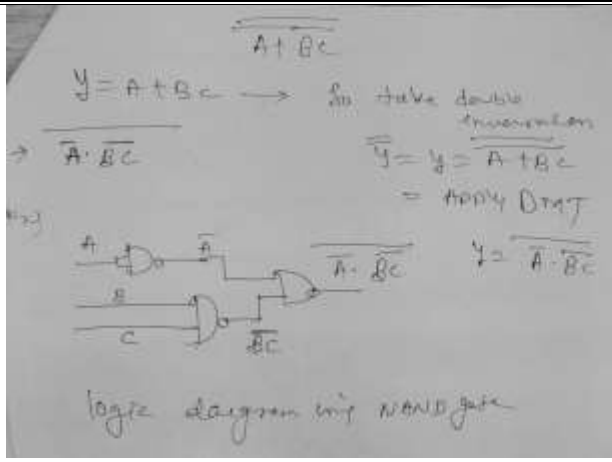
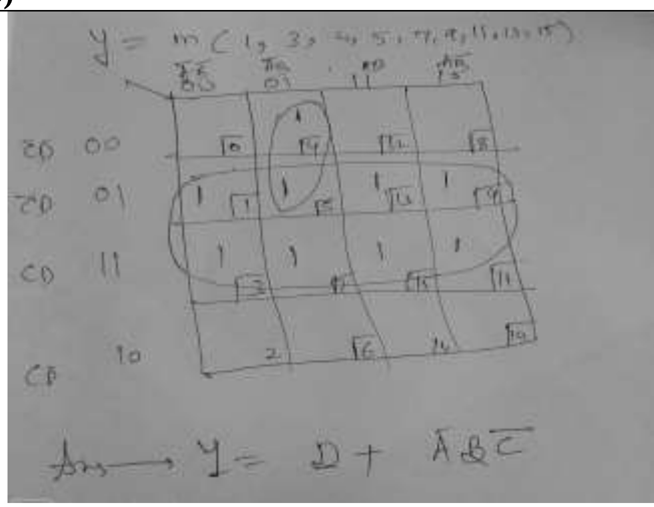
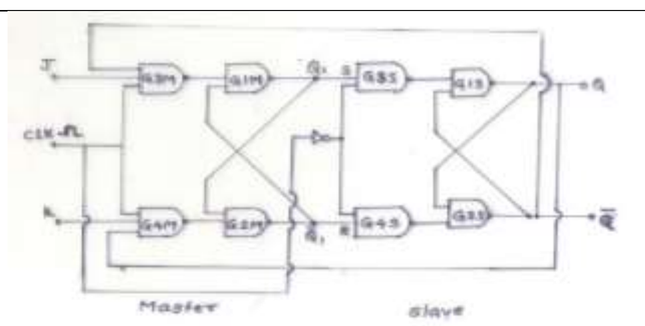
2M each

A	B	$\overline{AB}$	$\bar{A}$	$\bar{B}$	$\bar{A}+\bar{B}$
0	0	1	1	1	1
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	0	0	0

LHS $\overline{AB} = \bar{A}+\bar{B}$ RHS

: Verification of the theorem $\overline{AB} = \bar{A}+\bar{B}$

	(C)	**Add $(83)_{10}$ and $(34)_{10}$ in BCD.**	**4M**
	Ans :		**Conversion-1M** **Addition-1M** **Final Answer-2M**
Q. 2		**Attempt any FOUR of the following:**	**16 Marks**
	(a)	**Convert (2003.31)10 to hex equivalent.**	**4M**
	Ans :	**Fractional Part** **(.31*16) = 4.96** MB **(0.96*16) =15.36(F)** **(.36*16) = 5.76** LSD **(.76*16) = 12.16(C)** **Integer part** Final answer=$(7D3.4F5C)_{16}$	**2M fractional part** **2M integer part**
	(b)	**Implement the following expression by minimizing the variable using Universal gate** **$Y= A\bar{B} + AB + \bar{A}BC + ABC$**	**4M**

	Ans :	 $= A\bar{B} + AB + \bar{A}BC + ABC$ $= A(B + \bar{B}) + BC\,(A + \bar{A}\,)$ $= A+BC$	**4M**
	(c)	**Simplify using K map and Realize reduced expression using gates f(A,B,C,D)= Σm (1,3,4,5,7,9,11,13,15)**	**4M**
	Ans :		**Kmap-1M** **Pair-1M** **Final equation-2M**
	(d)	**Draw master slave- JK flip-flop using NAND gates and explain its working.**	**4M**
	Ans :	 Master slave JK FF. <table><tr><th>Case</th><th colspan="3">Inputs</th><th colspan="2">Outputs</th><th>Remark</th></tr><tr><td></td><td>CLK</td><td>J</td><td>K</td><td>Q_{n+1}</td><td>$\bar{Q}_{n+1}$</td><td></td></tr><tr><td>I</td><td>X</td><td>0</td><td>0</td><td>Q_n</td><td>$\bar{Q}_n$</td><td>No change</td></tr><tr><td>II</td><td>⎍ (1)</td><td>0</td><td>0</td><td>Q_n</td><td>$\bar{Q}_n$</td><td>No change</td></tr><tr><td>III</td><td>⎍ (1)</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Reset</td></tr><tr><td>IV</td><td>⎍ (1)</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Set</td></tr><tr><td>V</td><td>⎍ (1)</td><td>1</td><td>1</td><td>$\bar{Q}_n$</td><td>Q_n</td><td>Toggle</td></tr></table>	**(2M-diagram,1M-truthtable,1M explaination)**

Truth table

Master Slave flip flop, the master directly gets the clock pulse, whereas the slave gets the clock pulse through a NOT gate. Hence even if the output of slave is connected to input of master, the output of slave cannot change as it does not get the clock transition.

Case I: Clock=x, J=K=0

For clock=1 the master is active, slave in active. As J=K=0.Therefore Output of master i.e. Q1 and $\overline{Q_1}$ will not change. Hence the S and R inputs to the slave will remain unchanged.

Case II:clock= present , J=K=0

This condition has been already discussed in case I.

Case III:

Clock=1: Master active, slave inactive.

Output of themasterbecome Q1=0 and $\overline{Q_1}$=1.ThatmeansS=0and R=1Clock =0slave active masterinactive

Outputs of the slave become Q=0and= $\overline{Q_1}$=1

Thus we get a stable output from the MasterSlave.

Case VI:

Clock =1 master active, slave inactive

Outputs of master become Q1=1and $\overline{Q_1}$=0 i.e. S=1, R=0Clock=0:master inactive slaveactive.

Outputs of slave become Q=1and$\overline{Q_1}$=0.

Again if clock=1then it can be shown that the outputs of the slave are stabilized to Q=1and $\overline{Q_1} = 0$

Case V:CLK: = , J=1, K=1

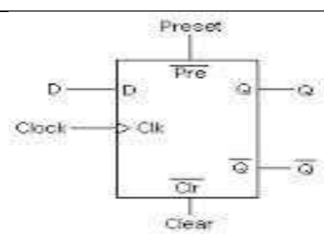
Clock =1: master will be active, slave inactive.

Outputs of master will toggle so S and R also will be inverted. Clock=0: master inactive, slave active

- Outputs of the slave willtoggle.

These changed outputs are returned back to the master inputs.

- But since clock=0,the master is still inactive. So it does not respond to thesechangedoutputs.
- This avoids the multiple toggling which leads to the race around condition. Thusthe master slave flip flop will avoid the race aroundcondition.

(e)	**Draw symbol of D flip-flop and write down its truth table**	**4M**
Ans:		**(2M- symbol 2M- truth table)**

Truth Table:

clock	Input Dn	Output Q_{n+1}
1	0	0
1	1	1

(Note: Symbol of D flip flop using any triggering method can be consider.)

(f) **Convert following equation to standard SOP form** — **4M**

$Y= (A + B\bar{C})\ (B +AC)$

Ans : — **4M**

f) SOP

$Y = (A + B\bar{C})(B + AC)$

$Y = AB + A\cdot AC + B B\bar{C} + ABC\bar{C}$

$Y = AB + AC + B\bar{C} + 0$

$Y = AB(C+\bar{C}) + AC(\bar{B}+B) + (A+\bar{A})(B\bar{C})$

$Y = \underbrace{ABC}_{1} + \underbrace{AB\bar{C}}_{2} + \underbrace{ABC}_{1} + A\bar{B}C + \underbrace{AB\bar{C}}_{2} + \bar{A}B\bar{C}$

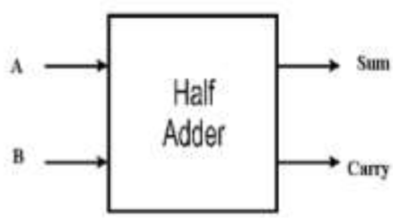
$Y = ABC + AB\bar{C} + A\bar{B}C + \bar{A}B\bar{C}$

$Y = m_7 + m_6 + m_5 + m_2$

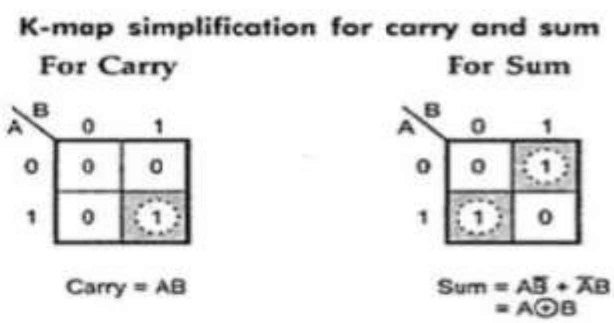
Q. 3 **Attempt any FOUR of the following :** — **16 Marks**

a) **Design half adder circuit using NOR gates only.** — **4M**

Ans :



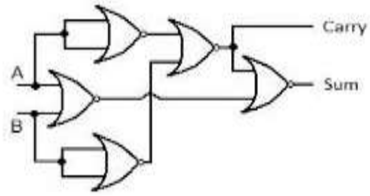
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Truth Table-1M

Kmap-1M

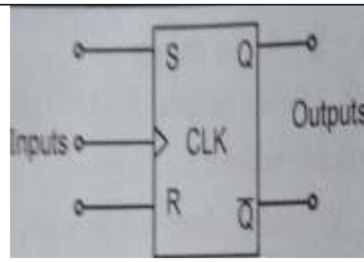
Diagram-2M



b) **Describe edge triggered flip-flop with waveforms.** **4M**

Ans:

Diagram-1M



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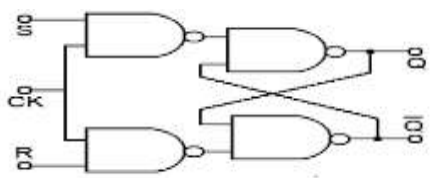


Positive Edge Triggered SR Flip flop

Explanation

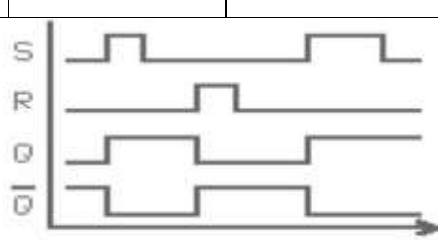
Explaination-1M

Case 1: S=0 & R=0
For S=0 and R=0 there is no change in the state of flip flop
Case 1: S=0& R=1
For S=0 and R=1 the flip flop is reset
Case 1: S=1&R=0
For S=1 and R=0 the flip flop is set
Case 1: s=1& R=1
S=1 and R=1 this is the invalid state of flip flop

Truth Table-1M

Clock	**S**	**R**	**Output**
↑	**0**	**0**	**Qn [No Change]**
↑	**0**	**1**	**0 [Reset]**
↑	**1**	**0**	**1 [Set]**
↑	**1**	**1**	**Invalid State**

Waveform 1M



(Note: Any flip flop using either positive or negative edge trigger can be consider.)

c) **State any four applications of DAC.** — **4M**

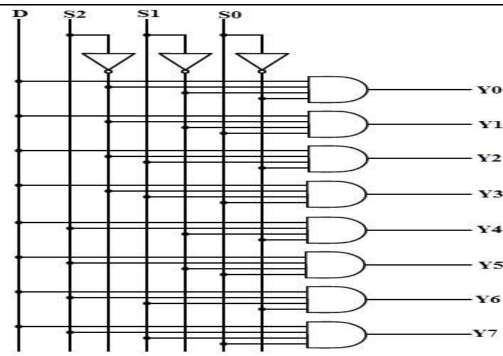
Ans:

Digital Motor Control
Computer Printers
Sound Equipment (e.g. CD/MP3 Players, etc.)
Function Generators/Oscilloscopes
Digital Audio
(Note: Any other applications also can be considered)

4M(1M each)

d) **Draw logic diagram of 1:8 demultiplexer. Write its truth table.** — **4M**

Ans:



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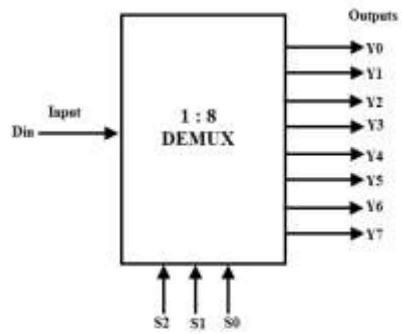


Data Input	Select Inputs			Outputs							
D	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

logic diagram-2M

Truth Table-2M

e) **What is race around condition and how it can be avoided? Explain.** — **4M**

Ans:

Race around Condition: In a JK flip flop the Race Around condition occurs when J=K=1 i.e. when the FF is in the toggle mode.
Elimination of Race around Condition
Race around condition can be avoided using

1. Master Slave Flip Flop.
2. Edge Triggered Flip Flop

Master Slave Flip Flop :
The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the **"master"** and the other as " **slave ".**The slave simply follows the master The master is active for 1 clock period and slave is active for another clock period avoiding the race condition

Edge Triggered Flip Flop :
In edge triggered JK flip flop, the positive/negative clock pulse is present only for a very short time. Hence by the time the changed outputs return back to the inputs of NAND gates , the clock pulse has died down to zero. Hence the multiple toggling cannot take place. Thus the edge triggering avoids the race around condition.

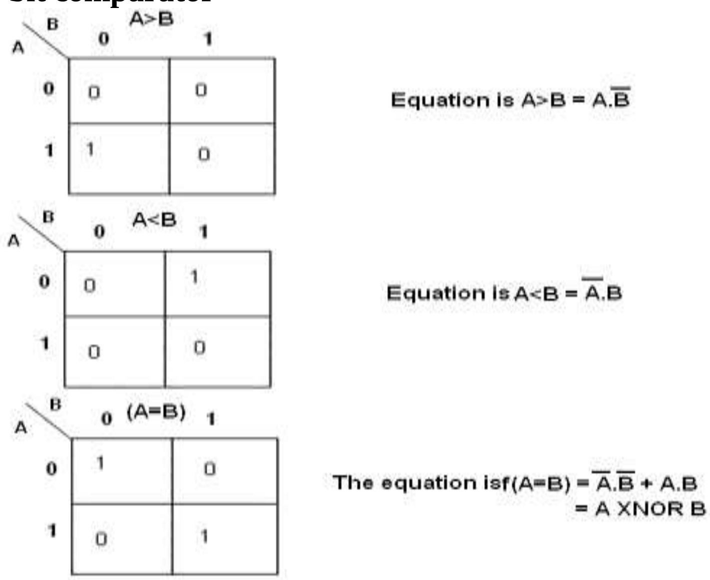
Race around condition-1M
How eliminate-1M
Explaination-2M

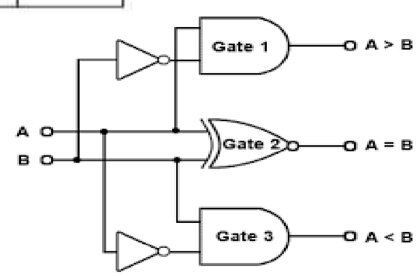
f) **Design 1 bit comparator using K-map & draw its logic diagram.** — **4M**

Ans :

A	B	A>B	A<B	A=B
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

Truth Table of 1 bit comparator



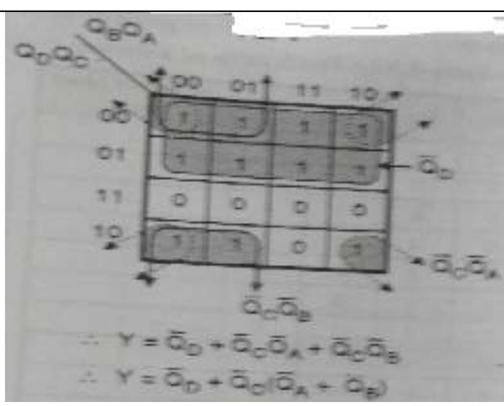


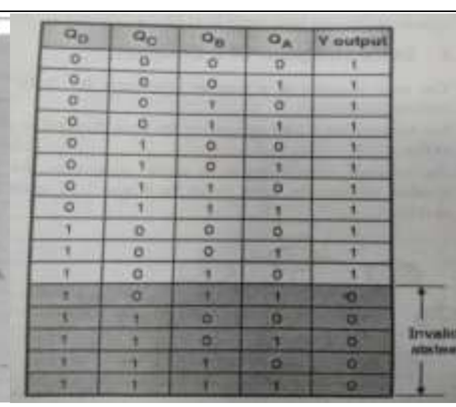
Truth Table-1M, Kmap-1.5M, Diagram-1.5M

Q. 4 (A) Attempt any FOUR of the following: **16 Marks**

(a) Draw the logical diagram of MOD 11 counter and describe its operation with truth table. **4M**

Ans :





Q_D	Q_C	Q_B	Q_A	Y output
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

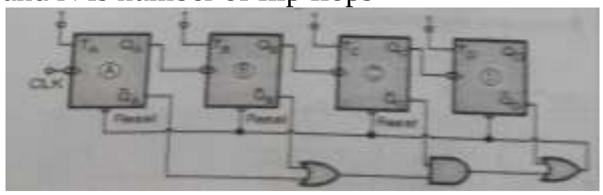
Invalid states

K-Map **Truth Table**

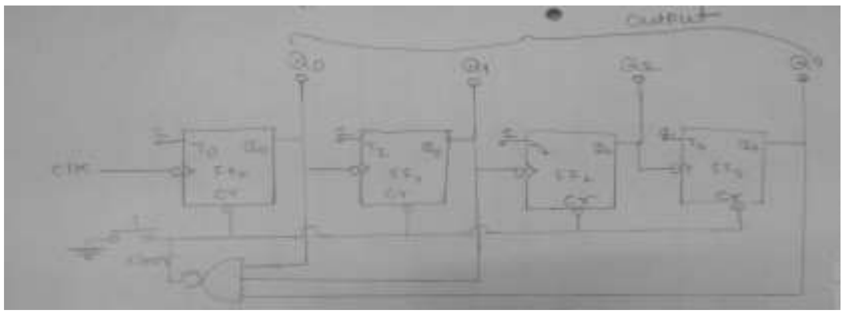
Explanation :

Diaram-2M, Explation -1M, Truth Table-1M (Kmap is optional)

- A MOD-11 counter will have 11 states it will count from 0 to 10 and reset when the count goes above 10
- For constructing a MOD-11 counter we require 4 T type Flip flops as N= 2^M-1 Where M is number of states and N is number of flip flops



OR



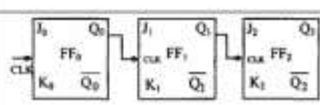
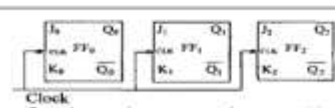
(b) **Compare R-2R and Weighted Register DAC.** **4M**

Ans: (Any 4 point-1M each)

SNo	Weighted Resistor DAC	R-2R Ladder Type DAC
1	Simple Construction	Slightly Complicated
2	Wide range of resistors are required	Resistors pf two values are required
3	One resistor per bit	Two resistors per bit
4	Not easy to expand for more number of bits	Easy to expand for more number of bits

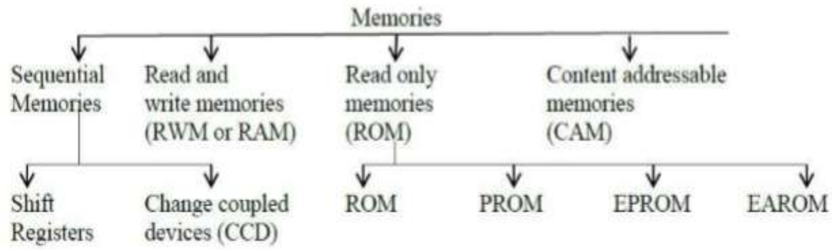
(c) **Differentiate between Asynchronous and Synchronous counter.** **4M**

Ans: (Any 4 point-1M each)

No.	Asynchronous Counter	Synchronous Counter
1.	In an Asynchronous Counter the output of one Flip Flop acts as the clock Input of the next Flip Flop.	In a Synchronous Counter all the Flip Flop's are Connected to a common clock signal.
2.	Speed is Low	Speed is High
3.	Only J K or T Flip Flop can be used to construct Asynchronous Counter	Synchronous Counter can be designed using JK,RS,T and D FlipFlop.
4.	Problem of Glitch arises	Problem of Lockout
5.	Only serial count either up or down is possible.	Random and serial counting is possible.
6.	Settling time is more	Settling time is less
7.	Also called as serial counter	Also called as Parallel Counter
8.		

(d) **Classify memories. Give function of each type.** **4M**

Ans:



The basic fuction of memory device is to store data

- Sequential Memories are storage devices that reads stored data in sequence
- Random Access Memory is a temporary or volatile storage device. Data can be accessed in any order .It is a read write memory
- Read Only Memory is a permanent or Non-Volatile memory device. We can only read but cannot write on it
- Content-addressable memory (CAM) is a special type of computer memory used in certain very-high-speed searching applications

Classification-2M

Explaination-2M

(e) Compare combinational logic system and sequential logic system. **4M**

Ans:

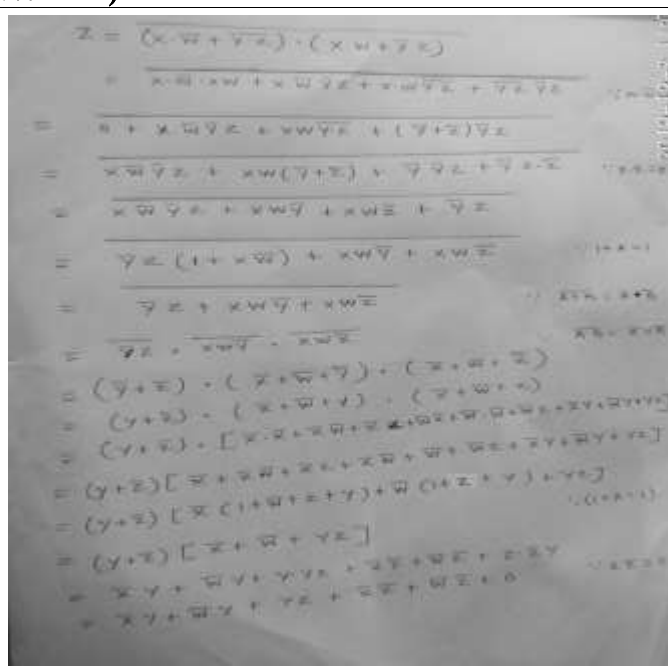
PARAMETERS	COMBINATIONAL CIRCUIT	SEQUENTIAL CIRCUIT
Definition	The output at any instant of time depends upon the input present at that instant of time.	The output at any instance of time depends upon the present input as well as past input and output.
Need of Memory	No memory element required in the ckt	Memory element required to stored bit
Need of clock	Clock input not necessary	Clock input necessary
Examples	E.g. Adders, Subtractors ,Code converters, comparators etc.	E.g. Flip flop, Shift registers, counters etc,
Applications	Used to simplify Boolean expressions, k-map , Truth table	Used in counters & registers

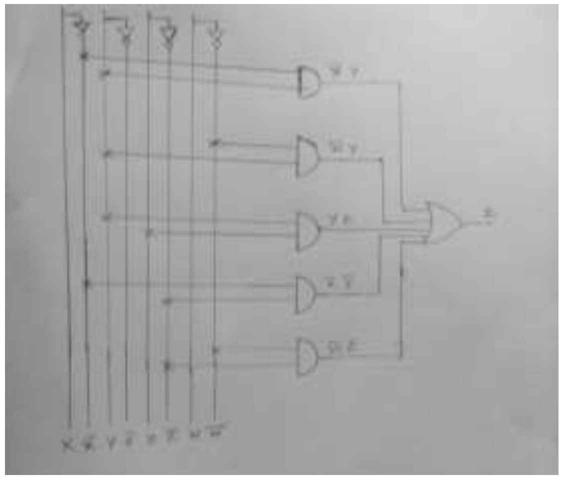
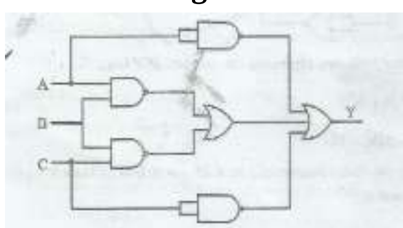
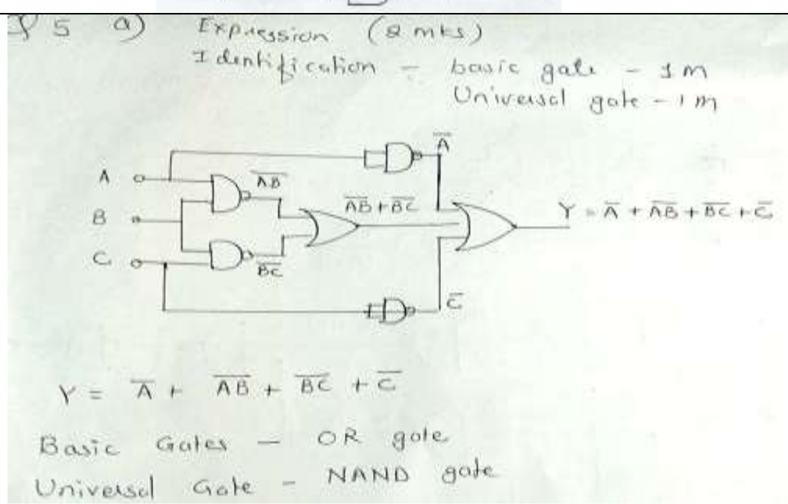
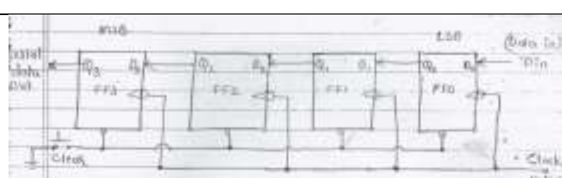
Any 4 point-1M each

f) Simplify following equation using Boolean algebra and draw its circuit diagram: **4M**

$Z = \overline{(X.\overline{W} + \overline{Y}.\overline{Z})\,(X.W + \overline{Y}Z)}$

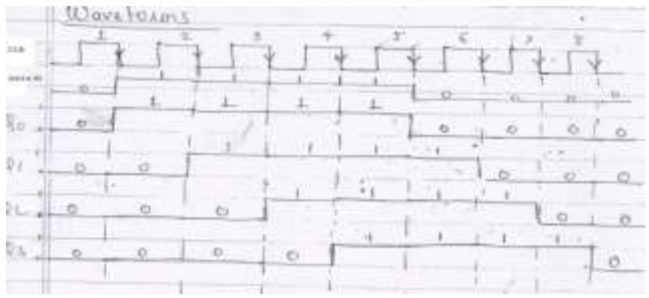
Ans:



			
Q. 5		**Attempt any FOUR of the following:**	**16 Marks**
	(a)	**For the logic circuit shown in figure below, what will be the expression for output Y? Identify the basic gates & universal gates used in ckt.** 	**4M**
	Ans :		**Final output- 2M** **Identification of gate-2M**
	(b)	**Draw and explain SISO with truth table and timing diagram.**	**4M**
	Ans :	 **Description**-As shown a 4 bit SISO shift register consists of 4 D flip-flop, data is fed from first flip-flop and on application of clock pulses the data is shifted from first flip-flop to the	**Diagram 1M** **explanation- 1M,**

last flip-flop, working as serial in and serial out shift register. Let the data be -1111.
The truth table and timing diagram is as shown below

truth table- 1M



timing diagram- 1M

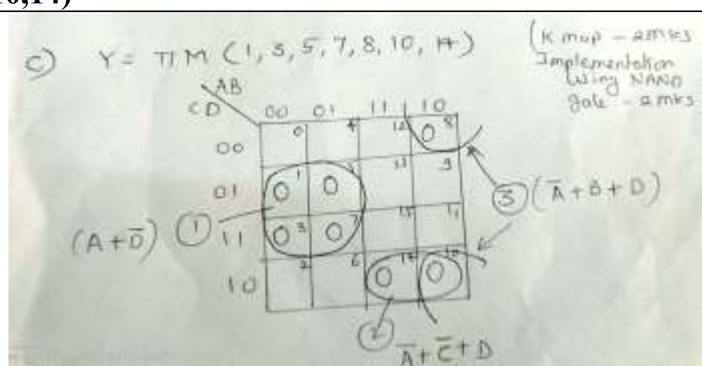
(NOTE: give marks to siso shift right operation also)

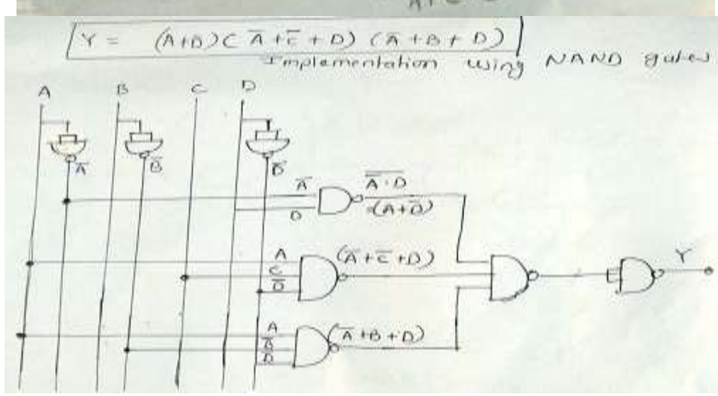
(c) **Reduce the following expression using K-map & Implement it using NAND gates.**

Y=∏M(1,3,5,7,8,10,14)

4M

Ans:



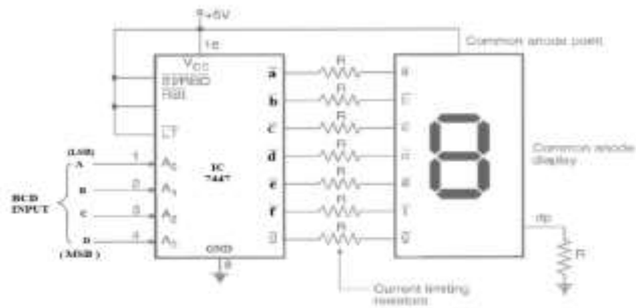


(Note: Implementation using NAND gate using other technique also can be consider)

(d) **Draw & explain block diagram of BCD to seven segment decoder/driver using IC 7447 with its truth table.**

4M

Ans:



1. BCD to 7 segment decoder is a combinational circuit that accepts 4 bit BCD input and generates appropriate 7 segment output.
2. In order to produce the required numbers from 0 to 9 on the display the correct combination of LED segments need to be illuminated.
3. A standard 7 segment LED display generally has 8 input connections, one from each LED segment & one that acts as a common terminal or connection for all the internal segments
4. Therefore there are 2 types of display 1. Common Anode Display 2. Common Cathode Display
5. As the 74LS47 decoder is designed for driving a common-anode display, a LOW (logic-0) output will illuminate an LED segment while a HIGH (logic-1) output will turn it "OFF".
6. For normal operation, the LT (Lamp test), BI/RBO (Blanking Input/Ripple Blanking Output) and RBI (Ripple Blanking Input) must all be open or connected to logic-1 (HIGH).

Truth Table of BCD to seven segment decoder using IC7447(common Anode)

Decimal No.displayed	BCD Inputs				Outputs						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	1	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0

Diagram 2M

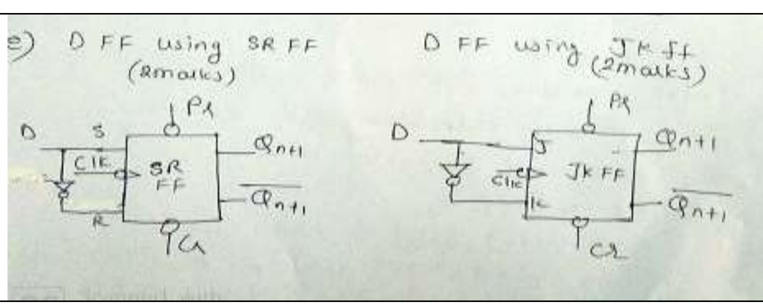
explain 1M

truth table 1M

e) **Draw D flip flop using**
(i) SR flip-flop
(ii) JK flip-flop

4M

Ans:



2M each

(f) **Convert $(6AC)_{16}=(?)_{10}=(?)_2$**

4M

Ans: **2M each**

Convert $(6AC)_{16} = (?)_{10} = (?)_2$ [H→D 2mks, H→B 2mks]

6	A	C
16^2	16^1	16^0

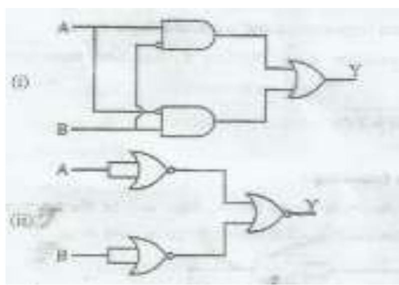
$$\therefore (6AC)_{16} = (6\times16^2) + (A\times16^1) + (C\times16^0)$$
$$= (6\times16^2) + (10\times16^1) + (12\times16^0)$$
$$= 1536 + 160 + 12$$
$$\boxed{(6AC)_{16} = (1708)_{10}}$$

$6 \rightarrow 0110$, $A \rightarrow 1010$, $C \rightarrow 1100$

$$\boxed{\therefore (6AC)_{16} = (011010101100)_2}$$

Q. 6 **Attempt any TWO of the following:** **16 Marks**

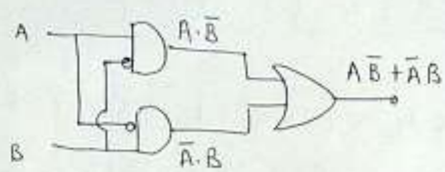
(a) **Find the Boolean expression for logic circuit given below.** **8M**



Ans:

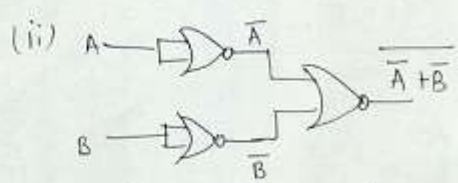
a) (i) – 4 marks
(ii) – 4 marks

(i)



$$\boxed{\therefore Y = A\overline{B} + \overline{A}B}$$

(ii)



$$\boxed{\therefore Y = \overline{\overline{A}+\overline{B}}}$$

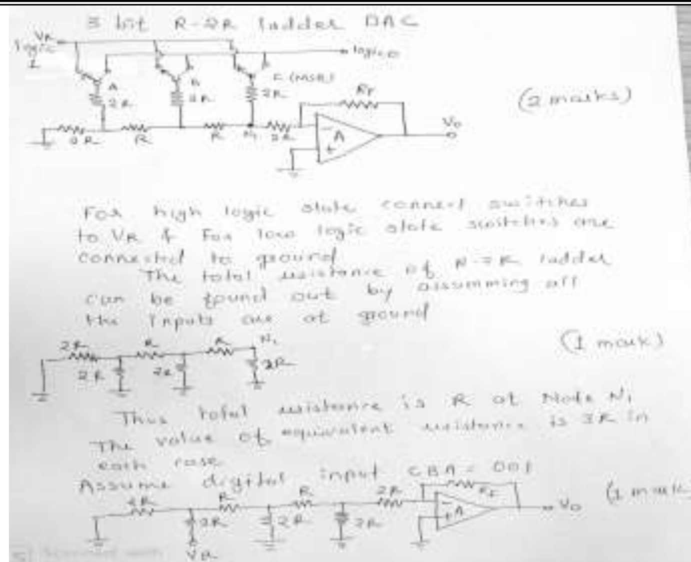
(b) **Convert following expression into standard SOP form.** **8M**

(i)$\overline{A}$+B$\overline{C}\overline{D}$

(ii)A$\overline{B}$C+$B\overline{D}$

	Ans :	b (i) 4 marks (ii) 4 marks (i) $\bar{A} + B\bar{C}\bar{D}$ total variables = 4 (A, B, C, D) missing variables in 1st term = B, C, D missing variable in 2nd term = A $= \bar{A}\cdot 1\cdot 1\cdot 1 + 1\cdot B\bar{C}\bar{D}$ $[\because A\cdot 1 = A]$ (1 mark) $= \bar{A}(B+\bar{B})(C+\bar{C})(D+\bar{D}) + (A+\bar{A})\cdot B\bar{C}\bar{D}$ $[\because A+\bar{A} = 1]$ (1 mark) $= (\bar{A}B + \bar{A}\bar{B})(CD + C\bar{D} + \bar{C}D + \bar{C}\bar{D}) + AB\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D}$ $= \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} +$ $\bar{A}\bar{B}CD + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} +$ (1 mark) $AB\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D}$ $[\because A+A = A]$ $= \bar{A}BCD + \bar{A}BC\bar{D} + \bar{A}B\bar{C}D + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}CD +$ $\bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D}$ (1 mark) = Standard SOP form Q6b) ii) $A\bar{B}C + B\bar{D}$ total variables = 4 (A, B, C, D) missing variables in 1st term = D missing variables in 2nd term = A, C $= A\bar{B}C\cdot 1 + 1\cdot 1\cdot B\bar{D}$ $[\because A\cdot 1 = A]$ (1 mark) $= A\bar{B}C[D+\bar{D}] + (A+\bar{A})B(C+\bar{C})\cdot\bar{D}$ $[\because A+\bar{A} = 1]$ (1 mark) $= A\bar{B}CD + A\bar{B}C\bar{D} + (AB+\bar{A}B)(C\bar{D}+\bar{C}\bar{D})$ (1 mark) $= A\bar{B}CD + A\bar{B}C\bar{D} + ABC\bar{D} + AB\bar{C}\bar{D} +$ $\bar{A}BC\bar{D} + \bar{A}B\bar{C}\bar{D}$ (1 mark) = Standard SOP form	
	(c)	**Draw the circuit diagram of 3 bit R-2R ladder DAC. Obtain its output voltage expression.**	**8M**

Ans :



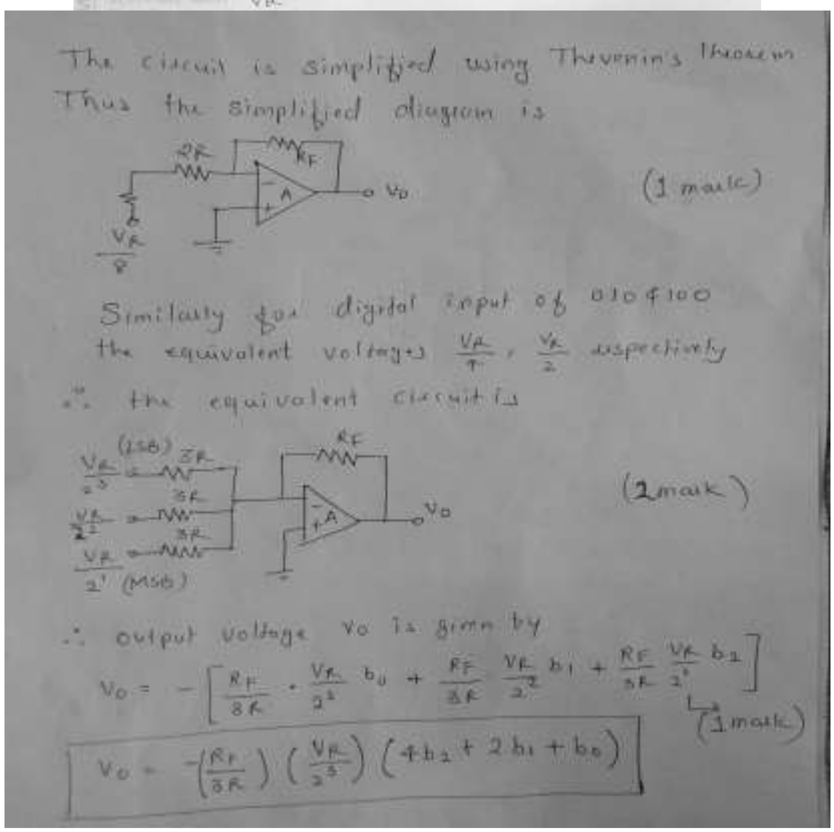
3 bit R-2R ladder DAC

(2 marks)

For high logic state connect switches to VR & for low logic state switches are connected to ground.
The total resistance of R-2R ladder can be found out by assuming all the inputs are at ground

(1 mark)

Thus total resistance is R at Node N1
Thus the value of equivalent resistance is 3R in each case.
Assume digital input CBA = 001 (1 mark)



The circuit is simplified using Thevenin's theorem
Thus the simplified diagram is

(1 mark)

Similarly for digital input of 010 & 100 the equivalent voltages $\frac{V_R}{4}$, $\frac{V_R}{2}$ respectively
∴ the equivalent circuit is

(2 mark)

∴ output voltage Vo is given by

$$V_o = -\left[\frac{R_F}{3R}\cdot\frac{V_R}{2^3}b_0 + \frac{R_F}{3R}\frac{V_R}{2^2}b_1 + \frac{R_F}{3R}\frac{V_R}{2^1}b_2\right]$$

(1 mark)

$$\boxed{V_o = -\left(\frac{R_F}{3R}\right)\left(\frac{V_R}{2^3}\right)(4b_2 + 2b_1 + b_0)}$$

3 BIT R-2R LADDER DAC

$$V_{out} = -\left(\left(R_F/3R\right) V_R \times b_0/2^3 + R_F/3R\ V_R \times b_1/2^2 + R_F/3R\ V_R \times b_2/2^1\right)$$

$$= -\left(R_F/3R\right)\left(V_R/2^3\right)\left(2^2 b_2 + 2^1 b_1 + 2^0 b_0\right)$$

$$= -\left(R_F/3R\right)\left(V_R/2^3\right)\left(4b_2 + 2b_1 + b_0\right)$$