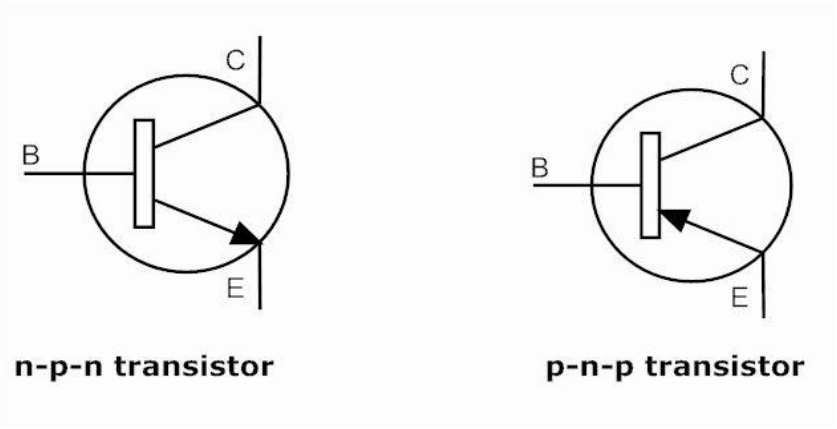
WINTER – 2019 EXAMINATION

Subject Name: Electronic Devices And Circuits **Model Answer** **Subject Code: 22346**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance. Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q. N.	Answer	Marking Scheme
1.		**Attempt any FIVE of the following:**	**10 M**
	a	**Define following parameter for JFET along with mathematical relation:** **(i) Transconductance** **(ii) Amplification factor** **Ans:** **1. Definition of transconductance:** It is given by the ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant drain to source (V_{DS}) .Mathematically , the transconductance , $G_m=\Delta I_D/ \Delta V_{GS.}$ **2. Definition of amplification factor:** It is given by the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate –to-source voltage (ΔV_{GS}) for a constant drain current (I_D). Mathematically, the amplification factor, $\mu= \Delta VDS/\Delta VGS$.	**01 M** **01 M**
	b	**Draw the symbol of** **(i) NPN transistor** **(ii) PNP transistor** **Ans:**  **Fig: Symbol of NPN and PNP transistor**	**02 M**

	c	**List any two applications of crystal oscillator.** **Ans:** **Applications of crystal oscillator:** 1. They are widely used in computers. 2. It is used in digital systems. 3. It is used in instrumentation. 4. It is used in phase-locked loop systems. 5. They are widely used in computers. 6. They are used in modems, marine, telecommunications, in sensors and also in disk drives. Crystal Oscillator is also used in engine controlling, clock and to trip computer, stereo, and in GPS systems.	**02 M**
	d	**Determine the output voltage of regulated power supply using following ICs-** **(i) IC 7915** **(ii) IC 7824** **Ans:** **1. IC7915:** It is a fixed positive linear voltage regulator IC. IC 7915 gives the output of +15V. **2. IC7824:** It is a fixed negative linear voltage regulator IC. IC 7824 gives the output of -24V.	**01 M** **01 M**
	e	**Define load and line regulation.** **Ans**: **Definition of load and line regulation:** **1. Load regulation:** the load regulation is defined as the change in output voltage that will occur per unit change in load current. Load regulation = V_{NL}- $V_{FL}/\Delta I_L$ **2. Line regulation:** The line regulation is the changes in output voltage that will be occur per unit change in the input voltage. Line regulation=$\Delta V_L/\Delta V_S$	**01 M** **01 M**
	f	**Compare linear and non-linear wave shaping circuits on the basis of :** **(i) Components used** **(ii) Applications** **Ans:**	**02 M**

Parameter	**Linear wave shaping circuits**	**Nonlinear wave shaping circuits**
Components used	Which make use of only linear circuit elements such as L,R,C.	Which make use of nonlinear circuit elements such as diodes and transistors.
Applications	Differentiation, Integration.	Clipping, clamping, amplitude limiting.

Table: Comparison of linear and nonlinear wave shaping circuits

g **State Barkhausen criteria for sustained oscillations.** — **01 M**

Ans:

Barkhausen criteria for sustained oscillations:

The Barkhausen criteria should be satisfied by an amplifier with positive feedback to ensure the sustained oscillations.

The Barkhausen criterion states that:

1. The loop gain is equal to unity, that is $\beta A_v = 1$ and
2. The phase shift around the loop is zero or an integer multiple of 2π: $\angle \beta Av = 2\pi$ or 0 the product βA_v is called as the "loop gain". — **01 M**

2. **Attempt any THREE of the following:** — **12 M**

a **Compare RC integrator and differentiator on the basis of:**

(i) Circuit diagram

(ii) O/P voltage equation

(iii) Time constant condition

(iv) Output voltage waveform for square wave input.

Ans:

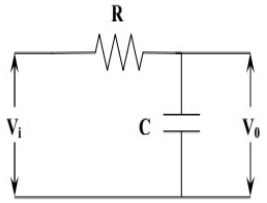
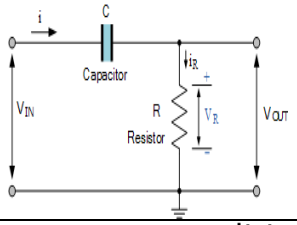
Parameter	RC Integrator	RC Differentiator
Circuit diagram		
Output voltage equation	$V_{out} = \frac{1}{RC}\int_0^t V_{in}\,dt$	$V_{OUT} = RC\frac{dV_{IN}}{dt}$
Time constant condition	T=RC and t >10T	T=RC and t < 0.1T
Output voltage waveform for square wave input	Triangular wave	Narrow pulses

Table: Comparison RC integrator and differentiator — **04 M**

b **Draw and describe working of negative clamper with neat circuit diagram and input /output waveforms.**

Ans:

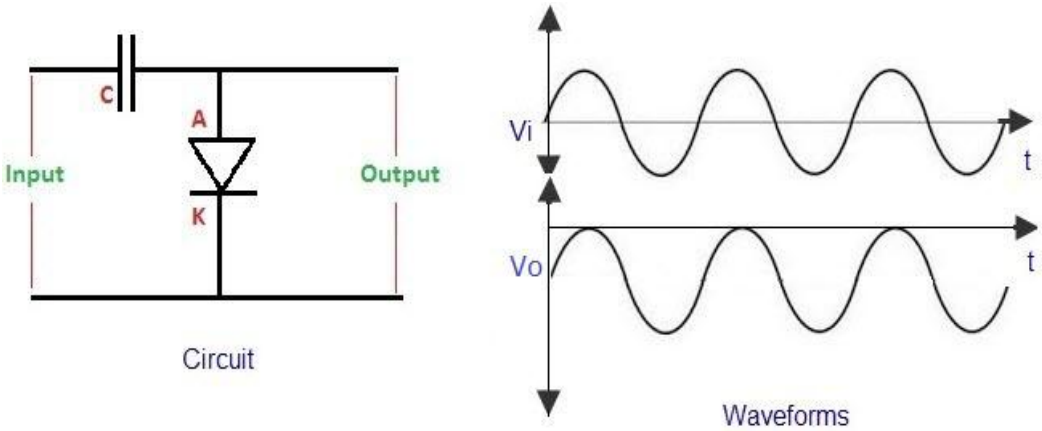
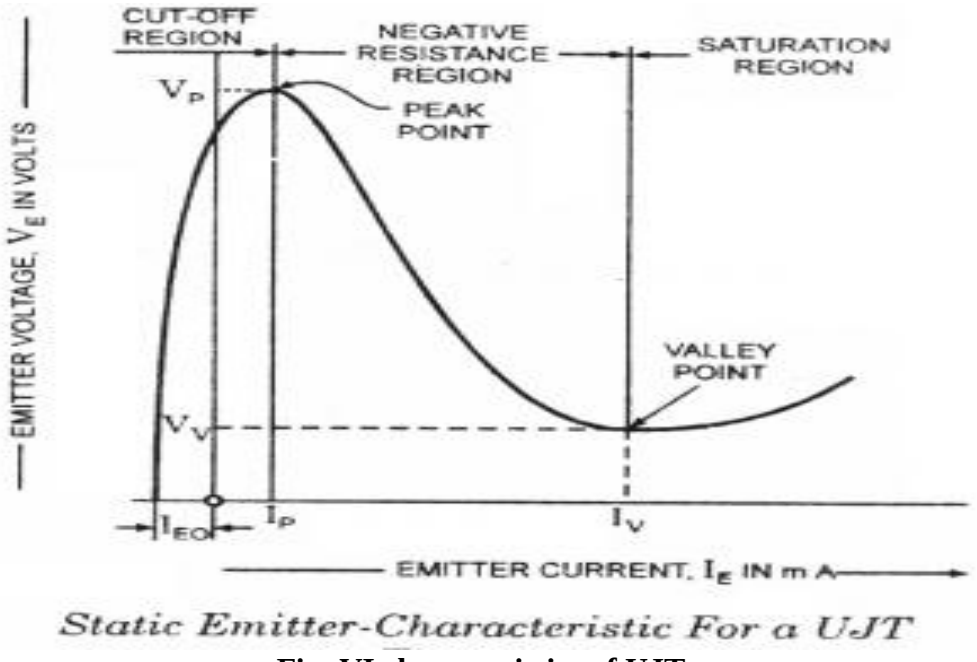


Fig: Negative Clamper — **02 M**

		For negative clamper it is required to clamp the input signal waveform negatively at 0V. Here the diode is forward biased during positive half cycle of the input signal. And as the diode conducts-capacitor gets charged (up to peak value of input supply). During the negative half cycle, the diode is reverse biased and does not conduct and the output voltage become equal to the sum of the input voltage and the voltage stored across the capacitor.	**02 M**
	c	**Derive the relation between α and β of transistor.** **Ans.** **The relation between α and β of transistor:** Common base current gain, α =(Ic / Ie) Common emitter current gain, β=(Ic/ Ib) From transistor current relations, Ie=Ic+Ib **α=Ic/Ie** α=Ic/(Ic+Ib) Dividing numerator and denominator by Ib α=(Ic/Ib)/((Ic/Ib)+(Ib/Ib)) ie, α=β/β+1 **β=Ic/Ib** α=Ic/(Ie-Ic) Dividing numerator and denominator by Ie β=(Ic/Ie)/((Ie/Ie)-(Ic/Ie)) ie, β=α/1-α	**02 M** **02 M**
	d	**Draw VI characteristics of UJT and show its operating regions on it.** **Ans:**  *Static Emitter-Characteristic For a UJT* **Fig: VI characteristics of UJT**	**04 M**
3.		**Attempt any <u>THREE</u> of the following:**	**12 M**
	a	**Compare class A, class B, power amplifiers on the basis of :** **(i) Current flow in terms of cycle** **(ii) Efficiency** **(iii)Distortion** **(iv)Place of Q point** **Ans:**	

Parameters	Class A power amplifier	Class B power amplifier
Current flow in terms of cycle	Current conduction for 360^0	Current conduction for 180^0
Efficiency	50%	78.5%
Distortion	Lowest distortion	High distortion (crossover distortion)
Place of Q point	Q point is on center of a. c. load line	Q point is on cut off point

Table: Compare class A, class B, power amplifiers — **04 M**

b **List types of feedback connections used in amplifiers and derive gain expression for voltage series feedback with neat block diagram**

Ans:

List types of feedback connections used in amplifiers: — **01 M**

1. voltage series feedback
2. voltage shunt feedback
3. current series feedback
4. current shunt feedback

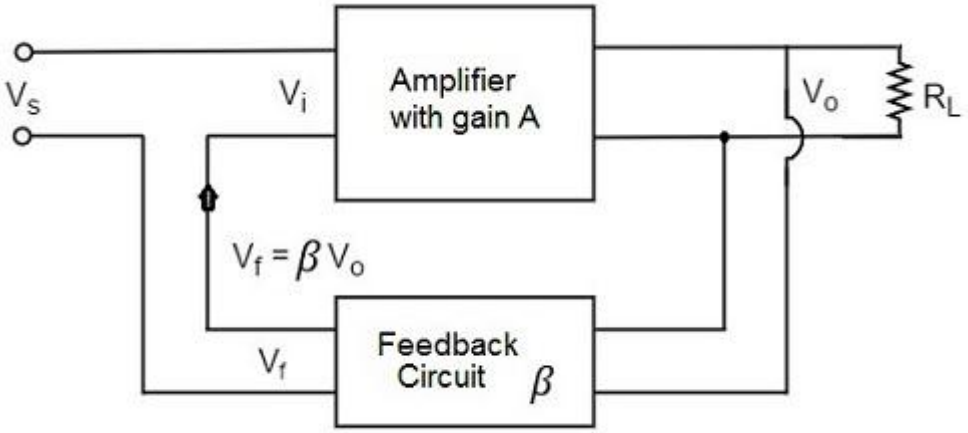


Fig: Block diagram voltage series feedback — **02 M**

Gain expression for voltage series feedback is given by:

$$A_{CL} = \frac{A_v}{1 + A_v B}$$

01 M

Where B is feedback fraction

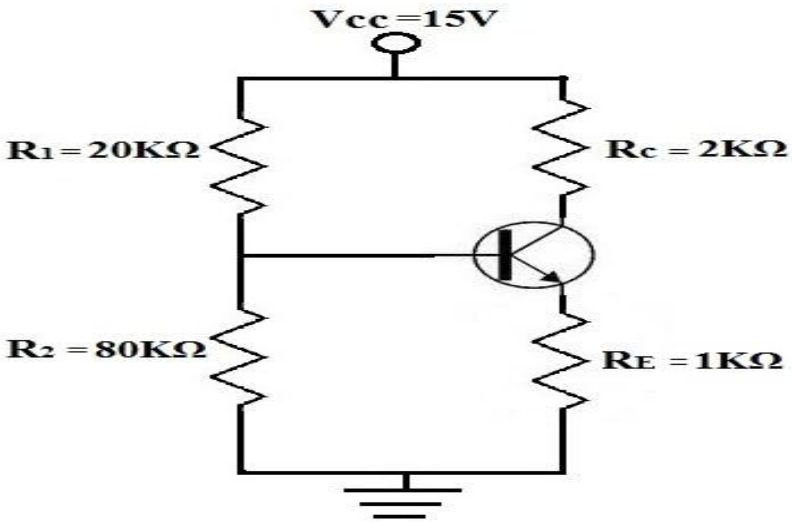
A_V is voltage gain of amplifier without feedback

A_{CL} is voltage gain of amplifier with feedback.

c **Draw and describe working of voltage divider bias used as biasing circuit in BJT.**

Ans:

Voltage Divider Bias Circuit, also known as emitter current bias, is the most stable of the three basic transistor bias circuits. A voltage divider bias circuit is shown in Fig. It is seen that, there is an emitter resistor (R_E) connected in series with the transistor. The total dc load in series with the transistor is (R_C+ R_E), and this total resistance must be used when drawing the dc load line for the circuit. Resistors R_1 and

		R_2 constitute a voltage divider that divides the supply voltage to produce the base bias voltage (V_B). Voltage Divider Bias Circuit are normally designed to have the voltage divider current (I_2) very much larger than the transistor base current (I_B). In this circumstance, V_B is largely unaffected by I_B, so V_B can be assumed to remain constant. $$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$ Referring to Fig. With V_B constant, the voltage across the emitter resistor is also a constant quantity, $V_E = V_B - V_{BE}$ This means that the emitter current is constant, $$I_E = \frac{V_B - V_{BE}}{R_E}$$ The collector current is approximately equal to the emitter current, so I_C is held at a constant level. the transistor collector voltage is, $$V_C = V_{CC} - (I_C R_C)$$ The collector-emitter voltage is, $$V_{CE} = V_C - V_E$$ V_{CE} can also be determined as, $$V_{CE} \approx V_{CC} - I_C(R_C + R_E)$$ Clearly, with I_C and I_B constant, the transistor collector-emitter voltage remains at a constant level.  **Fig: Voltage Divider Bias Circuit**	**02 M** **02 M**
	d	**Draw single stage BJT CE amplifier and describe function of each component used in it.** **Ans:** **Common emitter amplifier circuit elements and their functions:** **1. Biasing Circuit/ Voltage Divider** The resistances R1, R2 and RE used to form the voltage biasing and stabilisation	

circuit. The biasing circuit needs to establish a proper operating Q-point otherwise; a part of the negative half cycle of the signal may be cut-off in the output.

2. Input Capacitor (C1)

The capacitor C1 is used to couple the signal to the base terminal of the BJT. If it is not there, the signal source resistance, Rs will come across R2 and hence, it will change the bias. C1 allows only the AC signal to flow but isolates the signal source from R2

02 M

3. Emitter Bypass Capacitor (CE)

An Emitter bypass capacitor CE is used parallel with RE to provide a low reactance path to the amplified AC signal. If it is not used, then the amplified AC signal following through RE will cause a voltage drop across it, thereby dropping the output voltage.

4. Coupling Capacitor (C2)

The coupling capacitor C2 couples one stage of amplification to the next stage. This technique used to isolate the DC bias settings of the two coupled circuits.

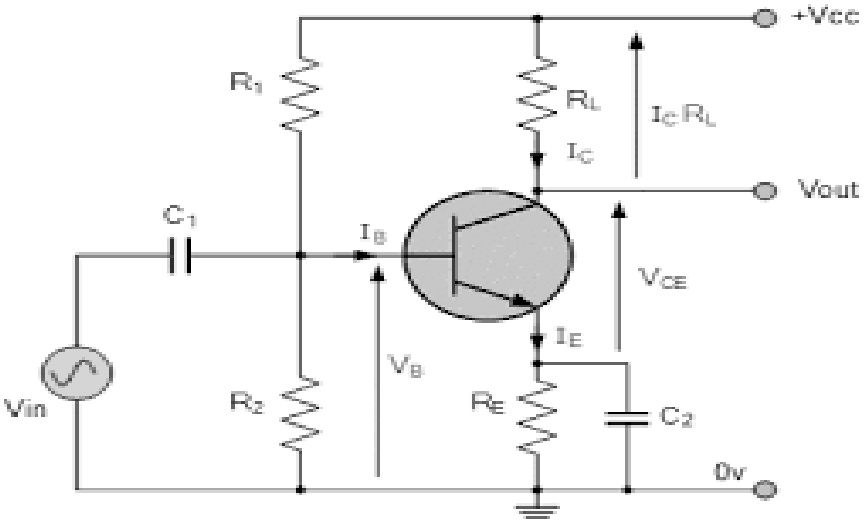


Fig: Single Stage BJT CE amplifier

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4.		**Attempt any <u>THREE</u> of the following:**	**12 M**
	a	**Compare BJT and JFET on the basis of :** **(i) Signal controlling in terms of voltage or current** **(ii) Input resistance** **(iii) Thermal stability** **(iv) Switching speed** **Ans:** **Comparison of BJT with JFET**	**04 M**

Parameters	BJT	JFET
Signal controlling in terms of voltage or current	current	voltage
Input resistance	Low input resistance	High input resistance
Thermal stability	less thermal stability	Better thermal stability
Switching speed	Lower switching speed	high switching speed

Table: Comparison of BJT with JFET

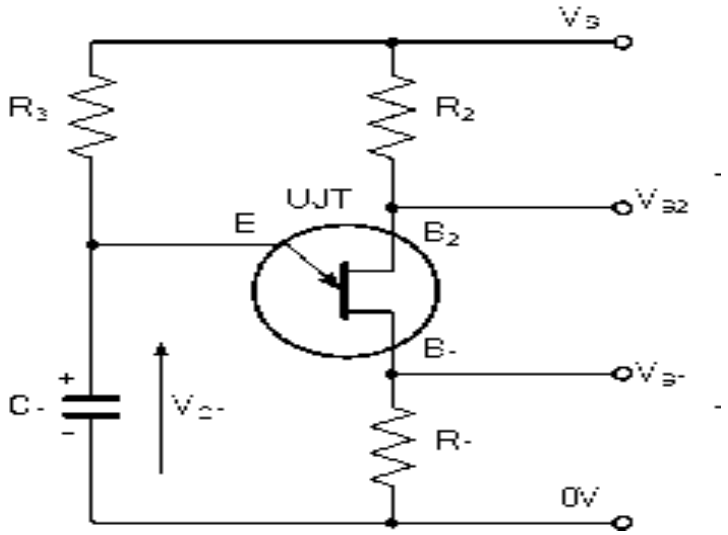
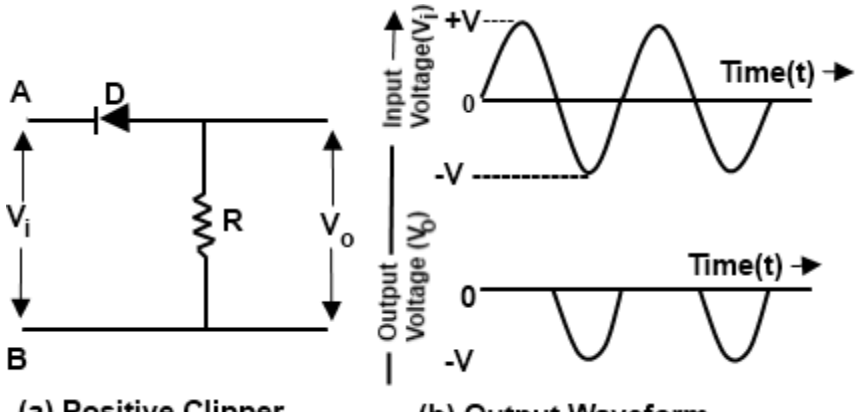
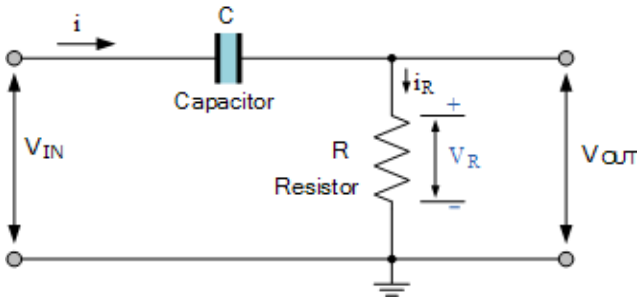
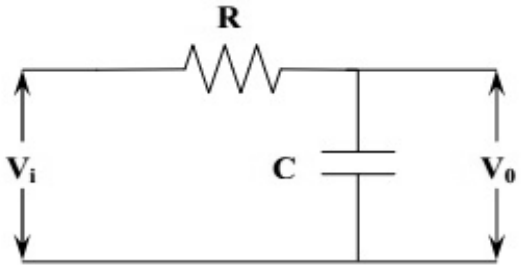
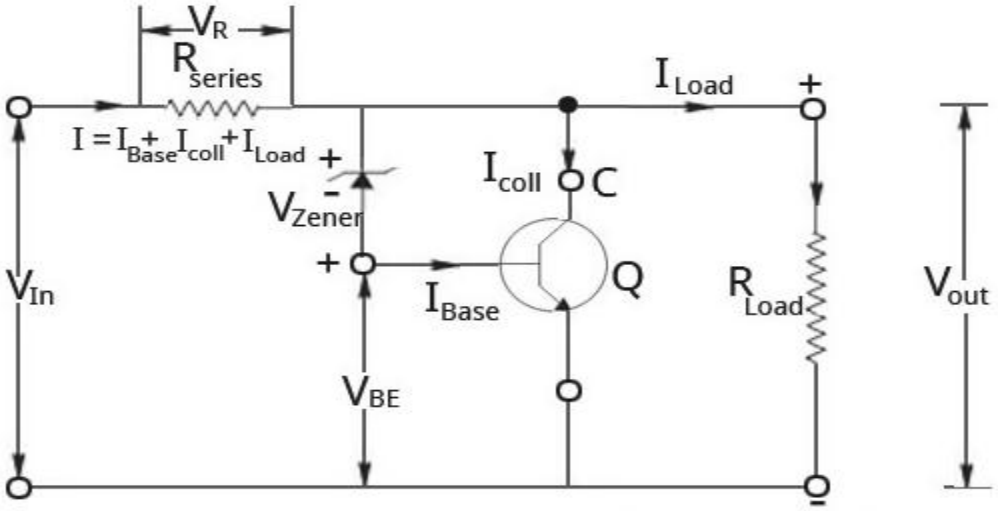
	b	**Describe the operation of UJT relaxation oscillation with neat circuit diagram.** **Ans:**  **Fig: UJT Relaxation oscillator** When a voltage (Vs) is firstly applied, the unijunction transistor is "OFF" and the capacitor C1 is fully discharged but begins to charge up exponentially through resistor R3. As the Emitter of the UJT is connected to the capacitor, when the charging voltage Vc across the capacitor becomes greater than the diode volt drop value, the p-n junction behaves as a normal diode and becomes forward biased triggering the UJT into conduction. The unijunction transistor is "ON". At this point the Emitter to B1 impedance collapses as the Emitter goes into a low impedance saturated state with the flow of Emitter current through R1 taking place. As the ohmic value of resistor R1 is very low, the capacitor discharges rapidly through the UJT and a fast rising voltage pulse appears across R1. Also, because the capacitor discharges more quickly through the UJT than it does charging up through resistor R3, the discharging time is a lot less than the charging time as the capacitor discharges through the low resistance UJT. When the voltage across the capacitor decreases below the holding point of the p-n junction (V_{OFF}), the UJT turns "OFF" and no current flows into the Emitter junction so once again the capacitor charges up through resistor R3 and this charging and discharging process between V_{ON} and V_{OFF} is constantly repeated while there is a supply voltage, Vs applied.	**02 M** **02 M**
	c	**Draw circuit diagram for positive clipper and describe its operation with input and output waveforms.** **Ans:**  (a) Positive Clipper (b) Output Waveform	**02 M**

		Fig. (a) Shows the circuit of a positive clipper.fig (b) Shows input and output waveforms of a positive clipper. During positive half cycle of the input voltage, diode is reverse biased and acts as a open switch. Therefore the applied voltage drops across the diode and none across the resistor .As a result, there is no output voltage during positive half cycle of the input voltage. During negative half cycle of the input voltage, diode is forward biased and acts as a closed switch. Therefore the applied voltage drops across the resistor and none across the diode .As a result, there is output voltage during negative half cycle of the input voltage.	**02 M**
	d	**Identify linear wave shaping circuit used to generate following waveforms and draw the circuit diagram for it.** **(i) Narrow pulses from square wave.** **(ii) Triangular wave from square wave.** **Ans:** **1. Narrow pulses from square wave: RC Differentiator**  **2. Triangular wave from square wave: Triangular wave**  	**01 M** **01 M** **01 M** **01 M**
	e	**Describe controlling action of transistorized shunt regulator with neat circuit diagram.** **Ans:**  **Fig: Transistorized shunt regulator**	**02 M**

		As there is a voltage drop in the series resistance Rseries the unregulated voltage is also decreased along with it. The amount of voltage drop depends on the current supplied t the load Rload. The value of the voltage across the load depends on the Zener diode and the transistor base emitter voltage Vbe. Thus, the output voltage can be written as Vout = Vzener + Vbe = Vin – I R series The output remains nearly a constant as the values of Vzener and Vbe are nearly constant. This condition is explained below. When the supply voltage increases, the output voltage and base emitter voltage of transistor increases and thus increases the base current Ibase and therefore causes an increase in the collector current Icoll (Icoll = β.Ibase). Thus, the supply voltage increases causing an increase in supply current, which intern causes a voltage drop i the series resistance R series and thereby decreasing the output voltage. This decrease will be more than enough to compensate for the initial increase in output voltage. Thus, the output remains nearly a constant. The working explained above happens in reverse if the supply voltage decreases. When the load resistance Rload decreases, the load current Iload increases due to the decrease in currents through base and collector Ibase and Icoll. Thus, there will not be any voltage drop across Rseries and the input current remains constant. Thus, the output voltage will remain constant and will be the difference of the supply voltage and the voltage drop in the series resistance. It happens in reverse if there is an increase in load resistance.	**02 M**
5.		**Attempt any <u>TWO</u> of the following:**	**12 M**
	a	**Draw circuit diagram of Zener diode as voltage regulator and describe its operation for:** **(i) Variable input voltage and constant load resistance.** **(ii) Constant input voltage and variable load resistance.** **Ans:**	**02 M**

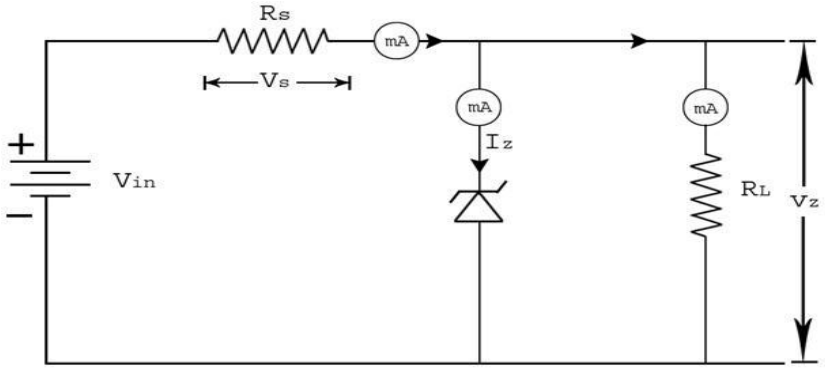


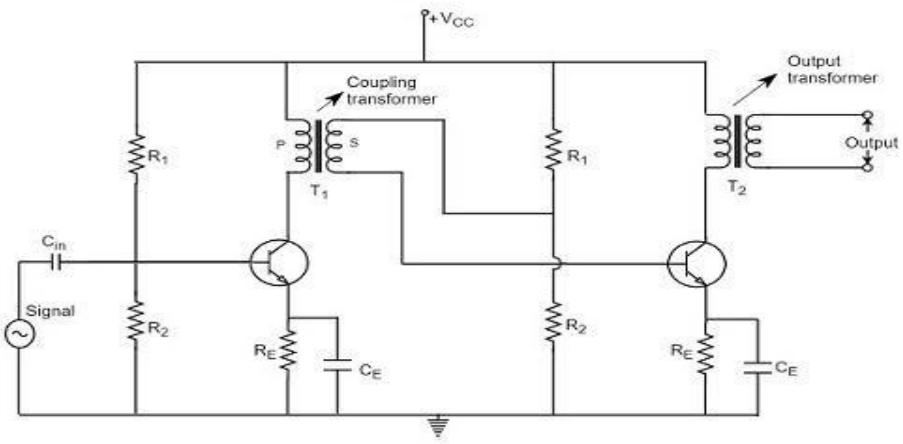
Fig: Zener diode as voltage regulator

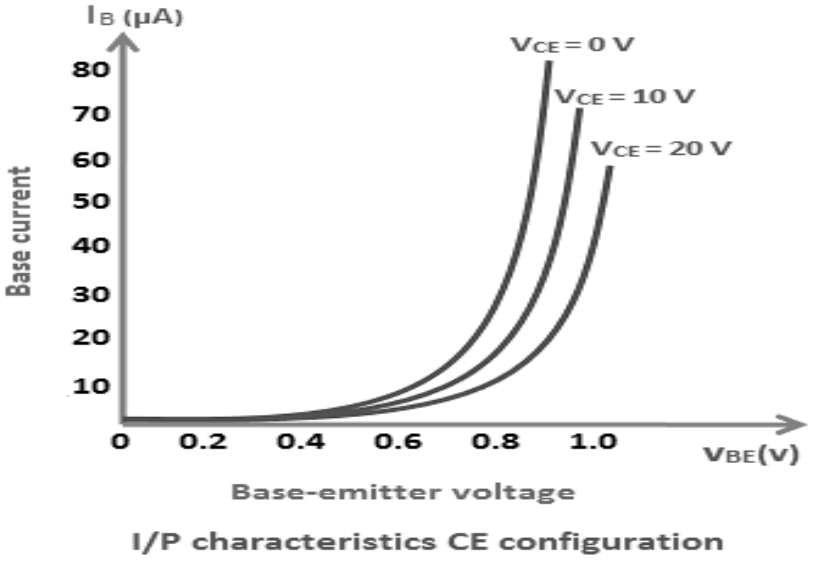
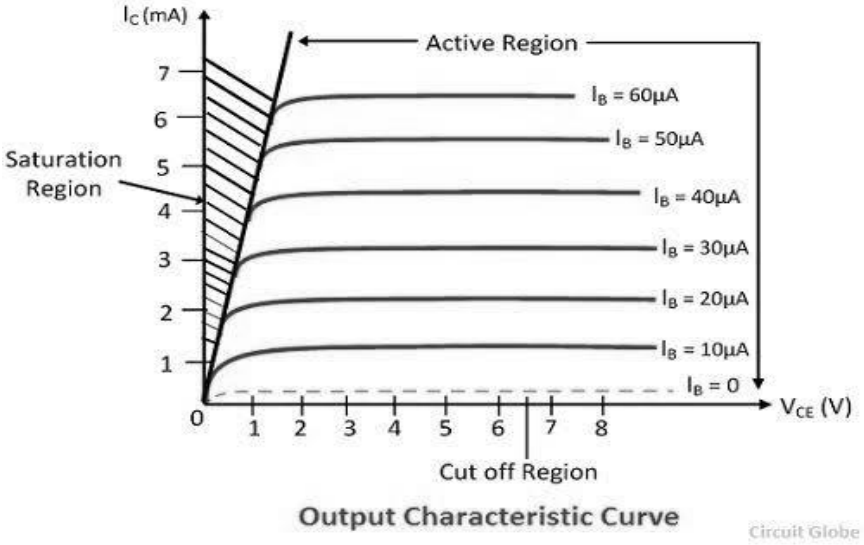
Variable input voltage and constant load resistance:

Here the load resistance is kept fixed and the input voltage varies within the limits. As the input voltage increases, the input current also increase **.**this increases the current through Zener diode, without affecting the current .the increase in input current will also increase the voltage drop across series resistance, thereby keeping the load voltage as constant. On the other hand, if the input voltage is decreased, the input current also decreases .as a result of this, the current through Zener will also decreases. Consequently, the voltage across series resistance will be reduced. Thus the load voltage and load current remains constant. **02 M**

Constant input voltage and variable load resistance:

Here the input voltage is kept fixed and the load resistance varies. The variation

		of load resistance changes the current through it, thereby changing voltage across it. When the load resistance decrease, the load current increases. This causes the Zener current to decreases. As a result of this, the input current and the voltage drop across series resistance remains constant. On the other hand, if the load resistance increase load current decreases. As a result of this, the Zener current increase .this again keeps the value of input current and voltage drop across series resistance as constant.	**02 M**
	b	**Draw circuit diagram for transformer coupled Two Stage Amplifier. Also draw its frequency response and explain it.** **Ans:**  **Fig: Transformer coupled two stage amplifier**  **Fig: Frequency response of transformer coupled two stage amplifier** The figure shows the frequency response of a transformer coupled amplifier. The gain of the amplifier is constant only for a small range of frequencies. The output voltage is equal to the collector current multiplied by the reactance of primary. At low frequencies, the reactance of primary begins to fall, resulting in decreased gain. At high frequencies, the capacitance between turns of windings acts as a bypass condenser to reduce the output voltage and hence gain. So, the amplification of audio signals will not be proportionate and some distortion will also get introduced, which is called as Frequency distortion.	**03 M** **01 M** **02 M**

	c	**Draw input and output characteristics for CE configuration of BJT and show different operating regions on it.** **Ans.**  **Fig: Input characteristics for CE configuration of BJT**  **Fig: Output characteristics for CE configuration of BJT**	**03 M** **03 M**
6.		**Attempt any <u>TWO</u> of the following:**	**12 M**
	a	**Compare CB, CE configurations of BJT on the basis of :** **(i) Current gain** **(ii) Voltage gain** **(iii) Input impedance** **(iv) Output impedance** **(v) Applications** **(vi) Phase shift** **Ans:**	

Parameters	CB	CE
Current Gain	Low	High
Voltage Gain	High	Low
Input Impedance	Low	High
Output Impedance	High	Low
Applications	Used as a cascade stage to isolate output voltage signal.	Used in general purpose amplifier designs
Phase Shift	0^o	180^o

Table: Comparison of CB, CE configurations of BJT

06 M

b **Describe working of N-ch JFET with neat circuit diagram. Also draw its drain characteristics with labeled operating regions on it.**

Ans:

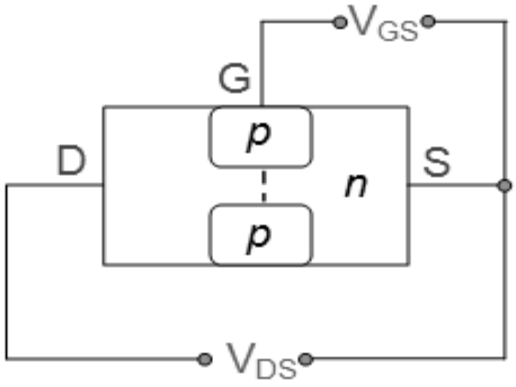


Fig: N-ch JFET

02 M

In n-channel JFET, the majority charge carriers will be the electrons as the channel formed in-between the source and the drain is of n-type. And the working of this device depends upon the voltages applied at its terminals.

Case I - Consider the case where no voltage is applied to the device i.e. $V_{DS} = 0$ and $V_{GS} = 0$. At this state, the device will be idle and no current flows through it i.e. $I_{DS} = 0$.

Case II-Now consider that the drain terminal of the device is connected to the positive terminal of the battery while its negative is connected to the source i.e. V_{DS} = +ve. However let the gate terminal remain at unbiased state, which means $V_{GS} = 0$. At this instant, the electrons within the n-substrate of the device start moving towards the drain being attracted by the positive force exerted by the battery. At the same time, the electron will also be repelled from the source as it is connected to the negative terminal of the voltage supply. This results in a net flow of current from drain to source

02 M

Further, it is seen that the increase in V_{DS} I creases the current flowing through the device at an initial state which can be termed to be JFET's Ohmic region. However, it is to be noted that the increase in V_{DS} also causes an increase in the width of the depletion regions surrounding the pn junctions. This in turn causes the channel width to reduce, thereby increasing its resistance. This phenomenon continues till both of the depletion regions grow up to an extent wherein they almost seem to touch each other, a condition referred to as pinch-off. The corresponding value of V_{DS} is referred to as pinch-off voltage, V_P. Nevertheless, even in this case, a narrow channel with high current density exists within the device due to which IDS will get saturated to a level of I_{DSS} as indicated in Figure 2.

It is this behavior of the JFET which causes it to behave as a constant current source.

Case III Next, let us add the voltage source at the gate terminal such that the gate is negative w.r.t source i.e. V_{GS} = -ve while V_{DS} is +ve. In this case, the device behaves in a way very-similar to that in Case II, but for a lower value of V_{DS}. This means that the pinch-off and the saturation occur quite earlier and are decided by the negative potential applied at the gate i.e. more negative the V_{GS}, earlier the pinch-off due to which earlier will be the saturation, reducing I_{DSS} (Figure 3). As the phenomenon continues, it is seen that a condition arises wherein the saturation level of the drain-to-source current I¬DS occurs right for a value of 0 mA. This means that there is no current flow through the device and essentially the device will turn OFF. The value of V_{DS} for which this happens will be nothing but the negative pinch-off voltage i.e. V_{DS} = - V_P.

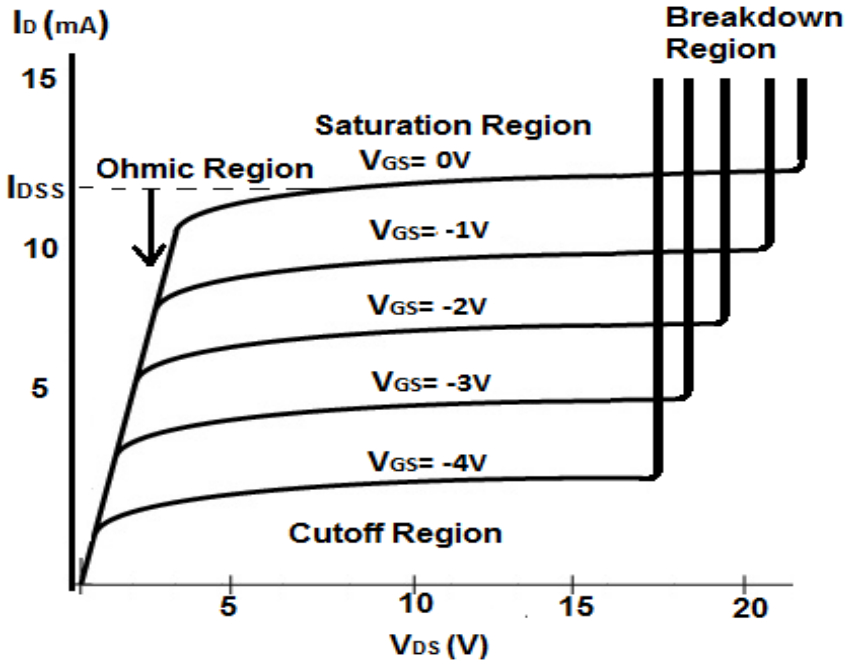


Fig: Drain characteristics curve

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c **Draw neat circuit diagram for class B push pull amplifier and describe its working with output current and voltage waveforms.**

Ans:

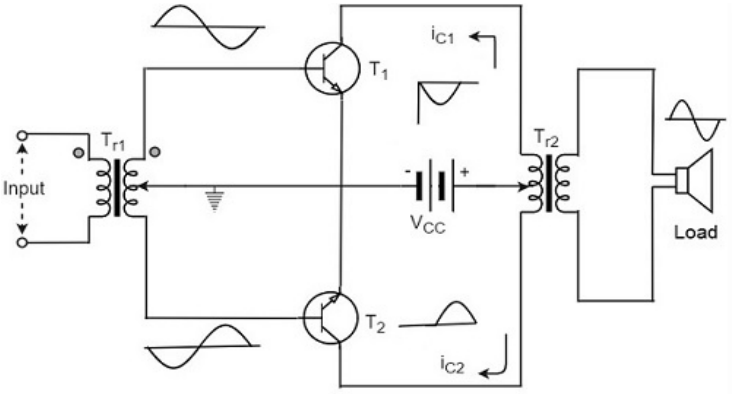
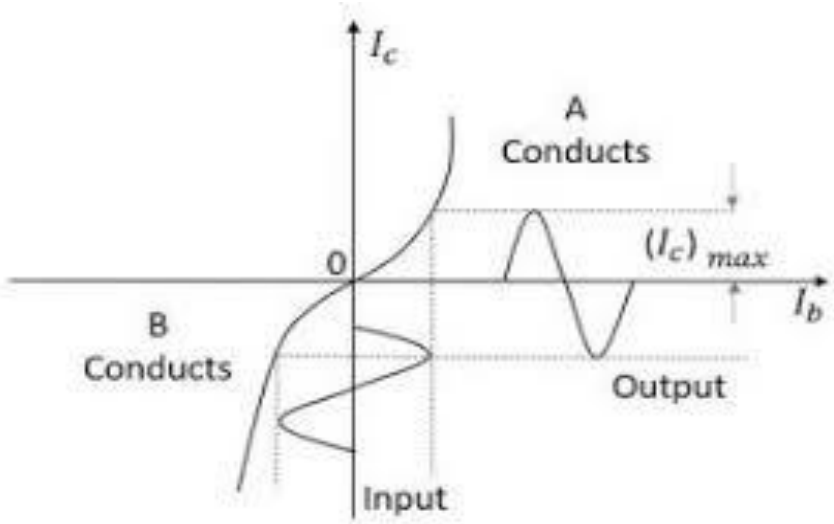


Fig: Class B push pull amplifier

02 M

The circuit of class B push-pull amplifier shown in the above figure clears that both the transformers are center-tapped. When no signal is applied at the input, the transistors T_1 and T_2 are in cut off condition and hence no collector currents flow. As

		no current is drawn from V_{CC}, no power is wasted. When input signal is given, it is applied to the input transformer T_{r1} which splits the signal into two signals that are 180^o out of phase with each other. These two signals are given to the two identical transistors T_1 and T_2. For the positive half cycle, the base of the transistor T_1 becomes positive and collector current flows. At the same time, the transistor T_2 has negative half cycle, which throws the transistor T_2 into cut-off condition and hence no collector current flows.	**02 M**
		 **Fig: Waveforms of output current and voltage**	**02 M**