MODEL ANSWER

SUMMER– 18 EXAMINATION

Subject Title: Linear Integrated Circuit Subject Code: 17445

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q1. a) Attempt any SIX of the following: **12**

i. Define:

1. Slew rate

2. CMRR

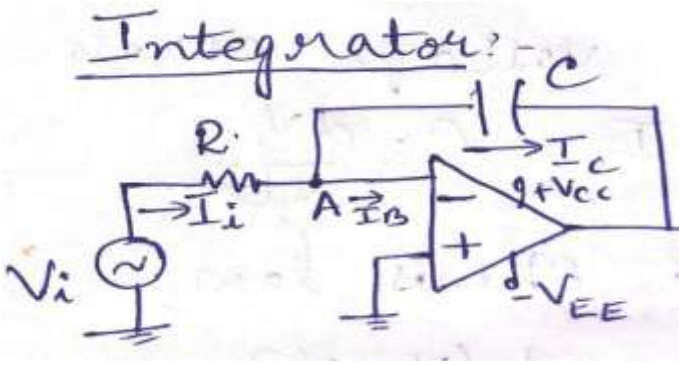
Ans : 1M for each definition

1. **Slew rate:** It is defined as the maximum rate of change of output voltage per unit time.
S.R.= $\Delta Vo / \Delta t$, Unit = V/μs.

2. **CMRR** : It is defined as the ratio of differential mode gain to the common mode gain. It is the ability of an amplifier to reject the common mode signals such as noise. Expressed in dB.

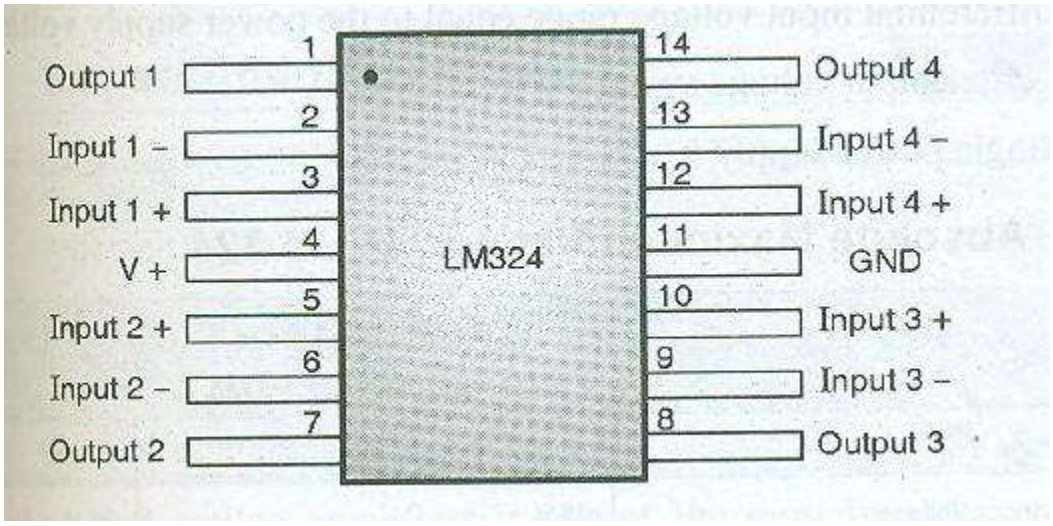
ii) Draw circuit of basic integrator using Op-amp.

Ans: 2M- correct diagram



iii) Draw pin diagram of IC LM-324

Ans: 2M- correct diagram



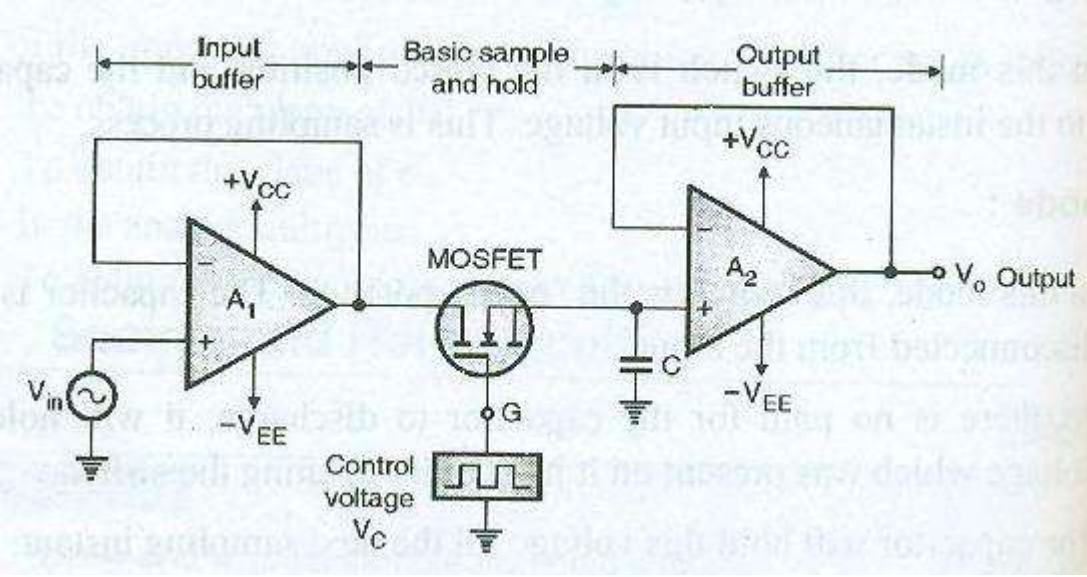
iv) State the need of signal processing (any two points)

Ans: Relevant Correct Explanation – 2 M

1. In an instrumentation system, a transducer is used for sensing various parameters. The output of transducer is an electrical signal proportional to the physical quantity sensed such as pressure, temperature etc. However the transducer output cannot be used directly as an input to the rest of the instrumentation system.
2. In many applications, the signal needs to be conditioned and processed. The signal conditioning can be of different types such as rectification, clipping, clamping etc. Sometimes the input signal needs to undergo certain processing such as integration, differentiation, amplification etc.
3. For example if we want to send temperature information to computer/microcontroller so that computer /microcontroller could monitor, control or change room temperature. For this we need signal processing.

v) Draw sample and hold circuit using Op-amp.

Ans: 2M- correct diagram



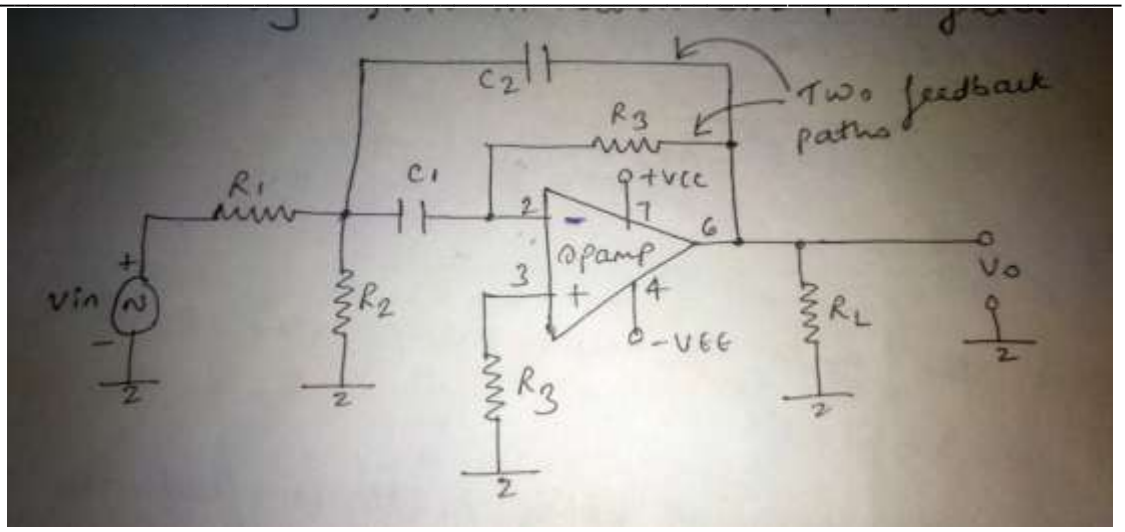
vi) Give classification of filters.

Ans: 2M- correct classification

1) On the basis of component used- active and passive filters.
2) On the basis of frequency range- AF (audio frequency) and RF (radio frequency) filters.
3) On the basis of frequency response filters- high pass, low pass, band pass and band reject filters.
4) On the basis of nature of pass band and stop band- narrow band pass, wide band pass, narrow band reject and wide band reject filters.

vii) Draw circuit diagram of narrow band pass filter using Op-amp.

Ans: 2M- correct diagram



viii) State functions of following pins of : IC 555.

1. Threshold

2. Discharge

Ans: 1M each

1. Threshold: This is non- inverting terminal of comparator C1 which monitors the voltage across the external capacitor. When the voltage at this pin is greater than or equal to 2/3 VCC, the output of comparator C1 goes high which in turn switches the output of the timer low.

2. Discharge: This pin is connected internally to collector of transistor Q1.When the output is high, Q1 is OFF and acts as open circuit to external capacitor connected between pin 7 and ground. On the other side when the output is low, Q1 is ON and acts as short circuit, shorting the external capacitor to ground.

b) Attempt any TWO of the following: 8

i. Describe the function of intermediate stage and output stage of Op-amp with its block diagram.

Ans: Block Diagram- 2Marks, Function of each block– 1 mark

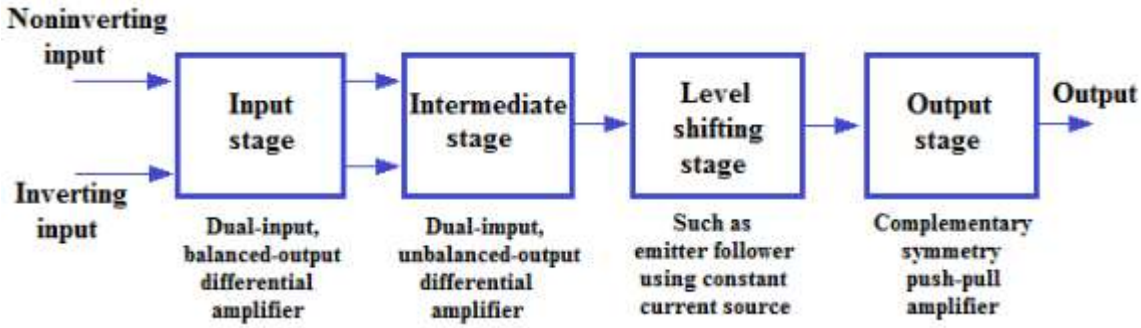


Fig: Block diagram of OP- AMP

1. **Intermediate stage:** This stage uses dual input unbalanced output differential amplifier. This stage provides additional gain, CMRR and isolation.

2. **Output stage:** This stage uses complementary symmetry push pull amplifier. This stage provides low output resistance and hence increases the current supplying capability of op-amp and also this stage increases the output voltage swing.

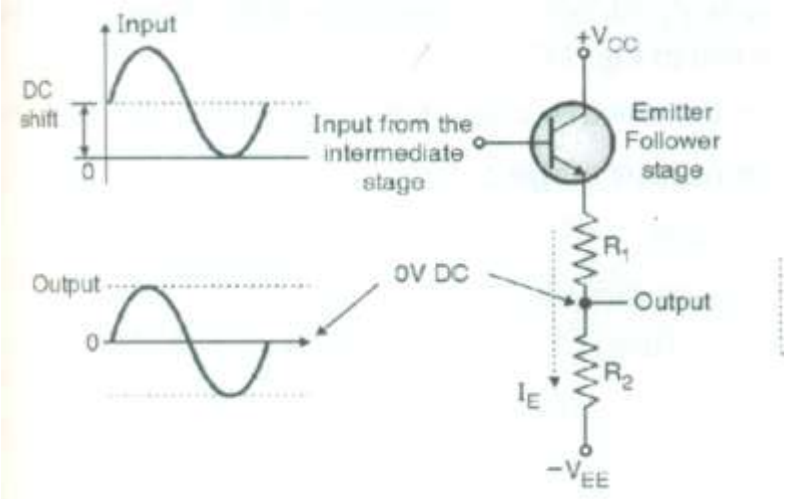
ii. State ideal and practical values of any four parameters of Op-amp.

Ans: Ideal parameter – 2M, practical parameter- 2M (any 4 parameters)

Sr. no	Parameter	Ideal values	Typical Practical values
1	Voltage gain	∞	$2* 10^5$
2	Input resistance	∞	2MΩ
3	Output resistance	0Ω	75Ω
4	Bandwidth	∞	1MHz
5	CMRR	∞	90 dB
6	SVRR	0	150 µV/V
7	Slew rate	∞	0.5V/µs
8	Input offset voltage	0V	6mV
9	Output offset current	0 A	200nA

iii. Draw the circuit diagram of level shifting and explain.

Ans: 2**M- correct diagram, 2 mks explanation**



Level shifting stage is used to bring the dc level to zero volts w.r.t. ground.

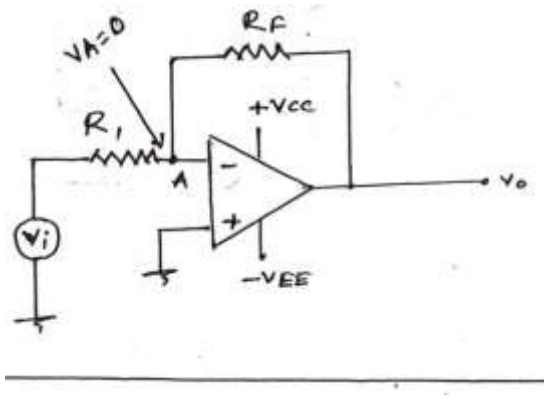
Explanation:-Op-amp is a direct coupled amplifier, So when input is zero or at ground potential ,the output of op-amp will be at some positive DC level which is an error voltage called as offset voltage . So in order to pull this o/p DC offset voltage to zero, the DC level shifter is used.

Q2. Attempt any FOUR of the following: 16

a) Explain the concept of Virtual ground and virtual short with reference to Op-amp.

Ans: 2M- for each

Virtual ground concept:-In circuit point VA is virtual ground. Figure shows inverting amplifier using op-amp. In this circuit non-inverting terminal is connected to the actual ground. Due to this potential of inverting terminal become zero. Thus, inverting terminal is not actually connected to the ground. There after its potential is zero. Thus point VA is known as virtual ground point. This phenomenon of having zero potential without actually grounding is known as virtual ground concept.



Virtual short concept:- For op-amp in non-inverting , non-inverting terminal is connected to input while inverting terminal is grounded. Vd should be zero (0) , so as non-inverting terminal is at Input signal potential ,the inverting terminal is also assumed to be input signal potential ie Vnoninverting = Vinverting. This concept is called as virtual short concept.

b) Compare open-loop and closed loop configuration of Op-amp(any four points).

Ans: 1M –each correct point(any four)

Sr. No	Parameters	Open loop	Closed Loop
1	Feedback	No feedback is used.	Positive or negative feedback is used.
2	Input resistance	Very high	Depends on the circuit
3	Output resistance	Low	Very low
4	Bandwidth	Bandwidth is low	Bandwidth is high
5	Gain	Voltage gain is very high	Voltage gain is low as compared to open

			loop.
6	Application	Comparator ,zero crossing detector	It is used in linear amplifier, oscillator etc

c) Derive expression for gain of closed loop inverting amplifier.

Ans: Diagram: 2M; Derivation:2M

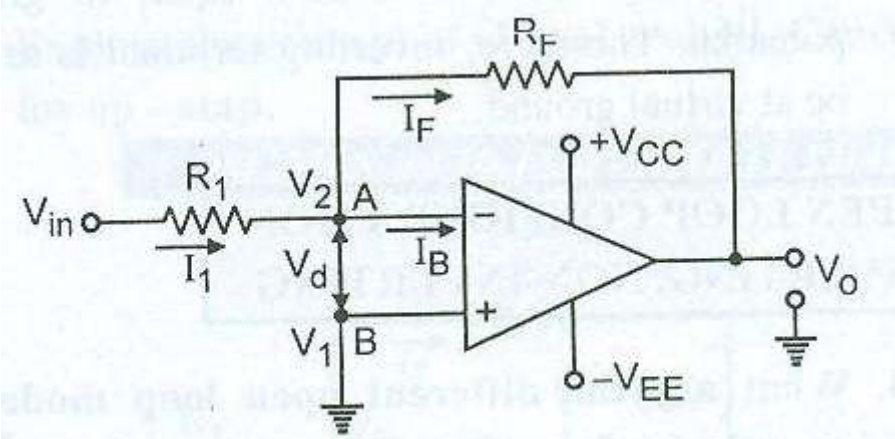


Fig. OP-Amp as an inverting amplifier

As input signal Vin is applied to inverting input, hence it is called as inverting amplifier and non- inverting terminal is grounded. A negative feedback is provided from output to inverting terminal through RF (Feedback resistor)

Vo= output voltage, Vin= input voltage, RF= Feedback resistor, R1= Input resistor.

(A) Derivation:

Apply KCL at node 'A', we get,

$I_1 = I_B + I_f$ — (1)

But, $R_{in} = \infty$

$\therefore I_B = 0$

$\therefore I_1 = I_f$

$\therefore \frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_o}{R_f}$

According to virtual ground condition,

$V_1 = V_2 = 0$

$\therefore \frac{V_{in}}{R_1} = \frac{-V_o}{R_f}$

$\therefore \boxed{V_o = -\left(\frac{R_f}{R_1}\right) V_{in}}$ — (2)

$\therefore \boxed{A_V = \frac{V_o}{V_{in}} = -\frac{R_f}{R_1}}$ — (3)

where, A_V = closed loop voltage gain

d) Derive the expression for output of differentiator with neat circuit diagram.
Ans: Diagram: 2M; Derivation: 2M

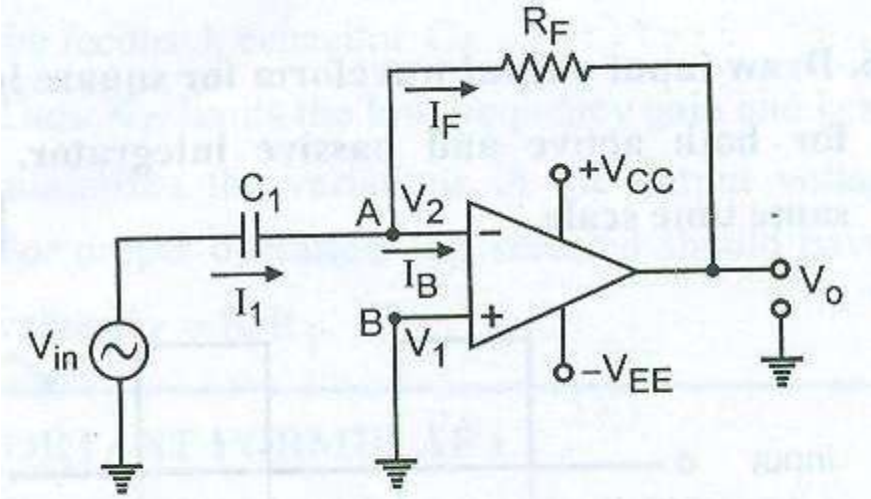


Fig. Circuit diagram of differentiator

Applying KCL at node 'A'

$I_1 = I_B + I_f$

$\therefore R_{in} = \infty, I_B = 0$

$\therefore I_1 = I_f$

$$C_1 \frac{d}{dt}(V_{in} - V_2) = \frac{V_2 - V_o}{R_f}$$

Due to virtual ground condition

$V_1 = V_2 = 0$

$$\therefore C_1 \frac{d}{dt} V_{in} = -\frac{V_o}{R_f}$$

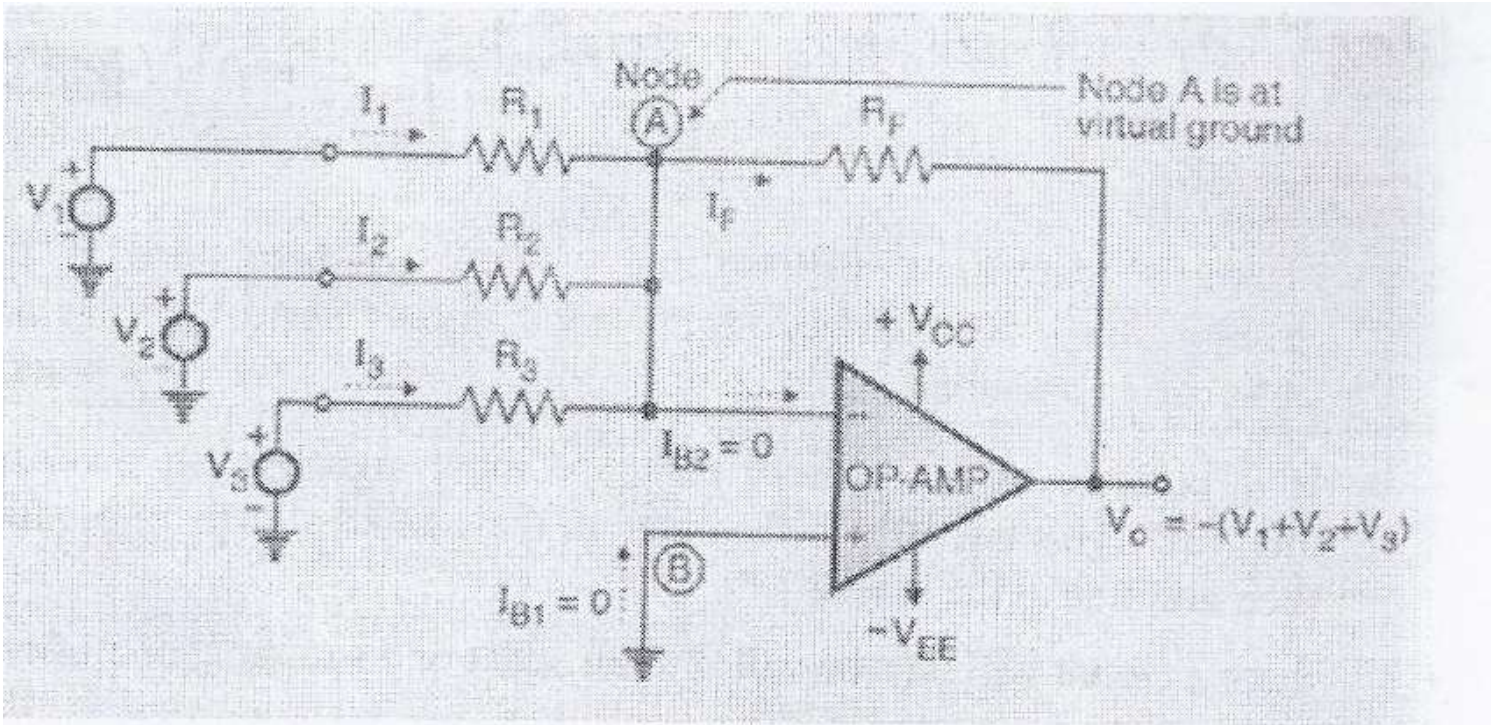
$$\therefore V_o = -R_f C_1 \frac{d}{dt} V_{in}$$

Negative sign indicates that it is an inverting amplifier and $V_o \propto \frac{d}{dt} V_{in}$.

e) Design and draw the circuit for the following operation using Op-amp.

Vo = - (V1+V2+V3)

Ans: 3M- designing,1M- diagram.



Inverting amplifier

Apply KCL at node A

$$I_1 + I_2 + I_3 = I_{B2} + I_F$$

But $R_i = \infty$, $I_{B2} = 0$ and $V_A = V_B = 0$ due to virtual ground concept.

hence $I_1 + I_2 + I_3 = I_F$ ⟶ (1)

From the input side

$$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1} \quad \text{as } V_A = 0$$

$$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2}{R_2} \quad \& \quad I_3 = \frac{V_3 - V_A}{R_3} = \frac{V_3}{R_3}$$

from the output side,

$$I_F = \frac{V_A - V_O}{R_F} = -\frac{V_O}{R_F}$$

Substituting these values in eqn. (1)

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_O}{R_F}$$ consider $R_F = R_1 = R_2 = R_3 = R$

$$V_O = -(V_1 + V_2 + V_3)$$

Thus the output voltage is the negative sum of the input voltage . Therefore this circuit is called as inverting adder or inverting summing amplifier

f) Suggest Op-amp based circuit to convert rectangular to sawtooth wave and draw the circuit diagram with input and output waveform.

Ans: 1M- circuit name, 2M-circuit diagram, 1M- waveform

The circuit which can convert the rectangular wave to saw tooth wave is an Integrator circuit. Diagram and waveform for the same is as shown below.

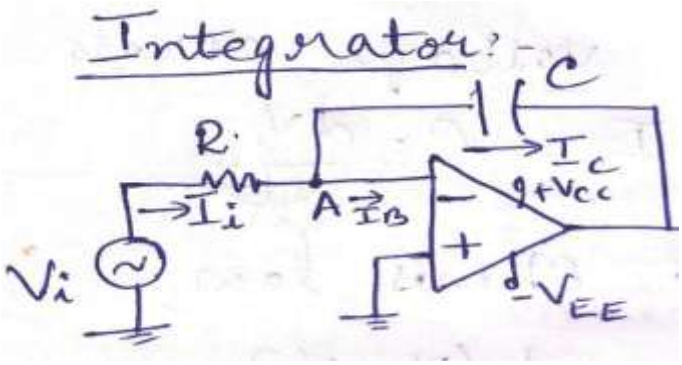
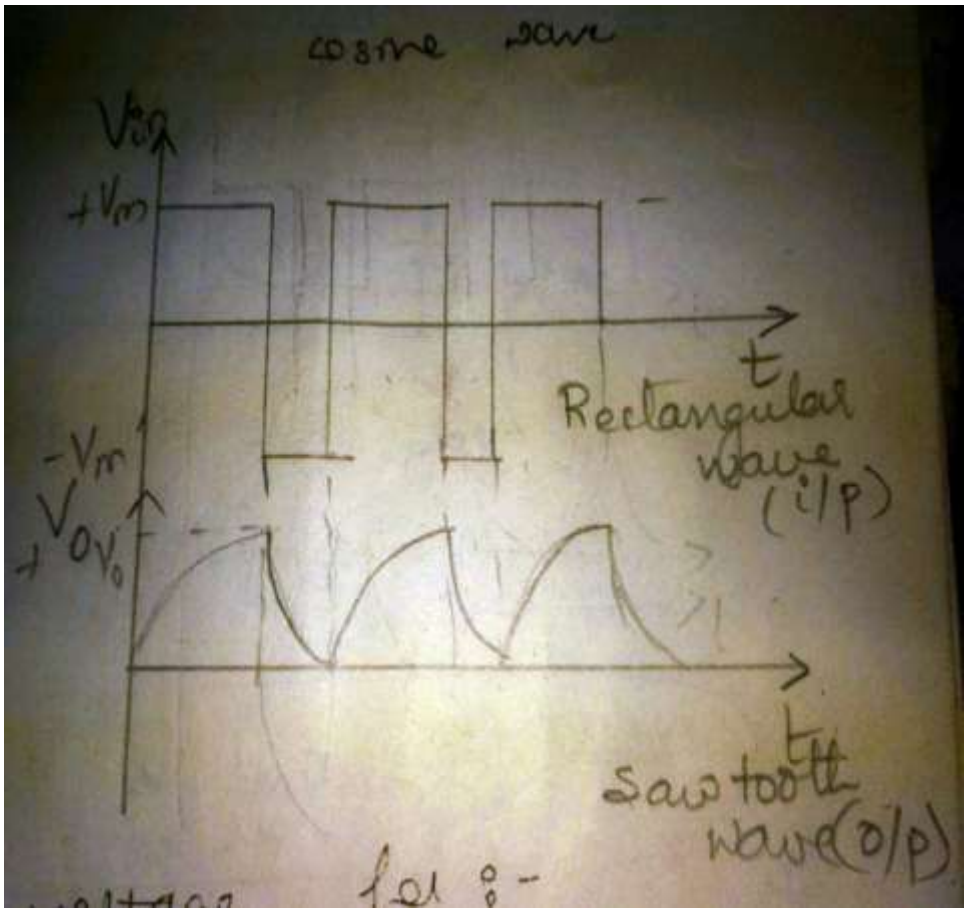


Fig: Integrator Circuit

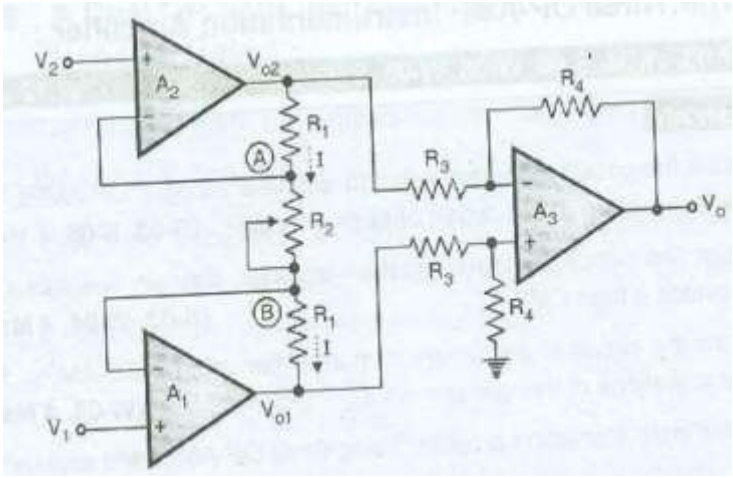


Waveform for Rectangular input as sawtooth as output

3. Attempt any four of the following 16

a) Explain the operations of instrumentation of amplifier using 3 Op-Amps.

Ans:- Diagram – 2 mks, explanation- 2 mks



The high impedance instrumentation amplifier using cross coupled difference amplifiers is as shown in fig.

A_1 and A_2 in Fig are basically non inverting amplifiers with their inverting (-) terminal connected to resistors R_2 instead of connecting it to ground.

As the input impedance of all OP- AMPs used in assumed to be infinite their input current is zero. Therefore current flowing through the resistors R_1, R_2 and R_3 is same i.e.I.

The overall gain of Av of the three Op-Amp instrumentation amplifier is given by

$Av = Av_1 \times Av_2$

Therefore, $Av = \left[1 + \frac{2R1}{R2}\right] \times \frac{R4}{R3}$

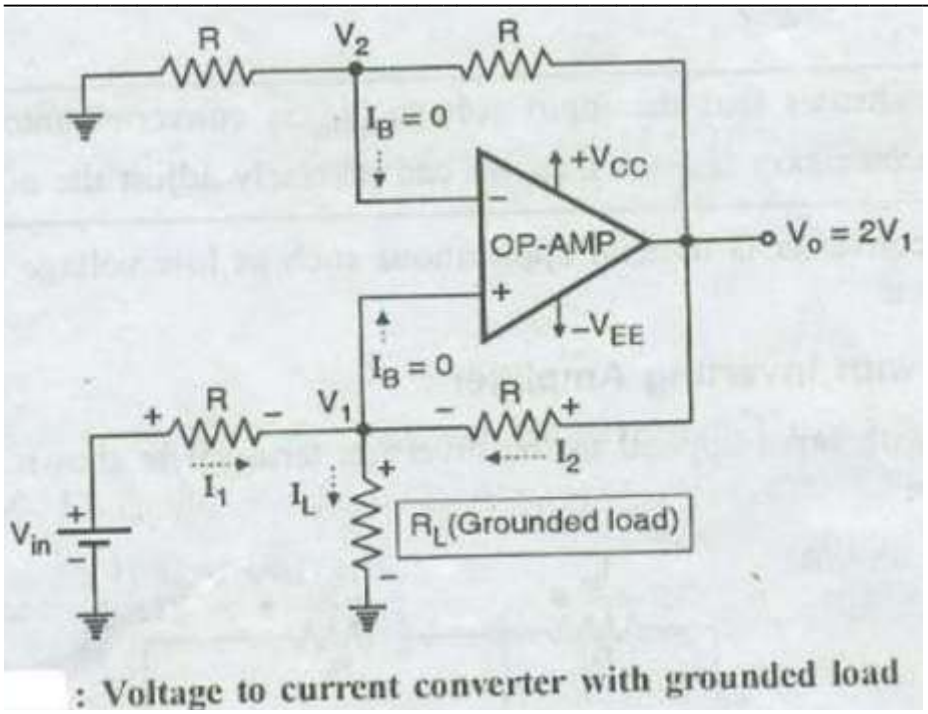
Hence by using a variable resistor R2 the overall gain can be easily and linearly varied.

The output is then given by

$Vo = Av \times (V_1 - V_2)$

b) Draw V-1 converters with grounded load and derive expression for its output.

Ans:- Diagram- 2 mks, derivation- 2 mks



: Voltage to current converter with grounded load

- The analysis of the circuit can be done by following two steps: First step is to determine the voltage V_1 at the non- inverting (+) terminal and the second step is to establish relationship between V_1 and the load current I_L.
- Applying KCL at node V_1,

  $I_1 = I_1 + I_2$ ---------- (1)

  But $I_1 = V_{in} - V_1 / R$ and $I_2 = V_o - V_1 / R$, Substituting these expression into equation (1)

$$I_L = \frac{V_{in} - V_1}{R} + \frac{V_o - V_1}{R}$$

$$\therefore \quad V_{in} + V_o - 2V_1 = I_L R$$

$$\therefore \quad V_1 = \frac{V_{in} + V_o - I_L R}{2} \qquad \text{-----(2)}$$

ius we have obtained the expression for V1.

- The OP- AMP is connected in the non- inverting mode. Therefore gain of the circuit is,

$$A_{VF} = 1 + \frac{R}{R} = 2.$$

- The output voltage is given by,

$$V_o = A_{VF} \times V_1 = 2V_1$$

- Substituting V1 from equation (2) we get,

$$V_o = V_{in} + V_o - I_L R$$

$$\therefore \quad I_L R = V_{in}$$

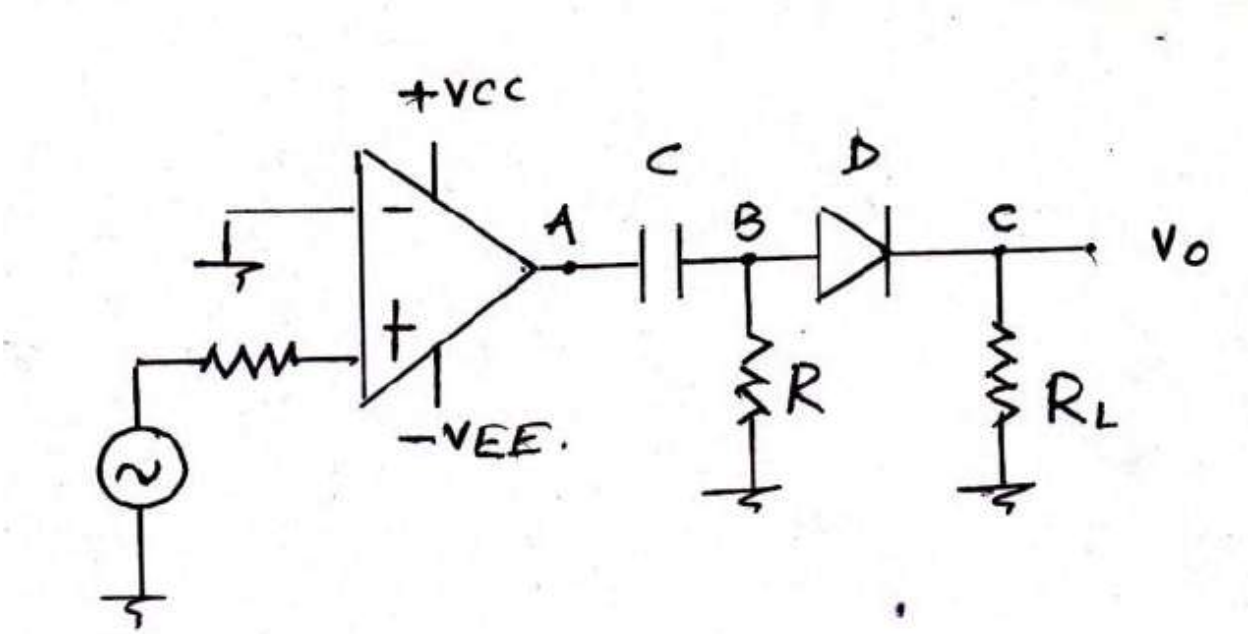
$$\therefore \quad I_L = \frac{V_{in}}{R} \qquad \text{-----(3)}$$

- Equation 3 shows that the load current is dependent on the input voltage and resistor R. Note that all resistors in the figure must be equal in value.

c) State that need of phase detector and draw its circuit diagram.

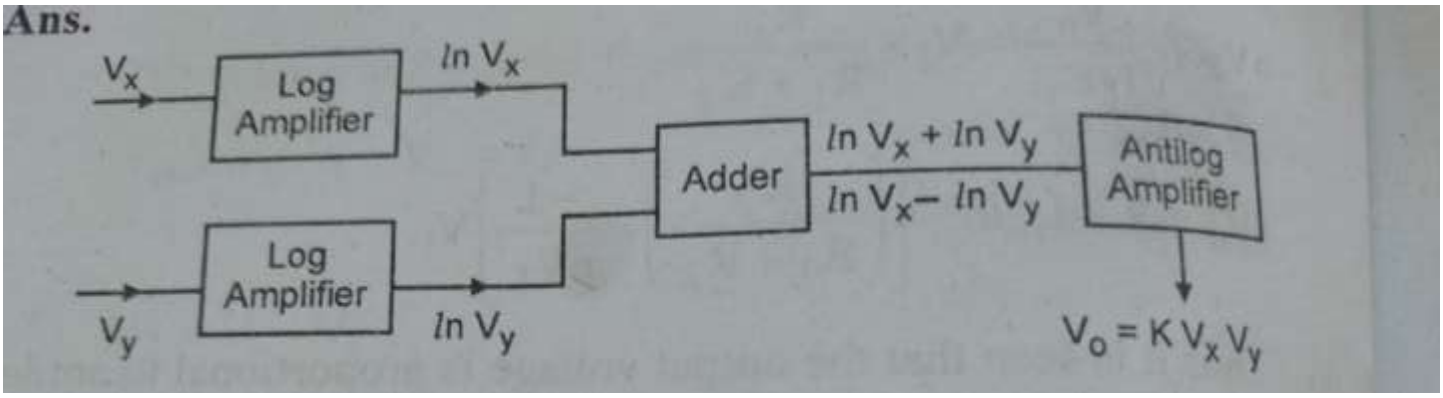
Ans:-Need-2 mks, diagram- 2 mks

Need-In order to detect the phase difference between two signals ,phase detector is used where the width of the pulse obtained is proportional to the difference in phase between two signals V1 and V2.



d) Draw and describe following Op-Amp based operation using log and antilog amplifier $V_0 = V_1 \times V_2$

Ans:- Diagram-2 mks, description-2 mks

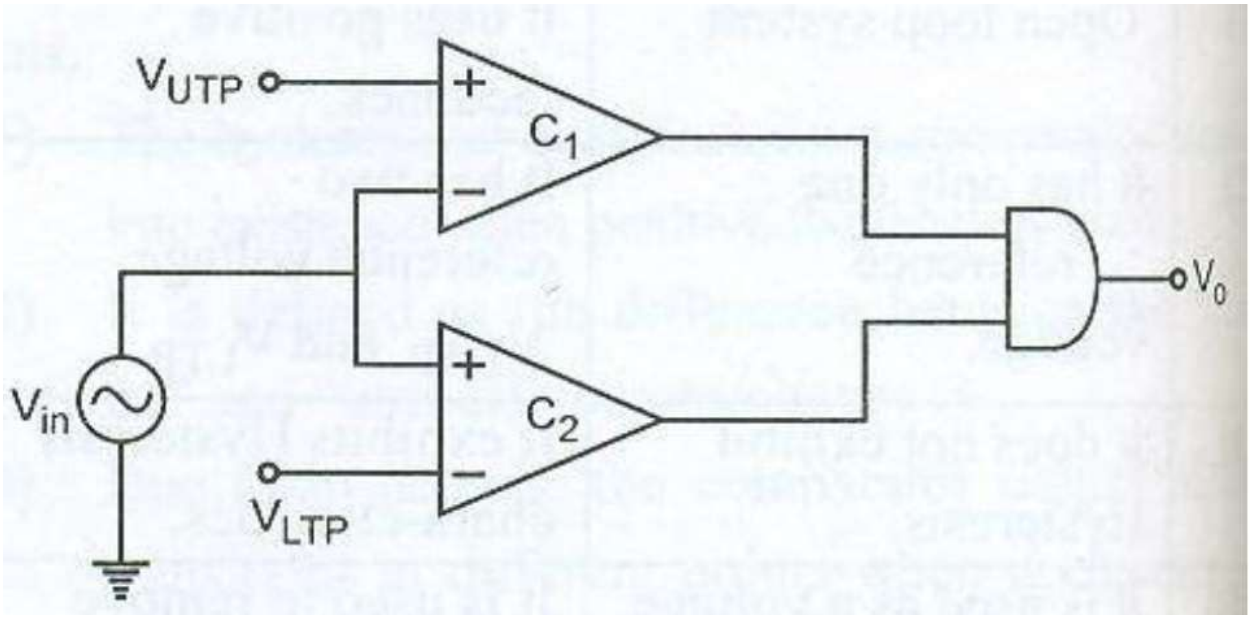


Description:- The two inputs to be multiplied are applied to the log amplifier to provide the outputs log V_X and log V_Y .The inputs are given to adder circuit to provide log Vx +log Vy. The two inputs are applied to antilog amplifier which provides the output

VO= K*Vx *Vy.

e) Draw circuit diagram and input output waveforms of window detector.

Ans:-Diagram- 2 mks, waveforms- 2 mks



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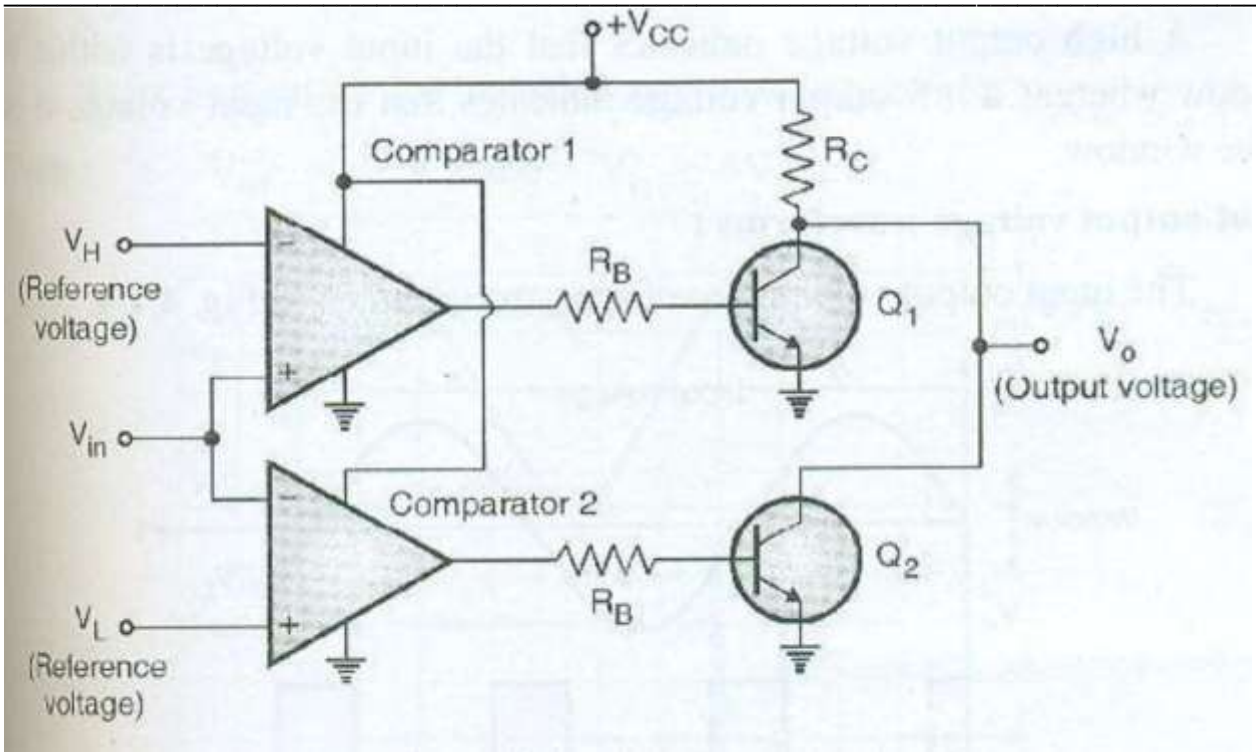
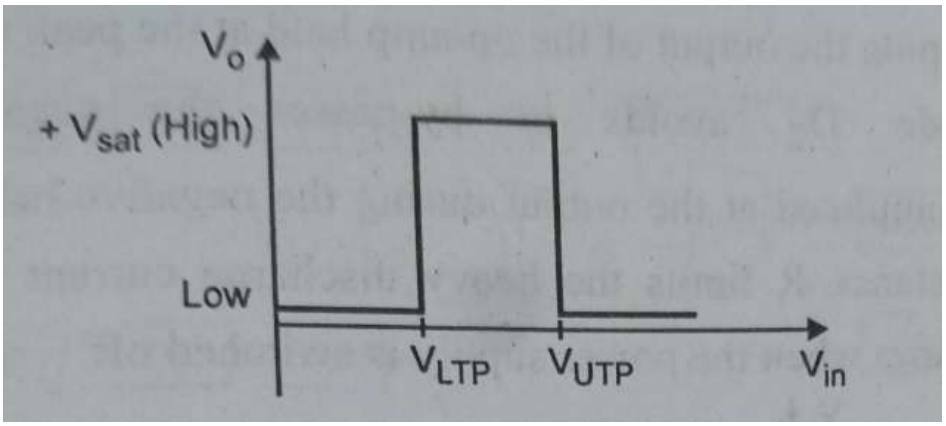
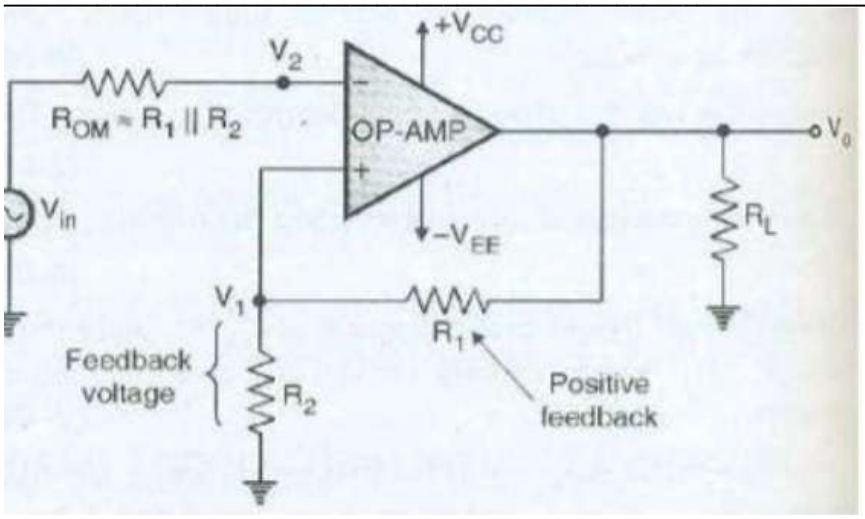


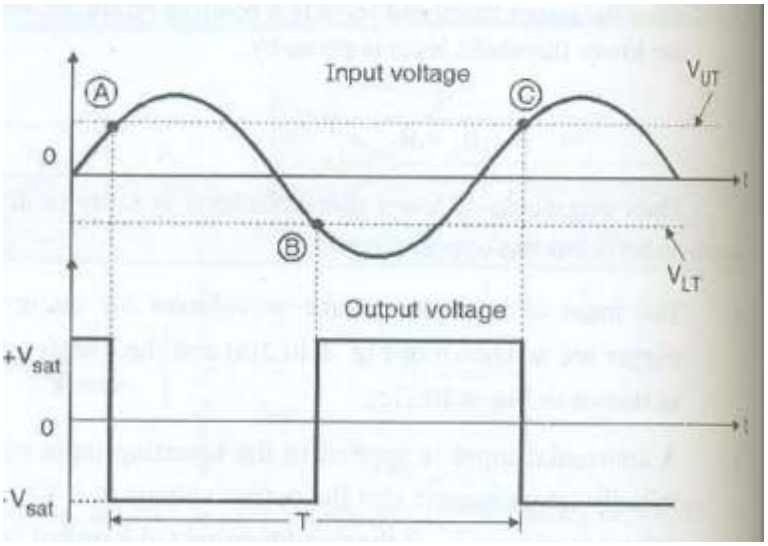
Waveforms-



f) Describe the operation of Op-Amp based Schmitt trigger with neat circuit diagram.

Ans:- (Circuit diagram-2 mks, waveforms- 1 mks,explanation-1 mks)





Initially, before the application of any input, the output is assumed to be small and positive. This is the output offset voltage. The potential at point B is positive and point A = 0 V. The differential voltage V_{id} is positive. Hence the output is driven to $+ V_{sat}$.

At this instant, the potential at point B is

$$V_B = \frac{R_2}{R_1 + R_2} \cdot (+V_{sat})$$. This is called as the upper trigger point (V_{UTP}). When the input becomes more positive than V_{UTP}, the differential input is negative. Therefore, the output is driven to $-V_{sat}$.

At this instant, the potential at the point B is

$$V_B = \frac{R_2}{R_1 + R_2} \cdot (-V_{sat})$$

This is the lower trigger point (V_{LTP}). The output remains at $-V_{sat}$ until input voltage becomes more negative than V_{LTP}. When the input crosses and becomes more negative than V_{LTP}, the differential input voltage is again positive and the output becomes $+ V_{sat}$.

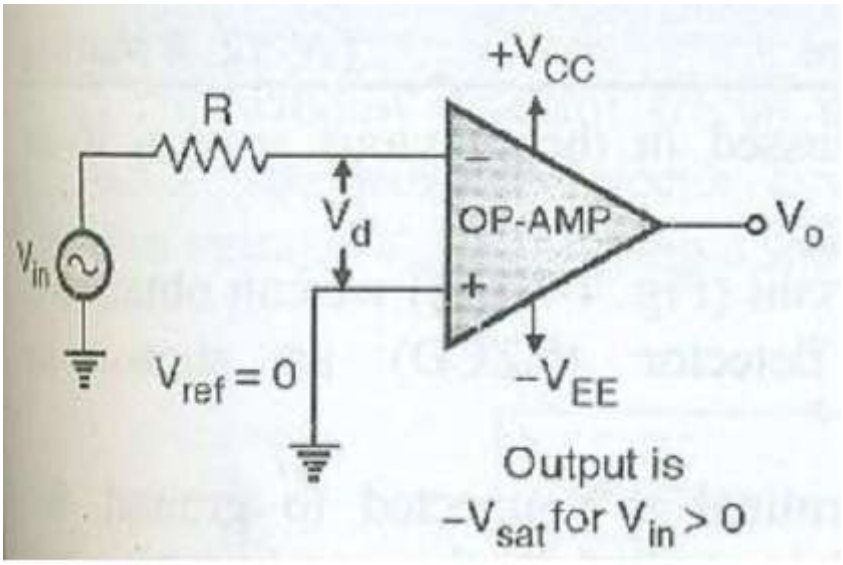
Thus, if the threshold voltages V_{UTP} and V_{LTP} are made larger than the input noise voltages, the positive feedback will eliminate the false output transitions.

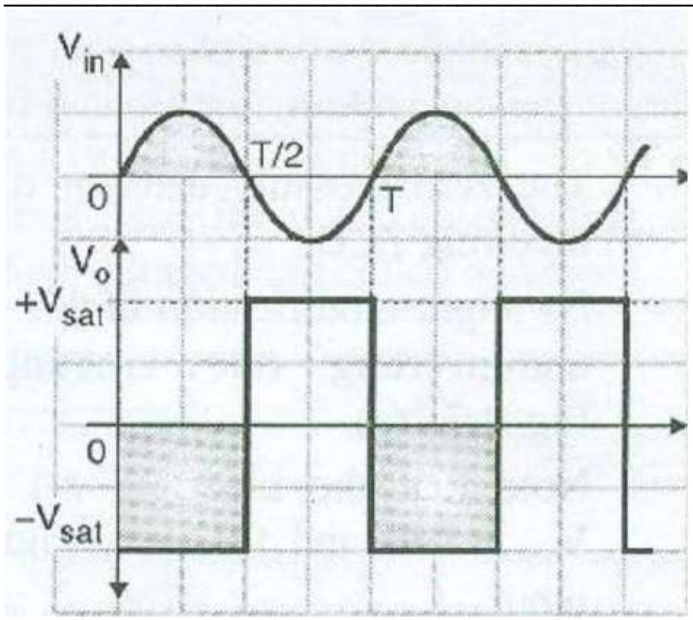
Thus, the Schmitt trigger has two, reference voltages.

4. Attempt any four of the following 16

a) Draw circuit and input output waveform of ZCDs.

Ans:- Diagram- 2 mks, waveforms-2 mks





b) Design and draw high pass filter with cut off frequency 2 KHz and pass-band gain of 2.

Ans:- Design steps – 2 mks, proper diagram with values- 2 mks

Given :- Cut off frequency=Fc=2 Khz

Passband gain= 2

Gain=1+ (RF/R1) =2, Choose R1=10k

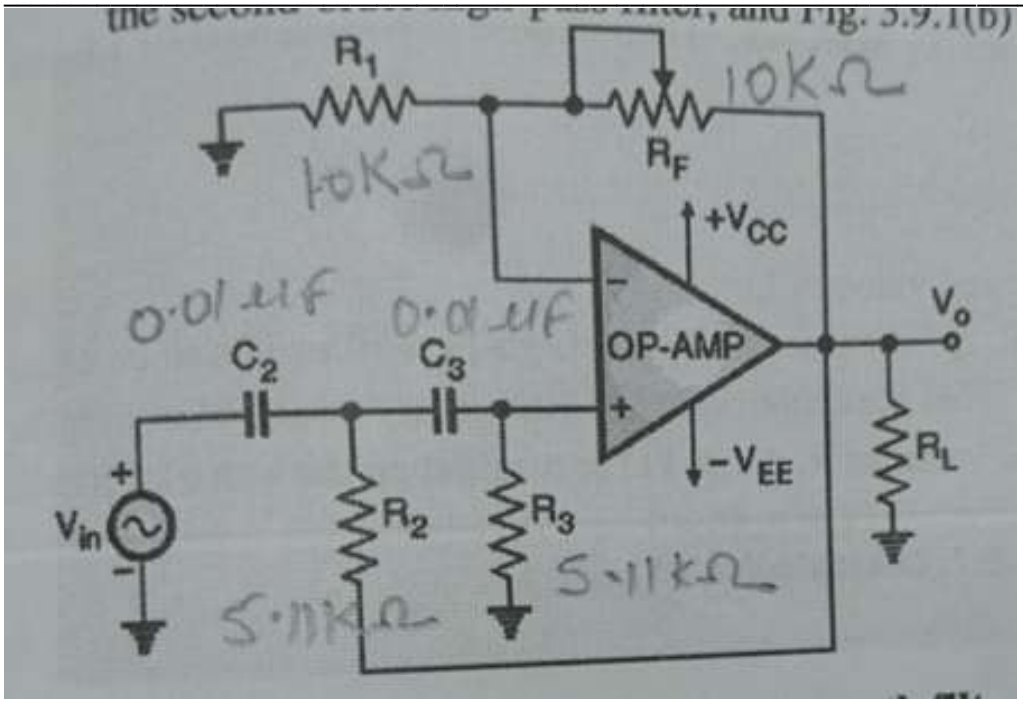
So, RF=R1

Let RF=R1=10KΩ

FC=1/(2πRC)= 2Khz

Let C=0.01μF = C2=C3

So, R=7.96KΩ = R2 = R3



c) State merits and demerits of active filters over passive filters (2 each)

Ans:- (2 mks for advantages , 2 mks for disadvantages ,any 2 points for each)

Merits

1) Gain and frequency adjustment possible
2) No loading problem
3) Cost is less

Demerits

1)Stability considerations limits the uses of most of the filters below 100kHz

2)Selectivity and center frequency are often very sensitive function of gain of op – amp or absolute value of feedback.

d) Explain the operation of wide bandpass filter with the help of neat circuit diagram.

Ans:- Circuit diagram- 2 mks, operation- 1 mks, frequency response- 1 mks

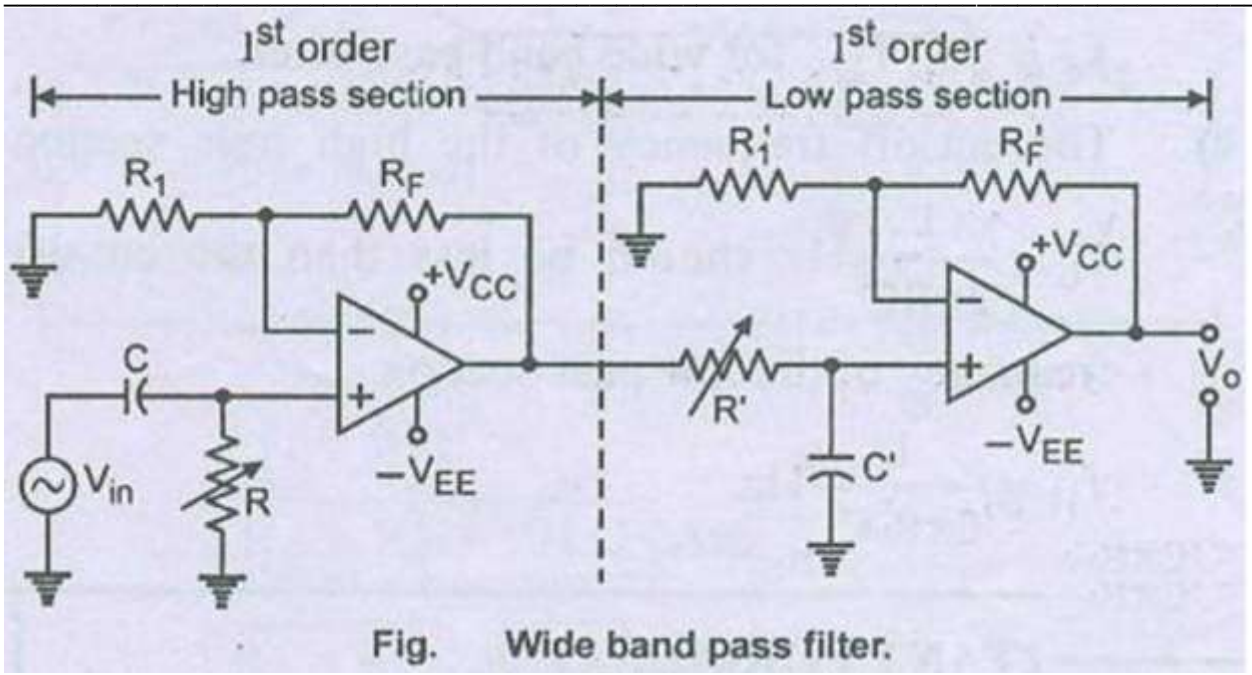
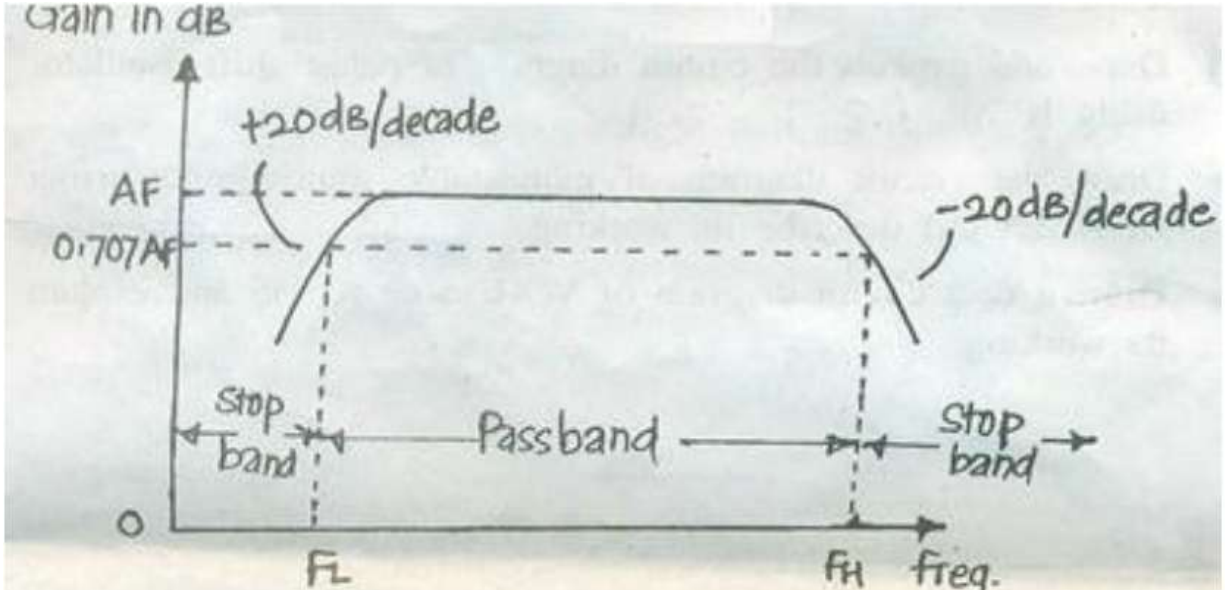


Fig. Wide band pass filter.



Operation:-

A wideband pass filter passes all the frequencies from FL to FH and attenuating frequencies outside the bands. The cutoff frequencies are given as

FL=1/(2 πRC)

FH=1/(2πR'C')

Also,

Gain is given as-

AF=1+(RF/R1) ,where RF=RF' and R1=R1'

e) Describe Notch filter with neat circuit diagram.

Ans:- (Circuit diagram-2 mks, operation-1 mks,frequency response- 1 mks)

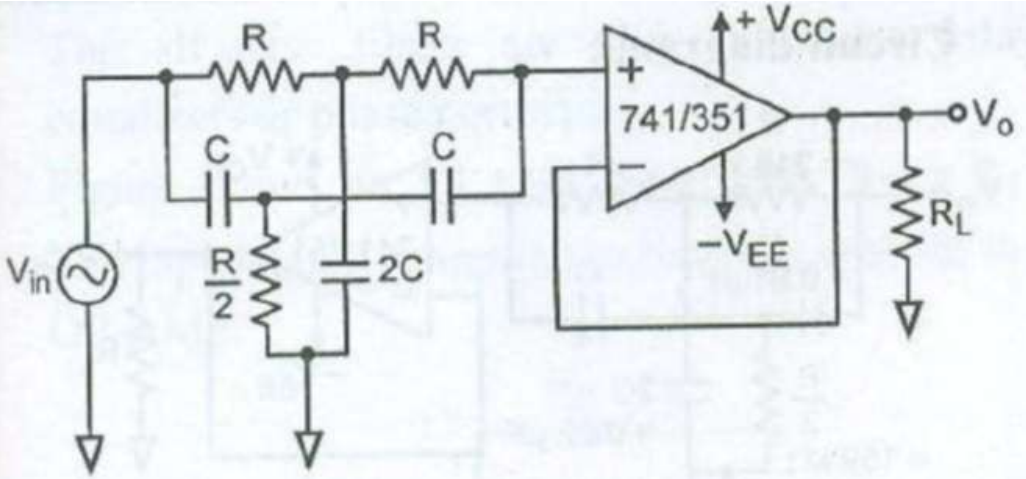


Fig. (a) Narrow band reject filter

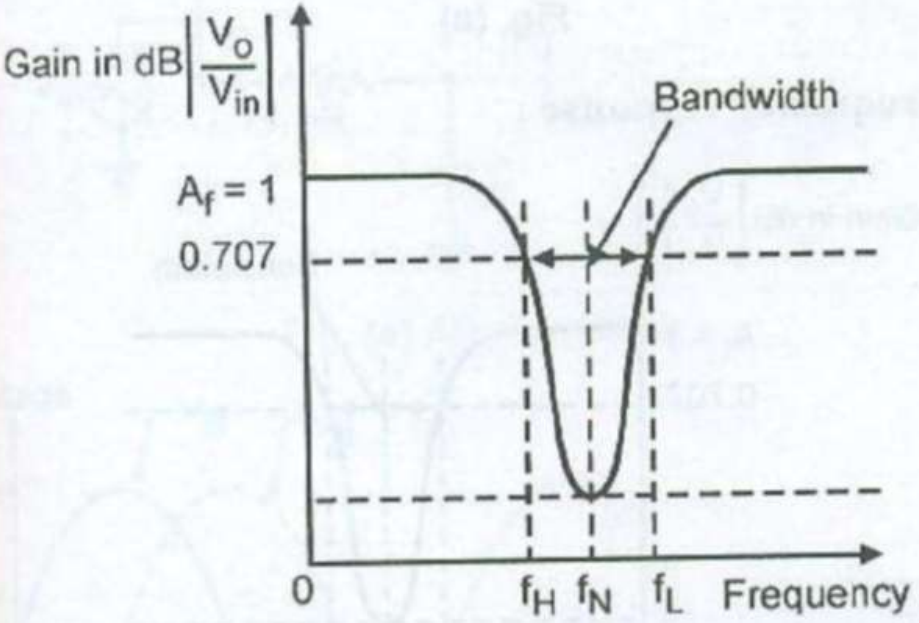


Fig. (b) Frequency response of narrow band reject filter

Operation:-

i. Fig. shows a narrow band rejects active filter often called as Notch filter. It uses a twin T- network.
ii. The twin T- network is a passive filter composed of two T- shaped networks.
iii. One T- network is made up of two resistors and capacitors while the other uses two capacitors and a resistor.
iv. The notch out frequency is the frequency at which maximum attenuation occurs, it is given by
$f_N = 1/2\pi RC$ Hz---------- (1)
v. The twin T- network has very low figure of merit Q. this is increased by using it with a voltage follower as shown in fig. The output of the voltage follower is fed back to the junction of R/2 and C.
vi. Q> 10 for narrow band reject filter.
vii. One typical application of such filter is for rejection of single frequency, such as 50 Hz power line frequency hum. This notch filter is also used in communication and Bio- medical instruments for eliminating undesired frequencies.
viii. Frequency in equation (1) is the frequency to be rejected. Choosing C≤ 1μF and then calculate for R, from the equation.

f) Define with respect to filters:

i) Roll off rate
ii) BW
III) Q Factor
iv) Stop –band

Ans:- (Each definition – 1 mks)

i) Roll off rate:- The rate at which the gain of op-amp decreases with increase in frequency beyond the cut-off frequency is called as roll off rate. It is expressed in dB/decade and it depends on the order of filter.

II) BW-The range of frequency over which the gain of op-amp remains almost constant and is given as the difference between higher cutoff frequency FH and the lower cutooff frequency FL

BW=FH-FL

iii) Q Factor- Defined as the ratio of energy store to energy dissipated and should be as high as possible.

iv) Stop band:- The range of frequencies over which signals are attenuated by the filter is called as stop band.

5. Attempt any four of the following 16

a) Describe the operation of phase detector and VCO in PLL.

Ans:- Each operation – 2 mks

Voltage controlled oscillator (VCO):

- The control voltage V_C is applied at the input of a VCO.
- The output frequency of VCO is directly proportional to the dc control voltage V_C. The VCO frequency f_o is compared with the input frequency f_s by the phase detector and it (VCO frequency) is adjusted continuously until it is equal to the input frequency f_s i.e. $f_o = f_s$

- The voltage controlled oscillator (VCO) is a free running multivibrator and operates at a frequency f_o, which is determined by external timing capacitor and external resistor.
- The operating frequency can be shifted on either side by applying a dc control voltage V_C externally.

Phase detector or phase comparator:

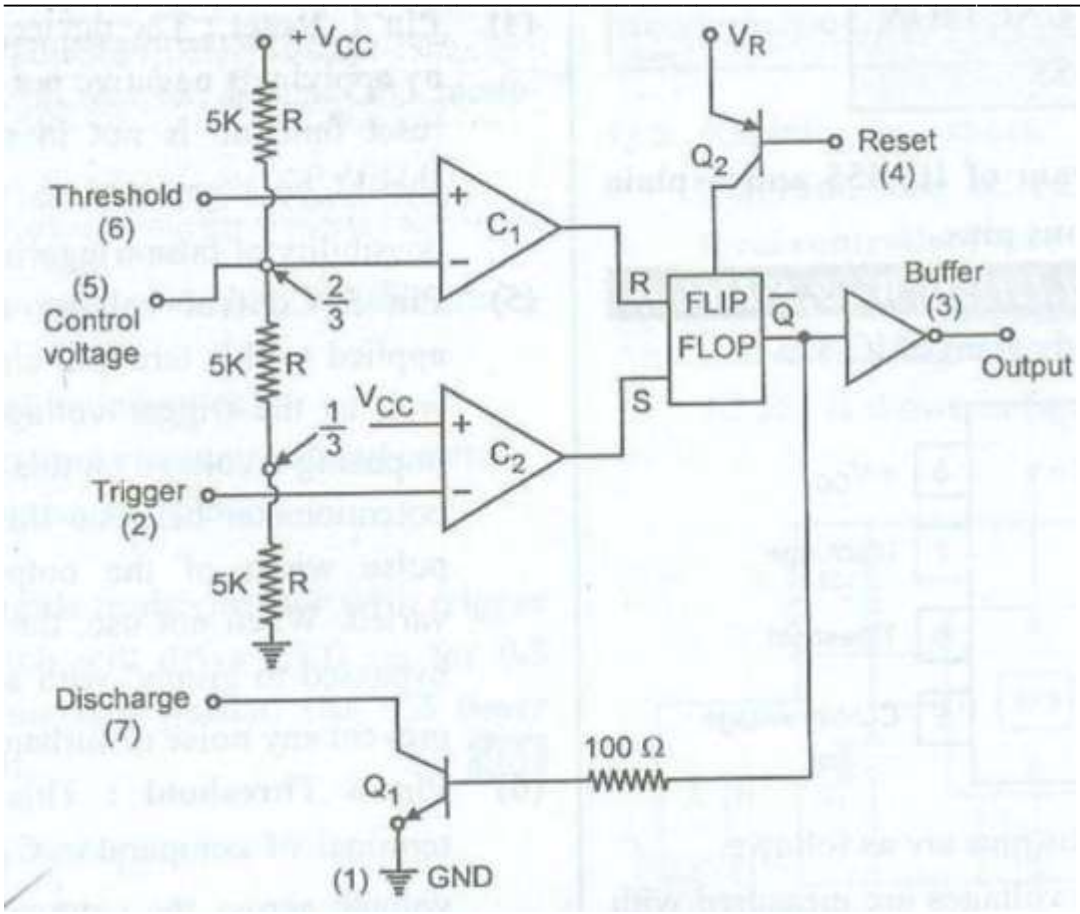
- The two points to a phase detector or comparator are the input voltage V_s at frequency f_s and the feedback voltage from a voltage controlled oscillator (VCO) at the frequency f_o

- The phase detector compares these two signals and produces a dc voltage V_e which is proportional to the phase difference between f_s and f_o. The output voltage V_e of the phase detector is called as error voltage.
- This error voltage is then applied to a low pass filter.

b) Draw block diagram of IC 555 and give function of each pin.

Ans:- Block diagram- 2 mks, function of any 2 pins -2 mks)

Note:- (for 2 mks, funtions of 8 pins is not expected asking 2 pins functions is justified)

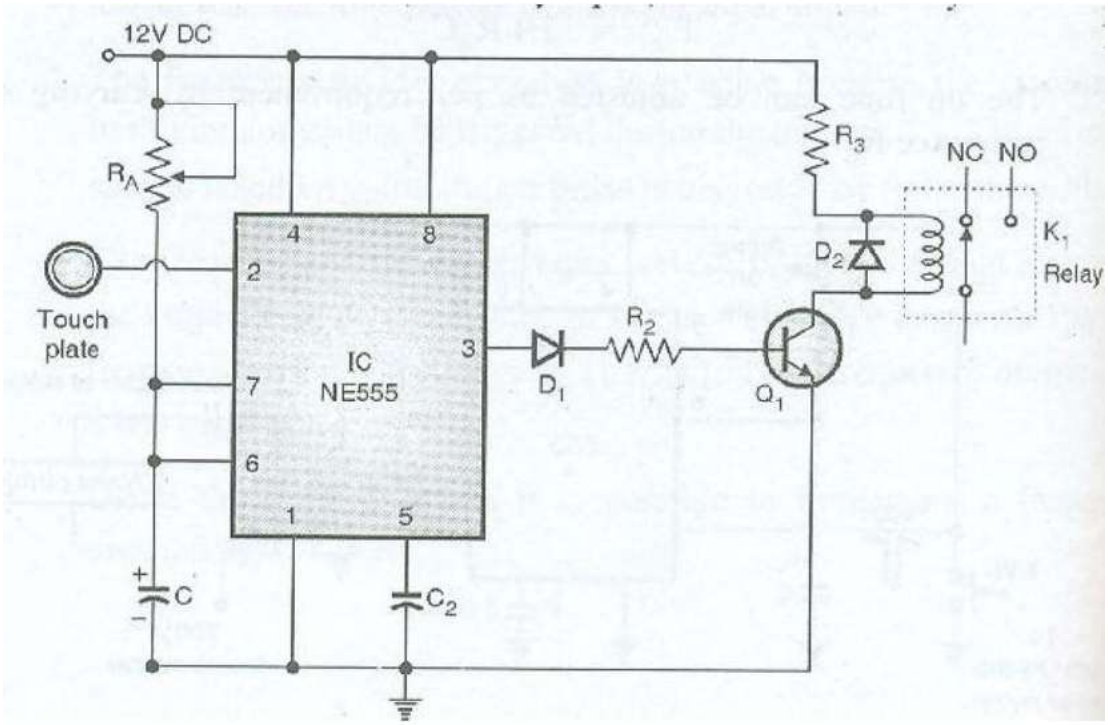


Functions of Pins:-

1. Ground:-All voltages are measured with respect to this pin.
2. Trigger:- This is the inverting terminal of comparator C2 which monitors the voltage across the external capacitor. When the voltage at this pin goes below or equal to 1/3 VCC, the output of comparator C2 goes low which in turn switches the output of the timer to high.
3. Output:-Output can be normally on load or normally off load at this pin.
4. Reset:- when a negative pulse at this pin is applied ,it will reset the IC. If not required to reset, this pin is shorted to +VCC.
5. Control voltage:-When the reference voltage of upper and lower comparator can be changed by applying external voltage to this pin. If not required this pin grounded through a capacitor of 0.1 µF.
6. Threshold: This is non- inverting terminal of comparator C1 which monitors the voltage across the external capacitor. When the voltage at this pin is greater than or equal to 2/3 VCC, the output of comparator C1 goes high which in turn switches the output of the timer low.
7. Discharge:- This pin is connected internally to collector of transistor Q1.When the output is high, Q1 is OFF and acts as open circuit to external capacitor connected between pin 7 and ground. On the other side when the output is low, Q1 is ON and acts as short circuit, shorting the external capacitor to ground and providing discharge path.
8. +VCC:-Power supply for operation.

c) Describe the operation of touch plate switch using IC 555 with neat diagram.

Ans:- (Circuit diagram- 2 mks, operation- 2 mks)



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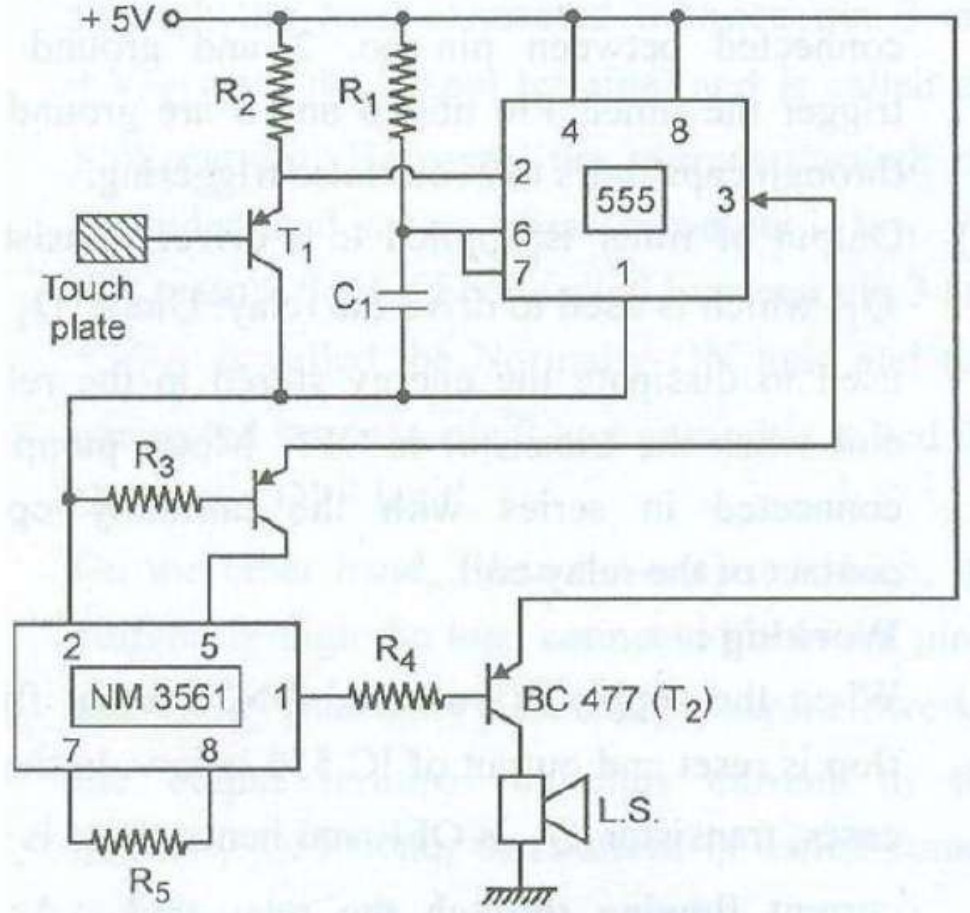


Operation:-

When this circuit is connected to a metal locker or cupboard, generates an alarm when touched by an undesirable entity.

The transistor gets saturated by just touching its base. The 50 Hz hum present in our body is the key to this circuit. The circuit is basically a burglar alarm with timer. Timer circuit is a monostable multivibrator.

If the sensor, which is base of the transistor T_1, touched by the finger, transistor T_1, is saturated. Now the voltage at pin 2 of IC_1 is less than 1/3 V_{CC}. As a result IC_1 gets a trigger pulse at its trigger input pin 2. Therefore its output goes high for a predetermined time period.

The period can be adjusted by varying the value of resistor R_1 or capacitor C_1 as $T = 1.1R_1C_1$ sec.

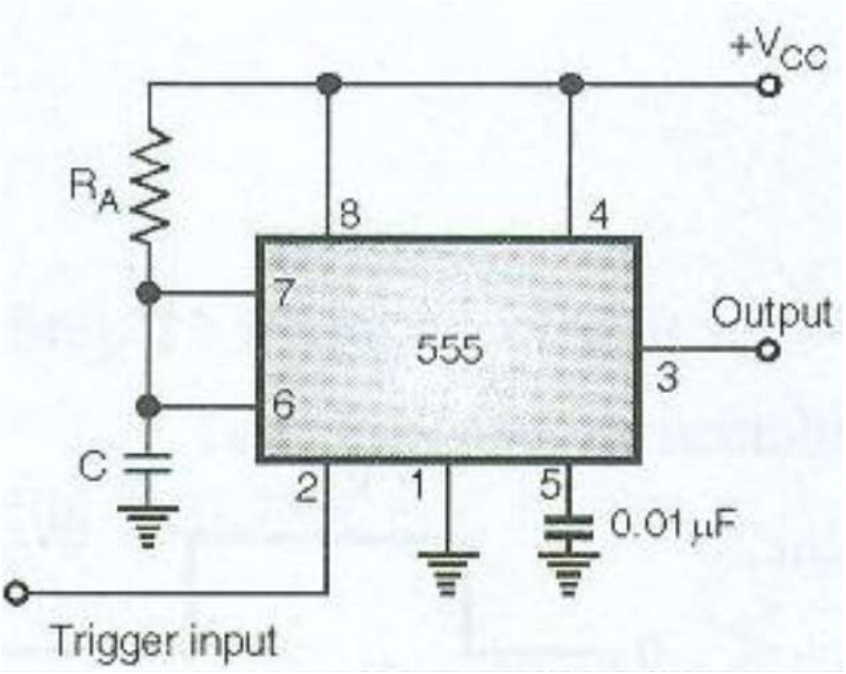
d) Explain the operation of frequency divider using IC 555.

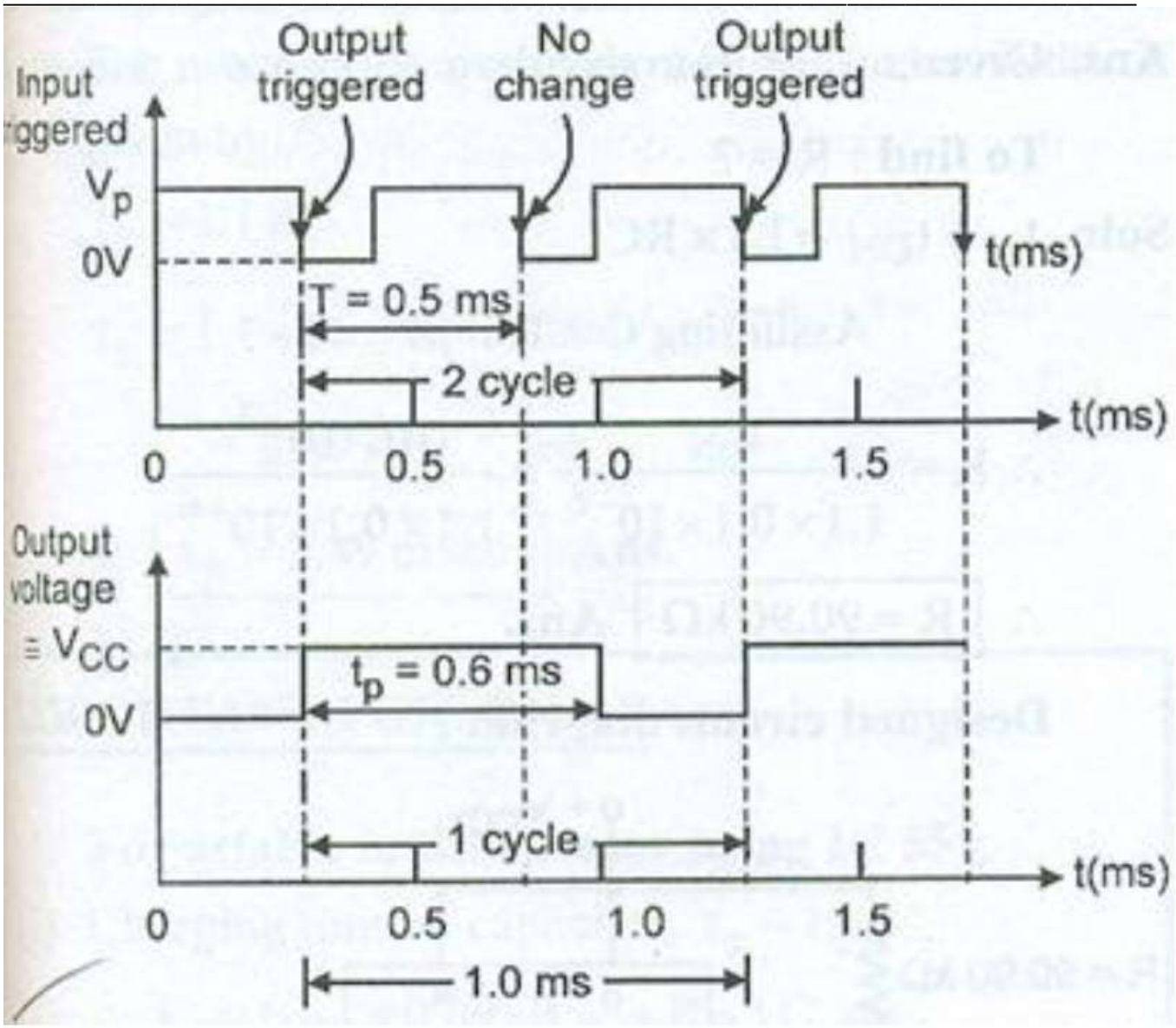
Ans:- (Diagram- 2 mks, operation- 1 mks, waveforms- 1 mks)

The monostable multivibrator can be used as frequency divider by adjusting the length of the timing cycle t_p with respect to time period T of the trigger input signal applied to pin 2.

To use the monostable multivibrator as divide by 2 circuit, the timing interval t_p must be slightly larger than the time period T of the trigger input signal as shown in figure below. By the same concept, to use the monostable multivibrator as divider by 3 circuit, t_p must be slightly larger than twice the period of the input trigger signal and so on.

The frequency divider application is possible because the monostable multivibrator cannot be triggered during the timing cycle.





e) Draw and describe the block diagram of PLL.

Ans:- (Diagram- 2mks, description – 2 mks)

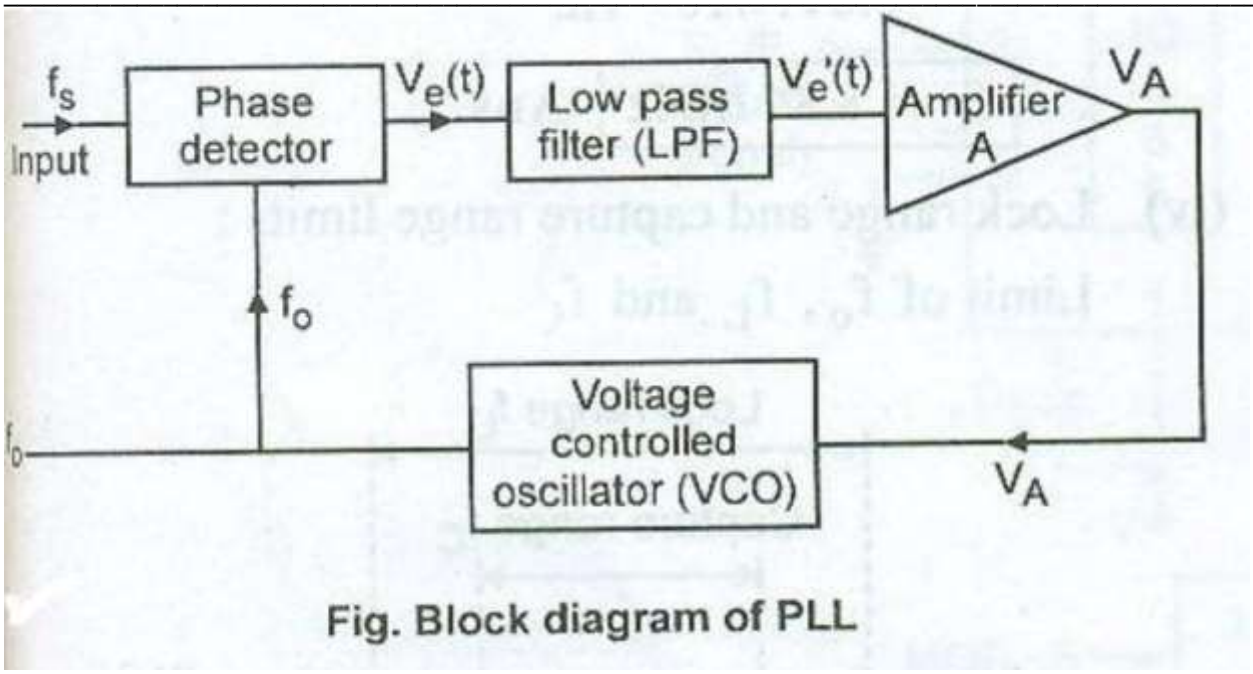


Fig. Block diagram of PLL

Here f_s is the signal frequency & f_o is the output frequency.

The voltage controlled oscillator (VCO) is a free running multivibrator and operates at a frequency f_o, which is determined by external timing capacitor and external resistor.

The operating frequency can be shifted on either side by applying a dc control voltage V_C externally.

The change in frequency is directly proportional to the dc control voltage applied and hence it is termed as voltage controlled oscillator (VCO).

If an input signal frequency f_S is applied to PLL, then the phase comparator/ detector compares the phase and frequency of the input signal with the output signal or feedback signal f_o of VCO.

If the two signals differ in frequency/ phase an error voltage $V_e(t)$ is generated.

The phase detector used is basically a multiplier which produces the sum $(f_s + f_o)$ and difference $(f_s - f_o)$ frequency signal at the output.

The high frequency signal $(f_s + f_o)$ is removed by low pass filter and the difference frequency signal $(f_s - f_o)$ is amplified by amplifier which is passed by low pass filter.

This difference frequency signal is then applied to VCO. VCO shifts the frequency so as to reduce the frequency difference between f_s and f_o.

Once this controlling action starts, the signal is in the capture range of PLL.

f) Define and state the expression for lock and capture range of PLL.

Ans:- (definition and formula- 1 mks each)

Lock range : The range of frequencies over which PLL can maintain the phase lock with the incoming signal Fs,is defined as lock in range.

Lock range =Fl =2Δ fL

$$f_L = \pm \frac{8fo}{V}$$

Capture Range : It is defined as the range of frequencies over which the PLL can acquire lock with the input signal Fs

Capture range = 2Δ fC

$$f_C = \pm [fL/2\pi x3.6x10^3 xC]^{1/2}$$

6. Attempt any FOUR of the following: 16

a) Describe VCO using IC 555 with neat circuit diagram.

Ans:- (Circuit diagram- 2 mks, description- 2 mks)

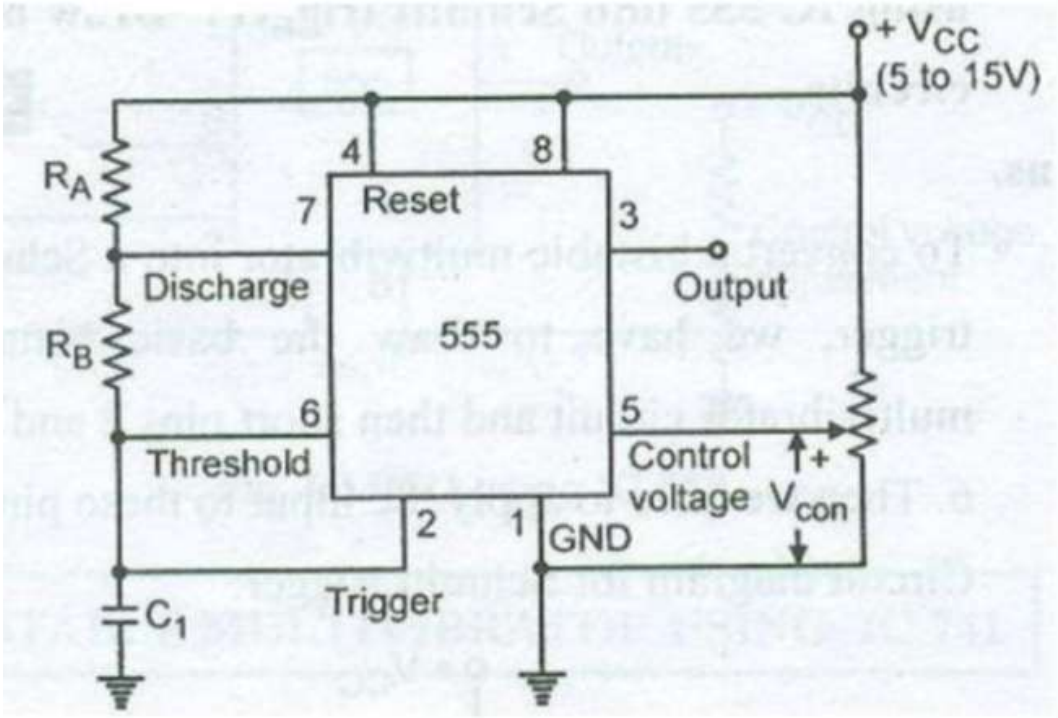
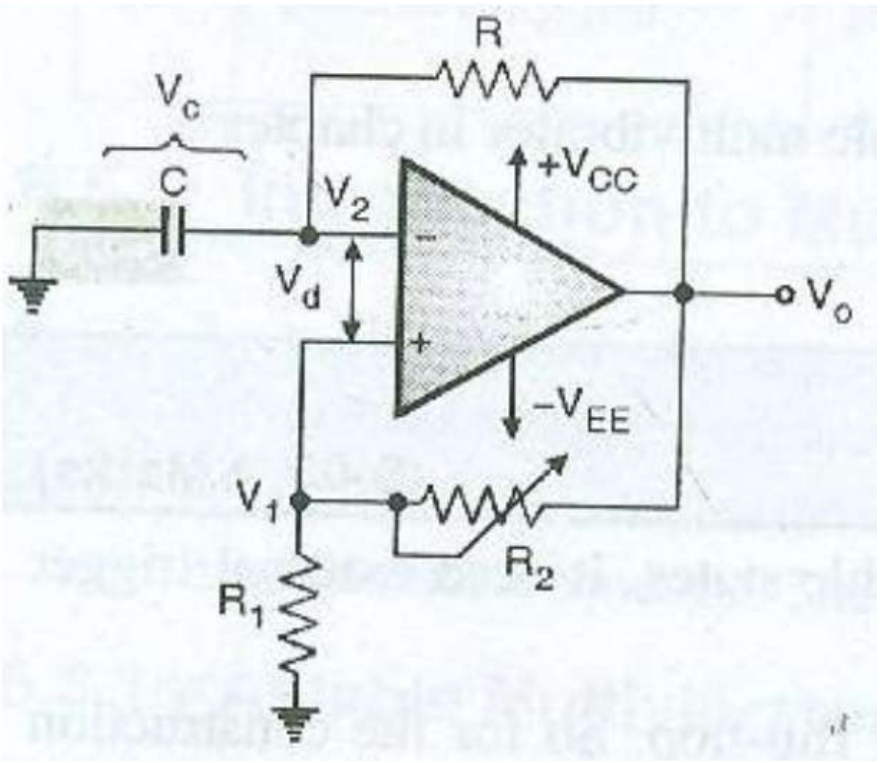


Fig: Circuit diagram of VCO using IC 555

- The value of charging and discharging current is dependent on the control voltage V_C applied at pin number (5) modulating input.
- This current can also be changed by varying the external timing resistor R_T.
- The potential difference between pins (5) and (6) I almost zero. That means these pins are equipotential.
- Therefore if we increase the modulating voltage V_C at pin number (5), the voltage at pin number (6) will increase with the same amount.
- This reduces the voltage drop across R_T and reduces the charging current.
- The voltage across the capacitor is thus triangular wave. This triangular wave is applied to a buffer A_1.
- The buffer is connected in order to avoid to avoid any possible loading of the capacitor. The buffer output is taken out at pin number (4) as triangular wave output.
- The buffer output is also applied to a Schmitt trigger A_2, which converts the triangular wave into square waveform.
- Resistors R_a and R_b is a potential divider generating the reference levels for the upper and lower trigger voltages. This square wave is inverted by inverter A_3 and made available at pin number (3).

b) Draw and explain astable multivibrtor using IC 741.

Ans:-Diagram- 2 mks, explanation- 1 mks , waveforms- 1 mks



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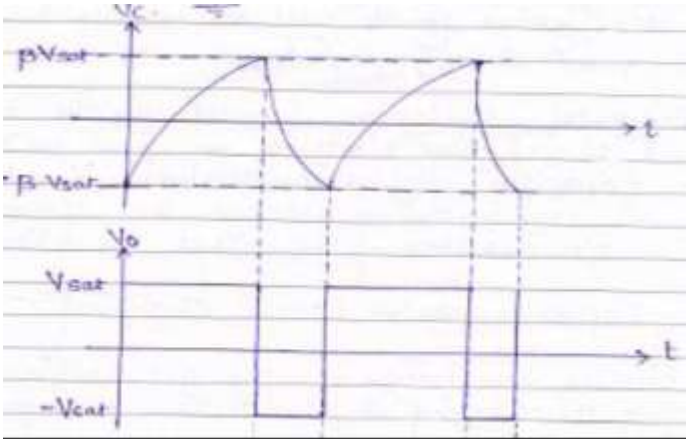


Description-

Initially there is output offset voltage due to the characteristics of op-amp. Consider it as + Vsat, therefore at point V_1, the voltage is equal to ,

$$V_1 = \left(\frac{R_1}{R_1 + R_2}\right)(+V_{sat})$$

- Therefore capacitor will start charging through R to the value $\beta\ (+V_{sat})$ which is equal to V_1
- When capacitor charges to the required value or slightly greater than the non inverting terminal, then output will get change to –Vsat.
- Now, at point V_1, the voltage is equal to ,

$$V_1 = \left(\frac{R_1}{R_1 + R_2}\right)(-V_{sat})$$

- Capacitor discharges & will try to reach value of $\beta\ (-V_{sat})$ which is equal to V_1
- When capacitor discharges below V_1 , then non inverting terminal becomes less than inverting terminal, then output will get change to +Vsat. Therefore capacitor starts charging.
- The process continues, so we get continuous charging & discharging of capacitor & thus output changes continuously.

c) Design monostable multivibrator with T_P = 1 ms using IC 555.

Ans:- Design steps- 2 mks, diagram with proper values- 2 mks

circuit.

Soln. The pulse width of the output of the monostable multivibrator is given by the formula

$T_{ON} = 1.1\ RC$

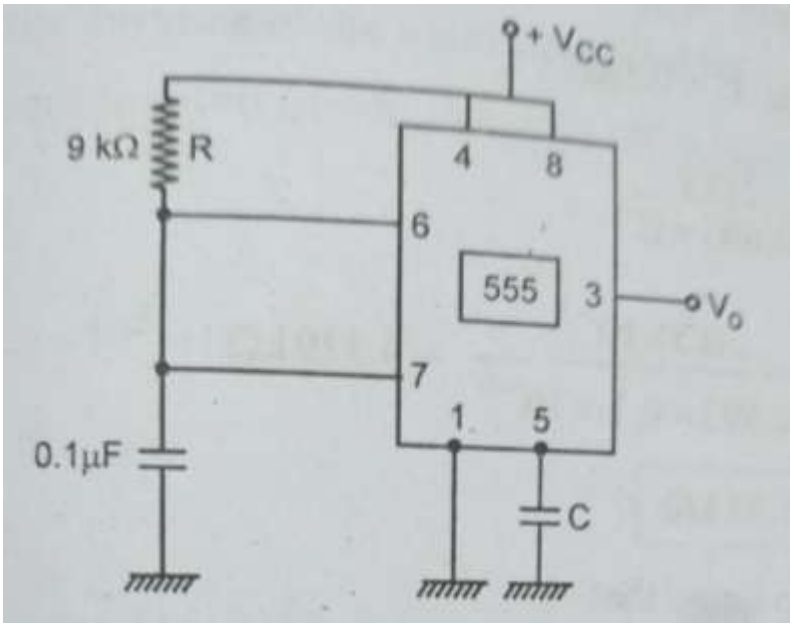
$C = 0.1\ \mu F$

$T_{ON} = 1\ ms$

$$R = \frac{1 \times 10^{-3}\ s}{1.1 \times 0.1 \times 10^{-6}}$$

$$= \frac{10^{-3}}{1.1 \times 10^{-7}}$$

$$= 0.909 \times 10^{4}\ \Omega = 9\ k\Omega \text{ (approx.)}$$



d) Design wein bridge oscillator for 1 kHz frequency using Op-Amp. Draw designed circuit.

Ans:- (Proper design – 2 mks, circuit diagram with component values – 2 mks)

$$f = \frac{1}{2\pi RC}$$

Assume $R = 1K$

$$1k = \frac{1}{2\pi \times 1K \times C}$$

$$C = \frac{1}{2\pi \times 1K \times 1K}$$

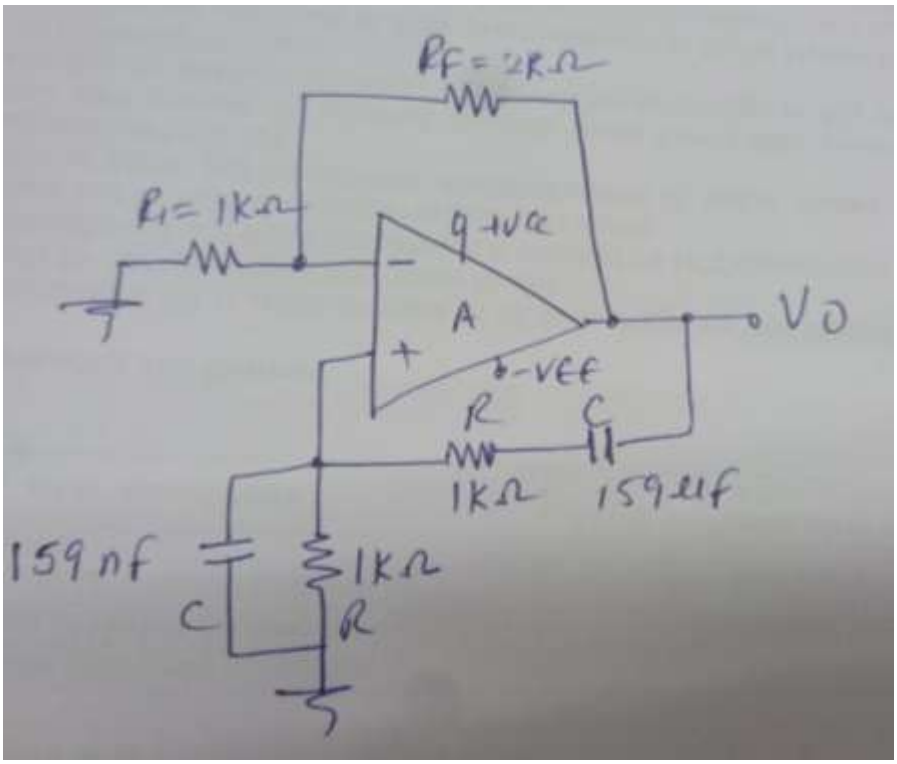
$$= 159\,nf$$

The gain is given as

AF=1 + (RF/R1) =3

So let R1= 1K and hence RF=2 K

The circuit designed is



e) Draw and describe operation of bistable multivibrator using Op-Amp.

Ans:- (Diagram- 2 mks, description- 1 mks, waveforms- 1 mks)

Fig. .(a) shows the circuit diagram of a bistable multivibrator using OP-AMP 741. This circuit will have two stable states.

In one stable state, the output voltage is + V_{sat} and in the other one it will be – V_{sat}. To switch over from one stable state to the other, we need to apply trigger pulses at the input.

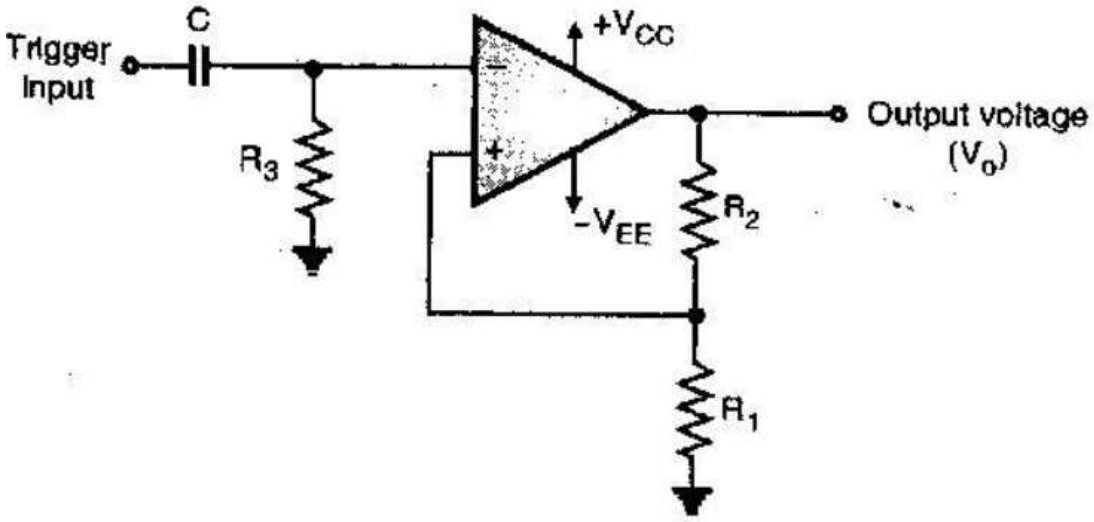
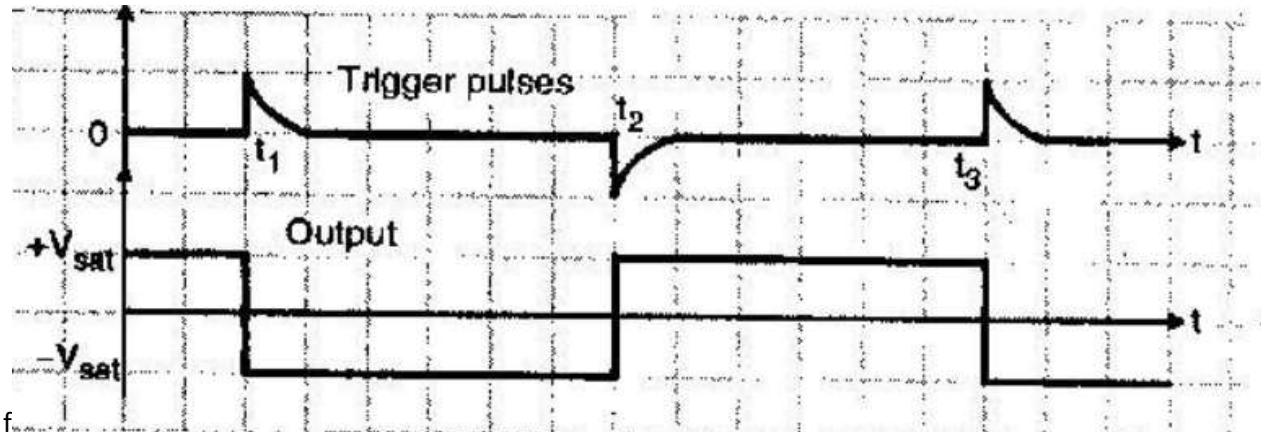


Fig a.



f.

Fig b.

This is because the inverting terminal is connected to ground through the resistor R_3. Output voltage $V_o = + V_{sat}$ is one stable state of the circuit.

- In order to change the state of output from $+ V_{sat}$ to $- V_{sat}$, it is necessary to have a higher positive voltage at the inverting (–) terminal, than that of the non-inverting (+) terminal. Therefore we apply a positive pulse at instant "t_1" at the trigger input terminal, as shown in Fig. (b) The amplitude of trigger pulse is given by,

$$V_{TRIGGER} > \frac{R_1}{(R_1 + R_2)} \times (+ V_{sat})$$

- As soon as this pulse is applied, the OP-AMP will change its output from $+ V_{sat}$ to $- V_{sat}$. This is the second stable state of this circuit.
- In this stable state the voltage at non-inverting (+) terminal will be equal to,

$$V_{NON\text{-}INV} = \frac{R_1}{(R_1 + R_2)} \times (- V_{sat})$$

- In order to switch the output from $- V_{sat}$ to $+ V_{sat}$, it is necessary to apply a negative trigger pulse at the input. The amplitude of this trigger pulse is given by,

$$V_{TRIGGER} = \frac{R_1}{(R_1 + R_2)} \times (- V_{sat})$$

- At the instant "t_2" as shown in Fig. (b), a negative trigger pulse of adequate amplitude is applied at the input of the circuit. The output will switch over from $- V_{sat}$ to $+ V_{sat}$ at this instant.

Operation of the circuit :

- Initially assume that the output voltage is equal to $+ V_{sat}$. Therefore voltage at the non-inverting terminal (+) is given by,

$$V_{NON-INV} = \frac{R_1}{(R_1 + R_2)} \times (+ V_{sat})$$

- The voltage at the inverting (–) terminal is given by,

$$V_{INV} = 0$$

f) How overall phase shift is achieved in phase shift oscillator using Op-Amp? Draw its circuit diagram.

Ans:- Explanation of phase shift- 2 mks, circuit diagram- 2 mks)

For an oscillator to oscillate at the desired frequency, the overall phase shift between input and output in an oscillator required is 0 °/ 360°. The opamp in inverting mode provides a phase shift of 180°. The 3 RC sections each provides a phase shift of 60°. So they provide phase shift of 180°.

Thus overall phase shift becomes 360°.