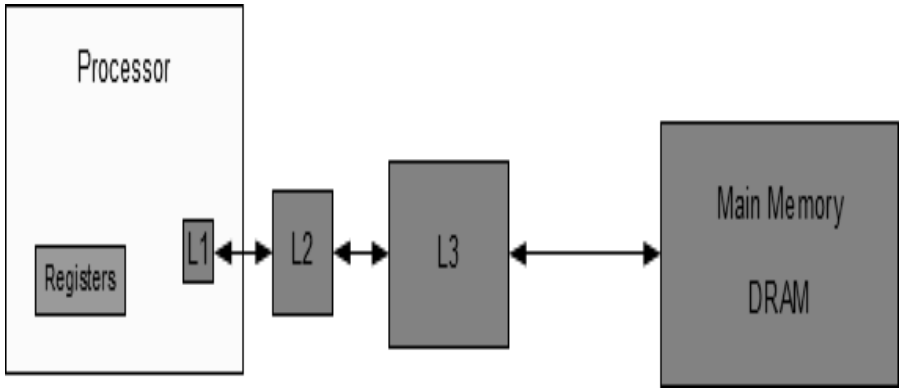
MODEL ANSWER

SUMMER – 2018 EXAMINATION

Subject: Computer Hardware & Networking **Subject Code:** **17533**

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the figure. The figures drawn by candidate and model answer may vary. The examiner may give credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

Q. No.	Sub Q.N.	Answer	Marking Scheme
1.	**a) (i) Ans.**	**Attempt any THREE of the following:** **Explain the concept of cache memory with neat diagram.**  Cache memory is extremely fast memory that is built into a CPU, or located next to it on a separate chip. It supplies the processor with the most frequently requested data and instructions. A cache controller always tries to make sure that the data required by the processor in the next memory access is available in the cache memory.	**12** ***4M*** ***Diagram 1M*** ***Cache memory description 1M***

		There are three types of cache memory: **L1, L2 & L3 cache memory.** **L1 cache memory:** The L1 cache also called internal or integral cache is always a part of the processor chip. L1 cache always runs at full processor speed. It was the fastest cache in the system. L1 cache was originally 8 KB. **L2 cache memory:** The L2 cache originally called external cache because it was external to the processor chip when it was introduced. It was present on the motherboard and used to run at CPU bus speed. To improve the performance of the system, L2 cache was directly incorporated as part of the processor die. L2 cache was originally 128 KB. **L3 cache memory:** The L3 cache has been present in high end work stations and servers such as Xenon and Itanium. Pentium 4 Extreme Edition was the first desktop PC processor with L3 cache. Later Editions of same processor were introduced with larger L2 cache rather than L3 cache.	***Types 2M***
	(ii) Ans.	**State any four preventive maintenance of a Hard Disk Drive.** **Preventive maintenance of Hard Disk** • Take periodic backup of data and critical areas such as boot sectors, FAT and directory structure on the disk. • Defragment the disk to maintain the disk efficiency and speed. • Delete all the temporary files, temporary internet files etc. • Take backup and format the HDD at least once a year and reinstall all the software to maintain disk efficiency and speed.	**4M** ***1M for each maintenance***
	(iii) Ans.	**Draw neat labeled block diagram of flat bed scanner.**	**4M**

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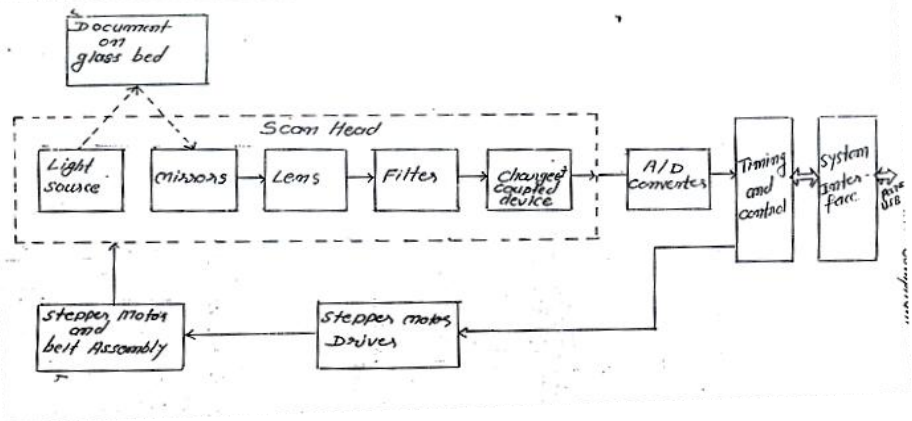
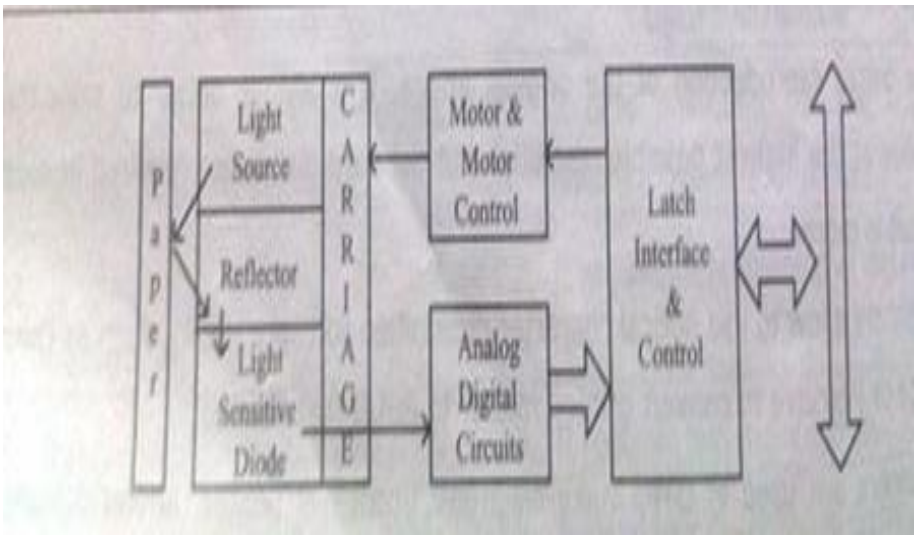
		 **OR** 	***Correct diagram 4M***
	(iv) Ans.	**State any four functions of Internet Protocol (IP).** **Functions of Internet Protocol (IP):** **1) Encapsulation:** The packaging of the transport layer data into a datagram **2) Addressing:** The identification of systems in the network using IP addresses. **3) Routing:** The identification of the most efficient path to the destination system through the IP.	**4M** ***1M for each function***

		4) Fragmentation: The breaking of data into fragments of an appropriate size for transmission over the network.	
1.	**b) (i)** **Ans.**	**Attempt any ONE of the following:** **Draw and explain the function of each layer of TCP/IP protocol architecture.**  **Functions of TCP/IP layers:** **1. Link layer:** The lowest layer of the TCP/IP protocol hierarchy. It defines how to use the network to transmit an IP datagram. Unlike higher-level protocols, link Layer protocols must know the details of the underlying network (its packet structure, addressing, etc.) to correctly format the data being transmitted to comply with the network constraints. The TCP/IP link Layer can encompass the functions of two lower layers of the OSI reference Model (Physical, Data Link layer) **2. Internet layer:** Provides services that are roughly equivalent to the OSI Network layer. The primary concern of the protocol at this layer is to manage the connections across networks as information is passed from source to destination. The Internet Protocol (IP) is the primary protocol at this layer of the TCP/IP model. The functions performed by this layer are: **Routing:** routing consists of two activities, determining path to destination and actual data transfer. **Fragmentation:** every network has a limit on the size of packet that can be	**6** **6M** ***Diagram 2M*** ***1M for each layer description***

		sent. If the data to be transmitted is bigger than this limit, the internet layer breaks the data into smaller packets, this process is called as fragmentation. When internet layer receives such packets at destination side, it reassembles them into complete packet and then transfers it to transport layer. This process is known as reassembly. A message unit in an IP network is called an IP datagram. This is the basic unit of information transmitted across TCP/IP networks. Other internetwork-layer protocols are IP(Internet Protocol), ICMP(Internet control message protocol), IGMP(Internet Group message protocol), ARP(Address resolution protocol). **3. Transport layer:** The most-used transport layer protocol is the Transmission Control Protocol (TCP), which provides connection-oriented reliable data delivery, duplicate data suppression, congestion control, and flow control. This layer performs equivalent functions of the OSI transport layer as well as some OSI session layer functionalities. Transport layer delivers data reliably or unreliably depending on the protocol used. That means TCP provides a reliable service but UDP (User datagram protocol) provides unreliable service. Usually, UDP is used by applications that need a fast transport mechanism and can tolerate the loss of some data. Transport layer provides the mechanism of flow control to prevent sender from sending more data than what the receivers can handle. **4. Application layer:** Application layer performs the functionalities of application, session and some presentation layers of OSI model. Application protocols such as SMTP (simple mail transfer protocol), FTP(File transfer Protocol), HTTP(Hyper text transfer protocol) operates at this layer.	
	(ii) Ans.	**Compare between UTP cable and STP cable. (6-points)**	**6M**

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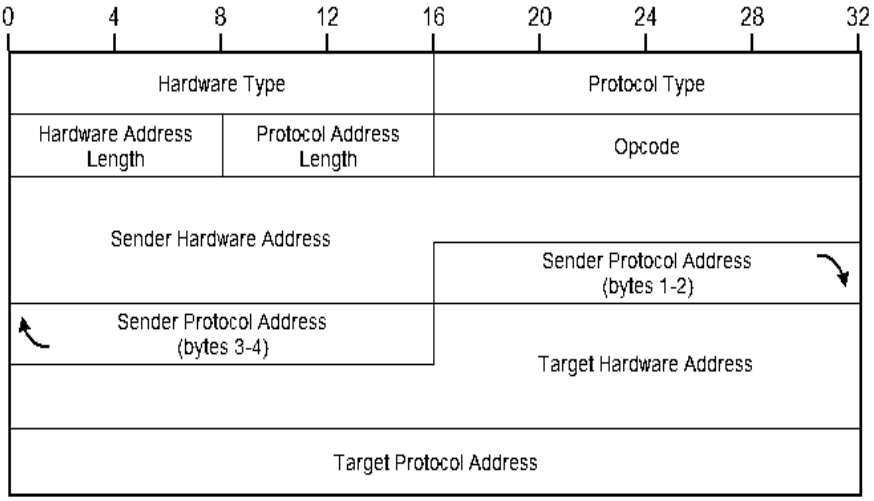
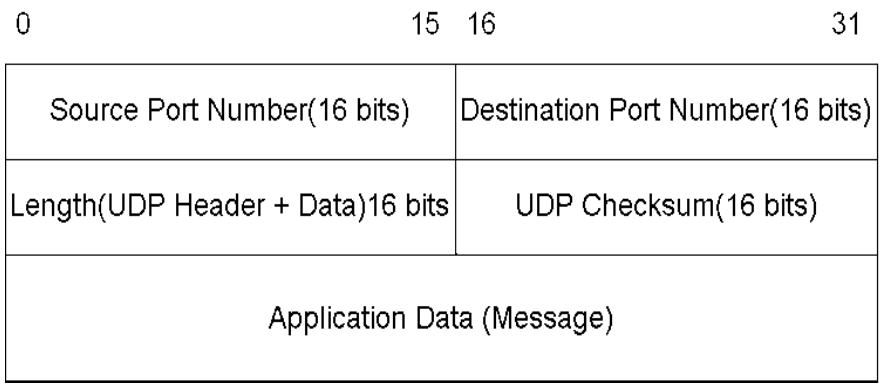
		<table><tr><th>Parameter</th><th>UTP</th><th>STP</th></tr><tr><td>Cost</td><td>Less expensive</td><td>More expensive than UTP</td></tr><tr><td>Speed/bandwidth</td><td>10Mbps to 100Mbps</td><td>10Mbps to 100Mbps</td></tr><tr><td>Security</td><td>Less secure</td><td>Less secure</td></tr><tr><td>Installation</td><td>Easy and less expensive</td><td>Easy but expensive than UTP</td></tr><tr><td>Distance/Cable length</td><td>500m</td><td>100m</td></tr><tr><td>Attenuation</td><td>Very high attenuation</td><td>High attenuation</td></tr><tr><td>EMI/Interference</td><td>Less resistant to EMI</td><td>More resistant to EMI</td></tr></table>	***1M for each parameter***
2.	**a) Ans.**	**Attempt any <u>FOUR</u> of the following:** **State any four features of PCI bus.** **Features of PCI bus:** 1. 33.33MHz clock speed 2. Transfer rate of 133MBps for 32bit bus width 3. 32-bits or 64-bits bus width 4. 32-bits address space 5. 32-bit I/O port space 6. 5V signaling 7. Plug and play facility	**16** **4M** ***1M for each feature***
	b) Ans.	**Explain beep error indications with reference to PC problem (any four)** **(*Note: Beep codes of other manufacturers shall be considered*)** 1 Short beep – Normal POST – System is OK 2 Short beep – POST error – error code shown on screen No beep – Power supply, system board problem, disconnected CPU, or disconnected speaker Continuous beep – Power supply, system board, or may be RAM problem, keyboard problem.	**4M** ***1M for each error***
	c) Ans.	**Explain power on self-test (POST) of PC.** **<u>POST [Power On Self Test]</u>:** Separate test programs called POST are executed by the processor as soon as the PC is powered ON. These programs are confidence tests which verify whether the hardware is free from faults. Only when these tests are successfully run further operation of the PC is permitted. On finding any error, the PC is halted with an	**4M**

		appropriate error message, error code or abnormal symptom. The POST routines are stored in ROM. The POST routine starts from address FFFF0H. The first instruction is usually a JUMP instruction to the address from where the exactly the POST routine starts. The first instruction is CLI [Clear Interrupts]. Then POST starts executing test programs. The POST sequence followed in IBM PC is as follows: 1. 8088/86 processor test. 2. Initial housekeeping checksum test. 3. 8K BIOS ROM checksum test. 4. Timer 1 test. 5. Test DMA controller. 6. Initialize DMA channel 0 for memory refresh. 7. Start timer1 for memory refresh. 8. Set mode for DMA channels 2 and 3. 9. Enable I/O expansion box. 10. First 16K DRAM test. 11. System memory authorizing. 12. Initialize stack. 13. Initialize PIC-8259A. 14. Set up interrupt vector table. 15. Determine system configuration. 16. Confirm whether manufacturing test mode or user mode. 17. Initialized CRT controller 6845. 18. Test video RAM. 19. Display a horizontal bar on screen. 20. Test CRT interface lines. 21. Test interrupt controller. 22. Test Timer 0. 23. Initialize Timer 0. 24. Test Keyboard. 25. Set up hardware interrupt vector table. 26. Expansion I/O box detection and test. 27. Test remaining system RAM after 16K. 28. Test terminal count status of DMA channel 0. 29. Recognize optional ROM and do checksum. 30. Do checksum test for BASIC ROM. 31. Decide if FDC test to be skipped. 32. Test FDC.	***Correct explanation 4M***

		33. Detect presence of parallel and serial ports. 34. Reliability tests completion. 35. Enable NMI 36.Call bootstrap loader. A hardware engineer will be able to understand the system problems quickly if the engineer has a clear idea of POST sequence and execution and various types of errors indications by POST at different stages. The various method of error indications are as follows: • Hang or Halt of system. • Sound beeps. • Checkpoint Entry. • Error codes. • Detailed Error message.	
	d) Ans.	**Give the ARP protocol message format.**  	**4M** ***Correct ARP protocol message format 4M***
	e) Ans.	**Draw and explain the packet structure of UDP.**	**4M**



Structure 2M

Source port: Source port is an optional field. When used, it indicates the port of the sending process and may be assumed to be the port to which a reply should be addressed in the absence of any other information. If not used, a value of zero is inserted.

Destination port: It is the port number on which the data is being sent.

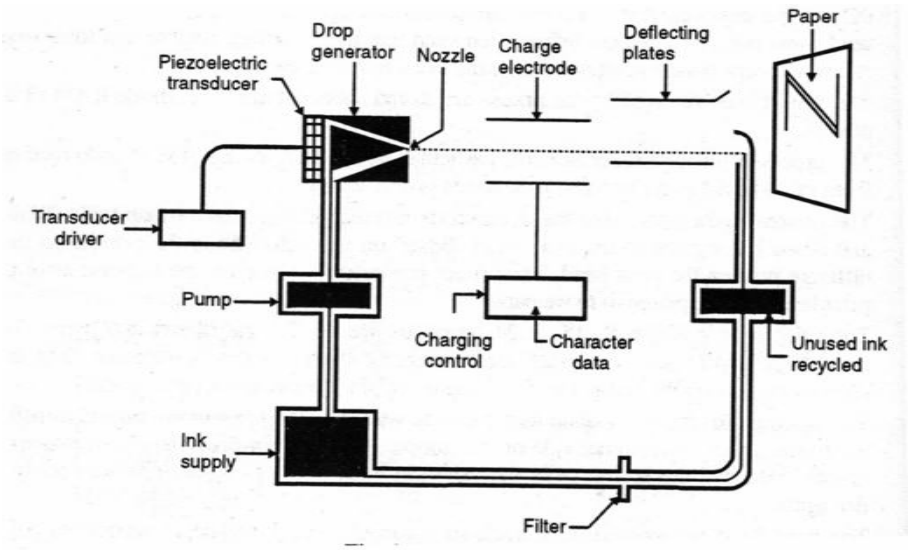
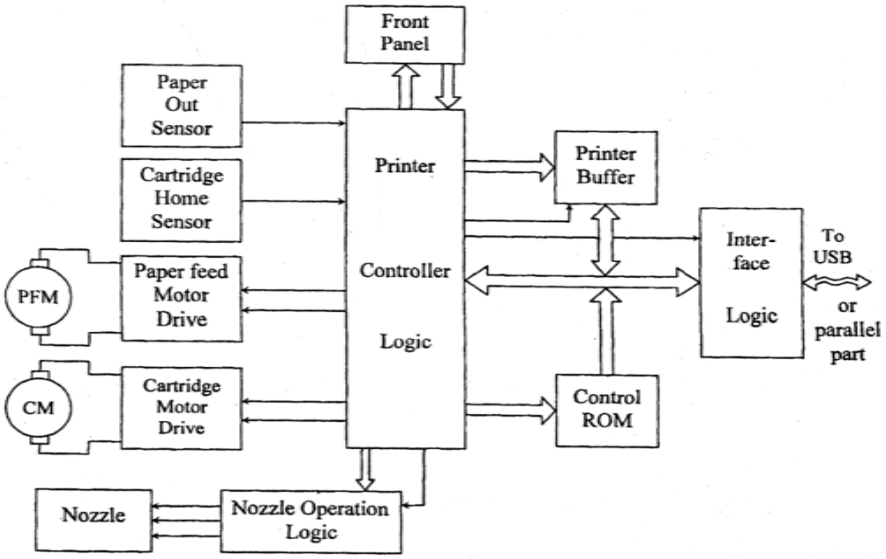
Explanation 2M

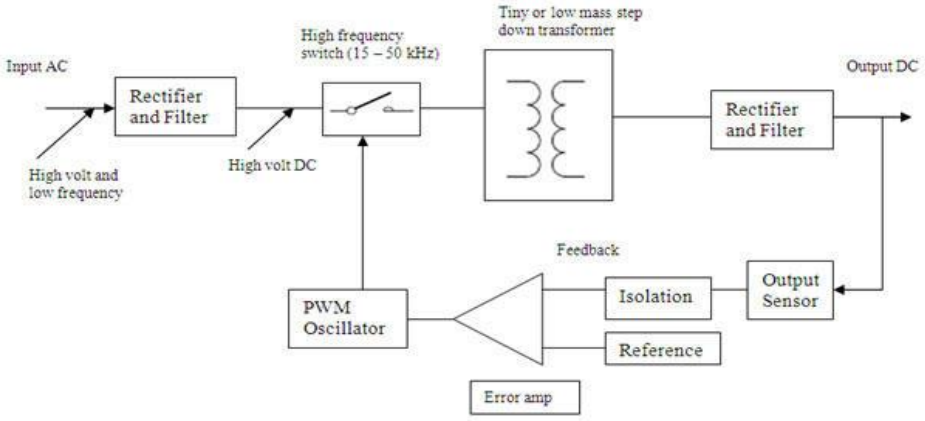
Length: It includes the length of UDP Header and Data.
The length in octets of this user datagram, including this header and the data. The minimum value of the length is eight.

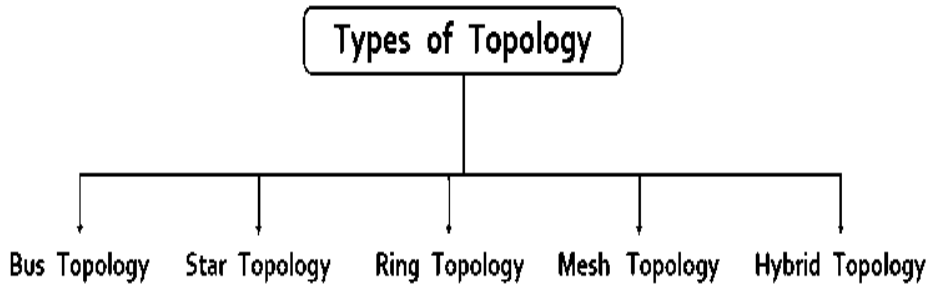
Checksum: The main purpose of checksum is error detection. It guarantees that message arrived at correct destination. To verify checksum, the receiver must extract these fields from IP Header .12-byte pseudo header is used to compute checksum.

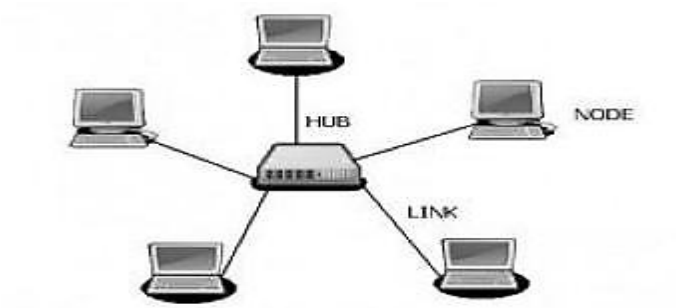
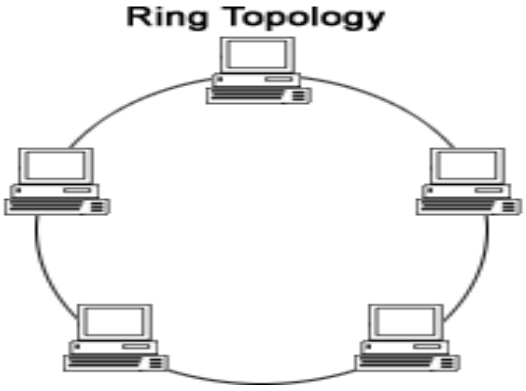
Data: It is the application data or Actual message.

3.		**Attempt any TWO of the following:**	**16**
	a)	**Explain the working of Inkjet printer with neat block diagram. State its two limitations.**	**8M**
	Ans.	It is a non-impact printer. It provides letter quality printout than dot matrix printer. Its output is sharper than Dot matrix though its output quality is not to the same level of laser printer & it is cost is less than Laser printer. In inkjet printer, ink is emitted from nozzles as they pass over the media. A print head scans the page in horizontal strips, using a motor assembly rolls the paper in vertical steps. A strip of image is printed, then the page moves on, ready for the next strip. To speed up things the print head doesn't print	***Explanation 4M***

		just a single row of pixel in each pass but a vertical row of pixels at a time.  **OR**  **<u>Principle</u>:** Conductive ink is forced through a very small nozzle to produce a high-speed stream or jet of drops of inks. The size and spacing of these drops are made constant by vibrating, the nozzle compartment at an ultrasonic frequency with a piezo crystal mounted at one end of the cavity.	***Diagram 2M***

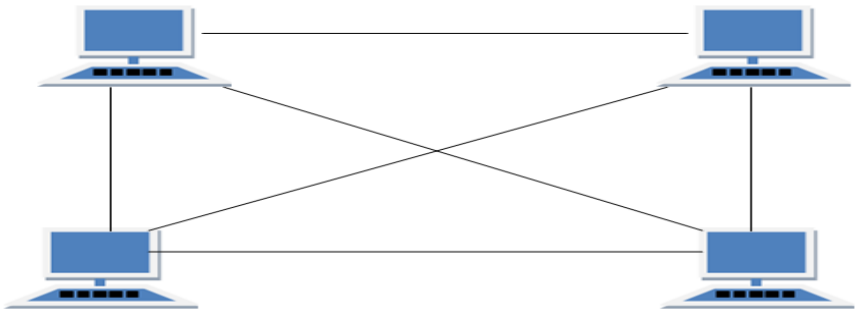
		The vibrating frequency is around 100 KHz; the drop diameter is 0.06mm and the spacing 0.15mm. Each drop of ink after leaving the cavity is given a specific amount of electrical charge as it passes through a charging electrode structure, which is located at the point at which the stream breaks up into drops. The drops are deflected vertically by a second electrode structure and strike the printing structure. The amount of deflection is determined by the charge originally imparted to the drop. With no charge imparted there is no deflection. **<u>Limitations:</u>** ➢ Ink-jet printers require periodic maintenance or else the ink gets logged in the nozzle. ➢ They require special paper with controlled absorbency for best results. ➢ Ink cartridges are costly than ribbon and don't last longer.	***Any two limitations 1M each***
	b) **Ans.**	**Draw the block, diagram and explain the working of SMPS. Give any two functions of PWM in SMPS.**  The performance of a PC depends upon the proper functioning of power supply. SMPS are commonly used power supply due to its small size, low cost and high efficiency. In SMPS a switching transistor is used in place of linear stabilizer. The transistor is opened and closed at high frequency. As a result there is no power loss in such devices. In this there is no continuous supply but a pulse waveform is used. The switching rate is about 20 KHz. But the SMPS suffers from the disadvantage of ripple voltage, and noise level at the output is high. Two types of switching logic are followed in the SMPS design: Pulse	**8M** ***Diagram 2M*** ***Explanation 4M***

		Width Modulation (PWM) and another is resonant approach. But the PWM method is normally employed in SMPS. In PWM the DC voltage is chopped at high frequency. The resultant square wave voltage is either stepped up or down by using transformer. The transformers secondary output voltage is rectified and filtered. The regulation in the o/p voltage is achieved by varying the duty cycle of the square wave. The outputs voltage is compared with the reference and by controlling the duty cycle of the drive signal applied to the switching circuit, the o/p voltage is maintained constant. After comparison with the reference the error voltage is fed to the PWM. The optoisolator provides isolation for the control loop against any pick up from the main path. The output of the optoisolator is amplified by the driver stages that controls the switching transistor. **<u>Functions of PWM:</u>** 1. The PWM provides a means to close the feedback loop in the switch mode power supplies that use for general system intelligence and control. 2. The integration of the PWM's SMPS input and output through its voltage comparator and current sense amplifiers, plus its MOSFET driver, enable designers to sue this single device to perform many different functions in their designs. 3. The result is smaller design foot print and lower overall cost.	***Any two functions of PWM 1M each***
	c) **Ans.**	**Give the classification of network topology. Explain any two network topology in details.** **<u>Network topology</u>:** The topology of a network is the geometric representation of the relationship of all the computers or links with linking devices (usually called nodes) to one another.  	**8M** ***Classification 2M***

		1) <u>Star Topology</u>: In this topology, nodes are connected to central cable; here all the hosts or workstations are connected to central device called hub. All the data on the star topology passes through the central device before reaching the intended destination.  STAR TOPOLOGY ***<u>Advantages:</u>*** • A single computer failure does not affect the entire network. • Easy to expand – Adding new node in Network is easy. • Centralized control-It enhance N/w monitoring &management. • Fault detection is easy because all nodes are connected to central HUB **2) <u>Ring Topology</u>:** A network topology that is setup in circular fashion. In other words all nodes in ring topology are connected in ring. ***Structure:*** In ring topology, each computer is connected to the next computer where the last computer is connected to the first.  ***<u>Advantages:</u>*** • This type of network topology is very organized.	***Explanation of any two topology 3M each***

- Each node gets to send the data when it receives an empty token. This helps to reduces chances of collision.
- Also in ring topology all the traffic flows in only one direction at very high speed. Even when the load on the network increases, its performance is better than that of Bus topology.
- There is no need for network server to control the connectivity between workstations.
- Each computer has equal access to resources.

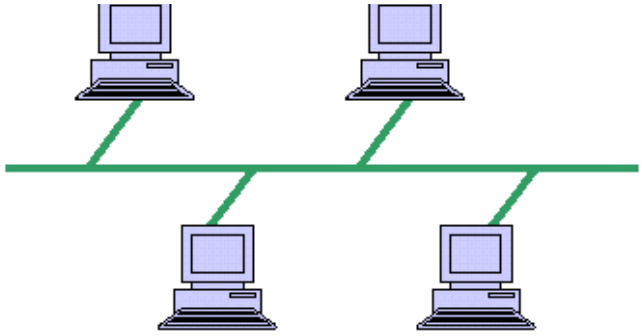
3) Mesh topology: In mesh topology, every device is connected to another device via particular channel.



Advantages:

1. Each connection can carry its own data load.
2. It is robust.
3. Fault is diagnosed easily.
4. Provides security and privacy.

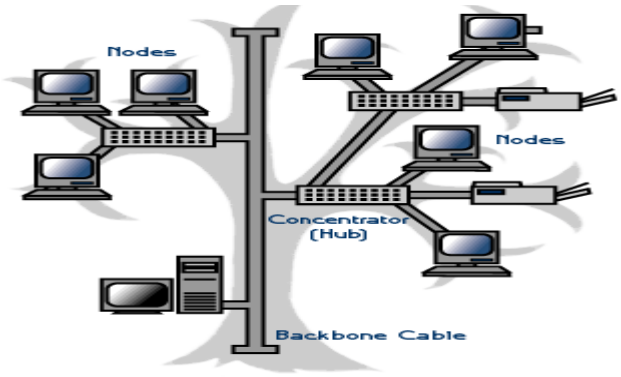
4) Bus Topology:



Advantages:

- If N devices are connected to each other in bus topology, then the number of cables required to connect them is 1 which is known as backbone cable and N drop lines are required.
- Cost of the cable is less as compared to other topology, but it is used to built small networks.

5) <u>Tree Topology</u>:



Advantages:

- Point-to-point wiring for individual segments.
- Supported by several hardware and software venders.